Design of CMOS Proteretic Device and its Applications

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by

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CERTIFICATE

It is certified that the work contained in this thesis, titled **"Design of CMOS Proteretic Device and its Applications"** by Salma Khan, has been carried out under my supervision and is not submitted elsewhere for a degree.

Date:

Advisor : Dr. Syed Azeemuddin

Abstract

The semiconductor industry is driven by the need to design smaller, faster and low power consuming circuits. A comparator is an integral part of any electronic system and by default the comparators exhibit hysteresis phenomenon. A Schmitt trigger is the most commonly used comparator in circuit design. Rigorous efforts have been made to speed up the circuit performance by various techniques at the system, circuit and transistor level and they have demonstrated incremental improvement. However, all these efforts are focused on reducing the switching time between the logic levels and shortening the width of hysteretic loop while maintaining noise immunity. This thesis presents a new paradigm shift from the conventional techniques of circuit speed up wherein the hysteretic device itself is replaced with a proteretic one and efforts to improve the circuit speed have been demonstrated successfully. Hysteresis has an inherent switching delay, whereas, proteresis or inverse hysteresis demonstrates an early response to the switching action of the circuit.

Proteresis is a known phenomenon across various domains like pharmacokinetics (PK) and pharmacodynamics (PD) drugs, ferro-electric materials and optical bi-stable devices, but their impact and study in area of Integrated circuits has been very limited. This is because proteresis is induced by feed forwarding the input to couple of hysteretic devices (Schmitt trigger) and this leads to output of circuit being stable for a small input ranges and prevalent instability over the remaining input range. However, this thesis proposes a novel mechanism of stabilizing the proteretic output over a wide input voltage range and hence leverages the benefit of early switching characteristics for improving the circuit speed by a factor of 25%. A detailed mathematical model for proteretic circuit design over various input ranges is presented and the trade-off in terms of area and power is also discussed with the ramp generator as a design example.

Hysteretic and proteretic devices are bi-stable and their interstate switching depends on triggering voltages. Conventionally, devices can be classified to work as either hysteretic or

proteretic. This thesis proposes the first attempt to describe a circuit that switches between two opposite characteristics of hysteresis and proteresis to present a new circuit called Prohys switch. The output of prohys switch demonstrates a limited amount of randomness in its first cycle of operation and this factor is a strong reason to employ a prohys switch for designing a Physical unclonable Function (PUF).

In recent times PUF's has gained immense popularity for securing the IC's by providing unique identification code to each chip. The key design parameters of a PUF are uniqueness and reliability and designing a highly efficient PUF with optimal values of uniqueness and reliability is quite a challenge. Reliability depends on the chip's ability to resist changes to supply voltage and temperature variations, whereas, uniqueness depends on process variations during chip fabrication. Multiple PUF designs that employ reliability enhancement circuits and security algorithms achieve these design characteristics. Nonetheless, these techniques are design overheads. Finally, this thesis presents a novel PUF based on the proHys switch called the prohys PUF. The proposed prohys PUF befittingly satisfies both uniqueness and reliability criteria, without any additional circuitry or security algorithms.

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List of Abbreviations

IC	Integrated Circuits
VTC	Voltage Transfer Characteristics
PUF	Physical Unclonable Function
DDDR	Dual-Domain Dynamic Reference
SOT-MRAM	Spin Orbit Torque Magnetic Random Access Memory
TDD	Time Domain Detection
PK	Pharmacokenetics
PD	Pharmacodynamics
TERU	Torasemide Excretion Rate in Urine
PMP	Piezoelectric Micro-positioning Platform
ST	Schmitt Trigger
BTS	Barium Stannate Titanate
DEA	Di-electric Elastomer Actuator
SOA	Semiconductor Optical Amplifier
PLL	Phase Locked Loop
HI	High Impedance
FOM	Figure of Merit
ProHys	Proteresis - Hysteresis
RO	Ring Oscillator
BER	Bit Error Rate
DWM	Domain-Wall Memory

HD	Hamming Distance
RAM	Random Access Memory
SRAM	Static Random Access Memory
RFID	Radio Frequency Identification
ASIC	Application Specific Integrated Circuit
FPGA	Field Programmable Gate Array
DFF	Delay Flip Flop
CRP	Challenge Response Pair

List of Symbols

μ	Mobility of majority carriers
ε_o	Permittivity of free space
ε_r	Relative permittivity of silicon-dioxide
$\mathbf{t}_{ox}$	Thichness of oxide layer between gate and channel
$\mathbf{V}_{TP}$	p-channel threshold voltage
$\mathbf{V}_{TN}$	n-channel threshold voltage
$\mathbf{V}_{DD}$	Supply voltage

Chapter 1

Introduction

1.1 Background

Systems that demonstrate bi-stability and encounters frequent interstate changes, exhibit hysteresis. The expected performance of an ideal system is that the transition from one state to another happens at a threshold level, irrespective of the direction of change i.e. from high to low or vice-versa. However, all naturally occurring phenomena exhibits two thresholds, one for going from low to high (upper threshold) and the other for going from high to low (lower threshold). Conventionally, the change does not happen at the first available threshold and is normally delayed and is termed as hysteresis. Inverters and schmitt triggers are good examples of circuits that demonstrate hysteresis.

Consider an ideal sinusoidal input applied to an inverter which also works as a single bit analog to digital converter that varies between V_{DD} and V_{EE} with 0V as the threshold point. The ideal input and output of the inverter along with voltage transfer characteristics is shown in Fig. 1.1. Now consider a sinusoidal signal which gets interfered with environmental noise and gets distorted. This noisy signal when transmitted through an inverter or a buffer (two inverters in series) generates a signal shown in Fig. 1.2. It is observed that the switching is triggered more often than actually required. This obtained signal varies from the desired signal due its multiple transitions and will also consume more power than the former case.

This problem can be avoided by using noise resistant or noise immune hysteretic devices and the Schmitt trigger is the most common circuit implementation of a hysteretic device. To get hysteresis, a circuit requires two thresholds instead of one (i.e) one for rising edge and another

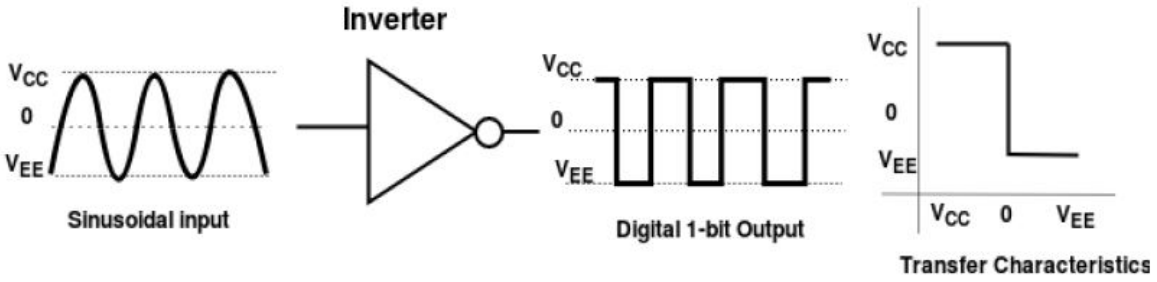


Figure 1.1: Response of inverter to ideal sinusoidal input

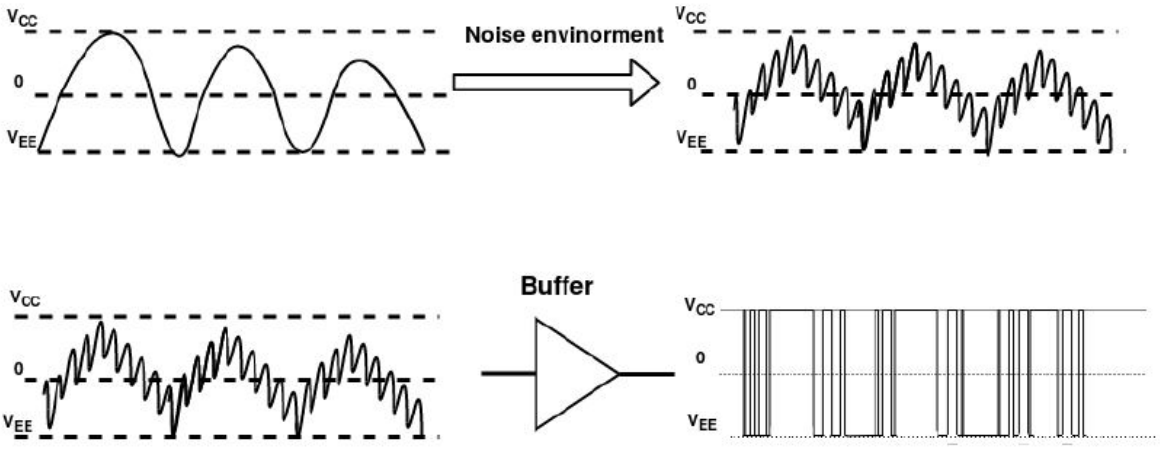


Figure 1.2: Noisy sinusoidal signal and its response to a buffer

for the falling edge [1; 2]. If the system's VTC follows hysteresis , then the problem of multiple transitions can be avoided thus obtaining a digital output similar to expected signal as shown in Fig. 1.3.

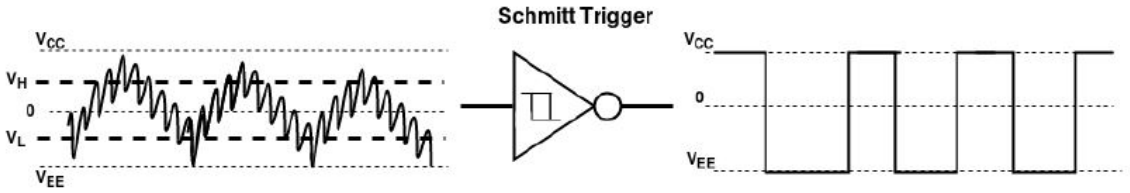


Figure 1.3: Response of schmitt trigger to noisy sinusoidal input

The Schmitt trigger performs the role of a two level comparator by default. The entire gamut of circuits used in analog to digital conversion and other analog applications implement comparators using the hysteretic design. These devices are used in memory elements [3], image sensors [4; 5], wireless analog transceivers [6], retinal prosthetic device [7], ramp generators

[8; 9] and ADC's [10].

1.2 Voltage Transfer Characteristics (VTC) of hysteresis and proteresis

Hysteresis refers to a phenomenon where there is a delay between the cause and its effect. Schmitt trigger circuits demonstrate hysteresis and are used in analog to digital conversion and improve noise immunity in signals. Proteresis is the reverse effect of hysteresis, it is described as the phenomenon where the cause has an early effect or response [11]. A proteretic device is supposed to speed up the system without losing the benefit of noise immunity [12]. Hysteretic and proteretic devices are bistable and their interstate switching depends on triggering voltages.

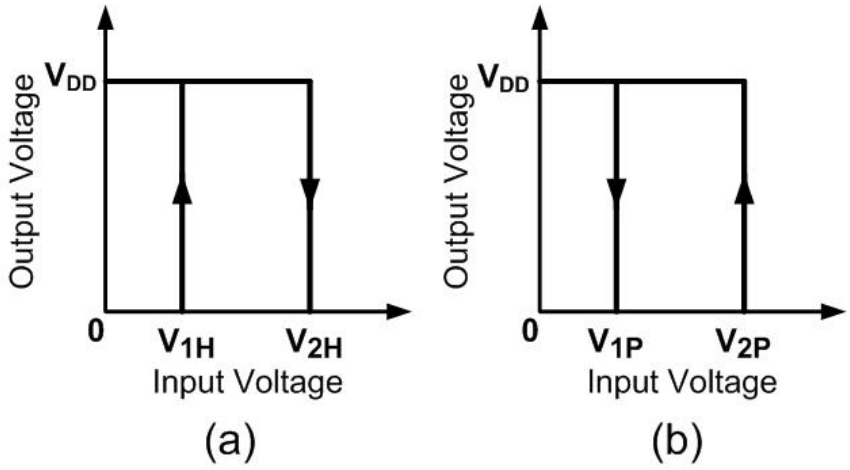


Figure 1.4: VTC of inverting (a) Hysteresis (b) Proteresis

The Voltage transfer characteristics (VTC) of hysteresis and proteresis are given in Fig. 1.4(a) and Fig. 1.4(b) respectively. The switching happens from V_{DD} (supply voltage) to 0V or vice-versa in both the phenomena's. The rising and falling edges of hysteresis indicate the triggering voltages V_{1H} and V_{2H} respectively. When the input signal is lower than the upper triggering voltage V_{2H} the output stays high, the curve then drops around that point. The output stays low as long as the input is higher than the lower triggering voltage V_{1H} as shown in Fig 1.4(a). The VTC depicts that transition from one state to another occurs after a significant delay.

On the other hand, proteresis is given by two triggering voltages V_{1P} and V_{2P} describing the falling and rising edges of the device respectively as shown in Fig. 1.4(b). The output stays

high as long as the input is below the lower triggering voltage V_{1P} then it becomes low. Next, the input must reach a point above the upper triggering voltage V_{2P} then, the output rises when the input signal becomes lower than V_{2P}. It indicates the onset of state transition, which is advanced, unlike hysteresis, where it is delayed. The noise immunity can be set by the circuit designer by varying the width of the hysteresis loop and it is given as the difference between two triggering voltages.

1.3 VTC from inverter to proteresis

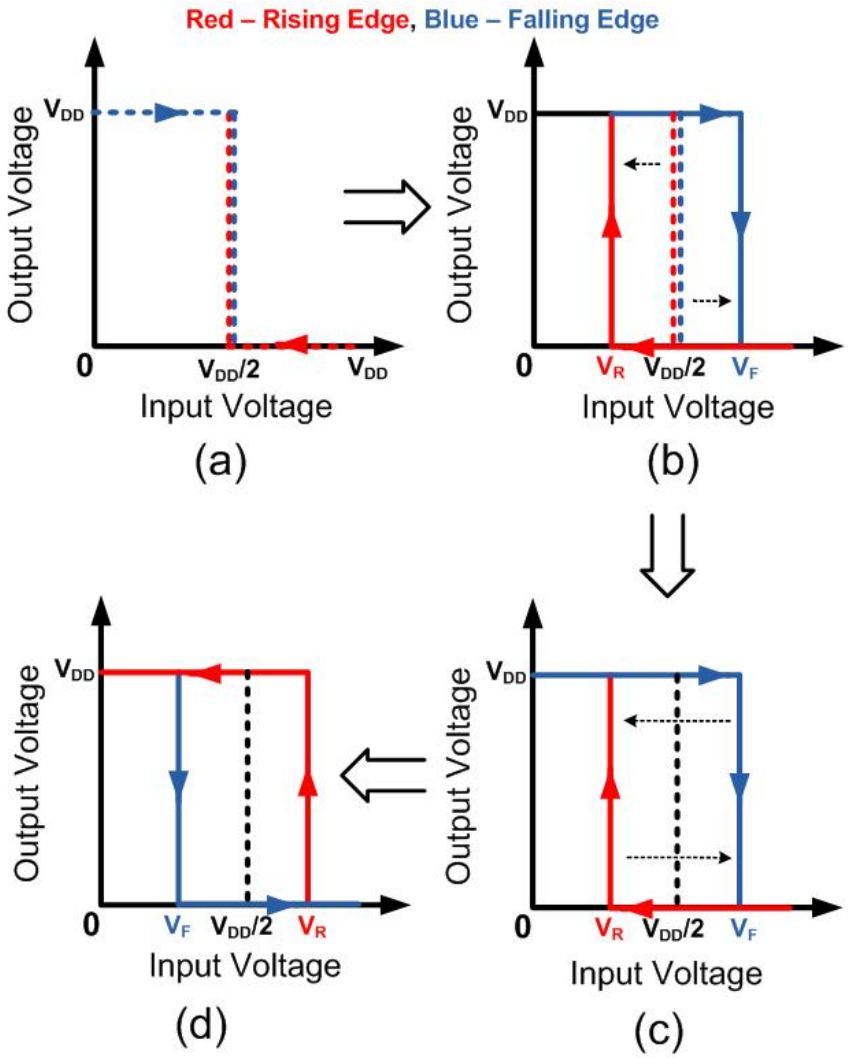


Figure 1.5: VTC of (a) Inverter, (b) Transition from inverter to hysteresis, (c) Transition from hysteresis to proteresis, and (d) Proteresis

The ideal characteristic of an inverter is shown in Fig. 1.5(a), with the forward and reverse

triggering which occurs at the same point $0.5V_{DD}$. As we tend to practicality, a loop is formed with two triggering voltages and the falling edge is shifted right, from $0.5V_{DD}$ to V_F and rising edge is shifted left to V_R as seen in Fig. 1.5(b). In both cases, the trigger points are delayed and hence the loop is known as the hysteretic loop. This work focuses on various efforts in system design, for interchanging the positions of rising and falling edges as seen in Fig. 1.5(c), which finally results in proteretic characteristics as seen in Fig. 1.5(d). This process is termed as proteresis because of the early transition in both directions, well in advance of $0.5V_{DD}$. Due to this advancement, proteretic based systems can be explored to achieve high speed performance with an area trade-off. A significant transformation to be observed from Fig. 1.5(c) is that, in hysteresis V_R is less than V_F and in proteresis V_R is greater than V_F. The loop width in both cases is the difference between the rising and falling edges and this loop voltage defines the noise immunity.

1.4 Applications of Schmitt Trigger as Comparator

Schmitt trigger is used as a comparator in many applications such as clock generator circuit used in power converters, flash ADC and ramp generators. This section gives an overview of schmitt trigger used as comparator for different circuits.

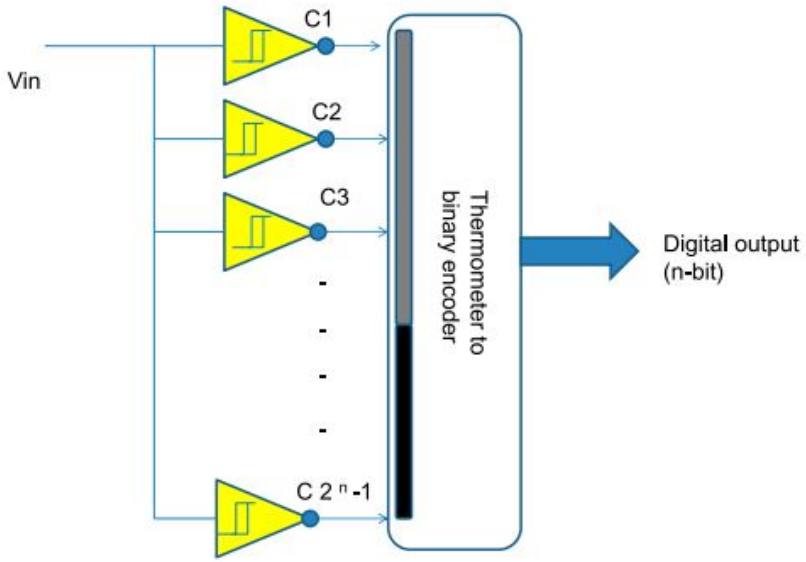


Figure 1.6: Schmitt Trigger based comparator array [13]

1.4.1 Flash ADC Circuit

Schmitt trigger based comparator array is shown in Fig. 1.6 which demonstrates the flash ADC structure. It generates a comparator array with temperature stability over a range of temperatures which can be used to replace the conventional methods including reference voltage source, voltage divider network and differential comparator array for flash ADC's. It contains sized CMOS Schmitt inverters (with n number of ADC bits) followed by a thermometer to binary encoder. This further generates n-bit digital output [13].

1.4.2 R-to-F (Resistance to Frequency) Converter

The schmitt trigger-based design shown in Fig. 1.7(a) is less complex, but standard circuits are not able to achieve high oscillation frequency. To increase the oscillation frequency compared to standard ST-based RC oscillators, a circuit with narrow equivalent hysteresis gap is shown in Fig. 1.7(b). The circuit design with narrow gap is used as R-to-F converter [14].

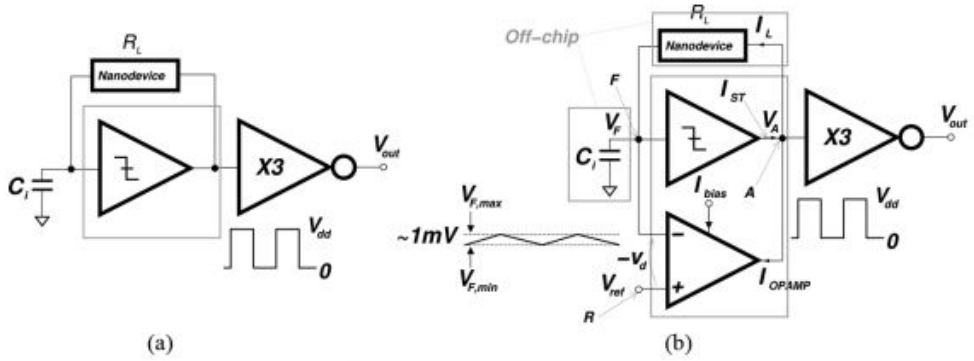


Figure 1.7: (a) Standard Schmitt-Trigger based oscillator, (b) Operational Schmitt Trigger R-to-F Converter [14]

1.5 Problem statement

Hysteresis and proteresis are two existing phenomena's which are complementary in nature. It is shown in section 1.3 that hysteresis experiences an in-built switching delay in the circuit, while proteresis has an early response to the switching action of the circuit. In order to implement

high speed comparators, one of the key constraints is the width of hysteresis loop. The circuit designers have struggled with the idea of designing an ideal comparator that gives a minimal hysteretic loop width and high circuit speed at the same time, but they are restricted by the physical design boundaries of hysteresis phenomena where the transition from one level to the other will take place after a set delay and no amount of logical effort can minimize this phenomenon. This thesis is based on the problem statement of speeding up the circuit design by considering an alternate switching approach complimentary to the conventional method of hysteretic design, this work proposes the implementation of reverse hysteretic or proteretic design.

1.6 Research objectives

The key objectives in this thesis is focused on establishing the new design methodology of proteretic circuit design and demonstrating that various circuits can be implemented at speeds higher than hysteretic designs. Further, the secondary objective is to discuss the challenges involved in design of proteretic circuit in terms of stability of the output, to perform circuit analysis and suggest solutions for the same. A circuit implementation of the proteretic comparator for design of a ramp generator is presented as a comparative analysis between hysteretic and proteretic designs. Thirdly, the best features of both hysteretic and proteretic designs can be achieved by using a combined circuit that can switch between the two operations of proteretic and hysteretic and christened as Prohys switch. Finally, the thesis also demonstrates the application of proposed prohys design to implement a Physical Unclonable Function (PUF).

1.7 Thesis outline

The subject matter of the thesis is presented in the following seven chapters,

Chapter 1 gives a background on the default presence of an inverter or buffer circuit. The inverse hysteretic or proteretic phenomenon is explained using the voltage transfer characteristics. Further, it defines the problem statement and the thesis objectives are elaborated.

Chapter 2 discusses the literature survey on the phenomena of hysteresis and proteresis in multidisciplinary domains such as CMOS circuits, pharmacokinetics (PK) and pharmacodynamics (PD) drugs, ferro-electric materials and optical bistable devices.

Chapter 3 gives the detailed mathematical analysis of hysteretic and proteretic circuits and presents the key design constraints in output stabilization and measures thereof to design a working proteretic circuit.

Chapter 4 highlights the design of a ramp generator using both the hysteretic and proteretic comparator. A comparative analysis of speed, area and power giving a detailed overview of the trade-off using proteretic comparator is presented.

Chapter 5 presents the design of a ProHys switch implementation using both hysteresis and proteresis as two modes of operation. This new technique switches the mode of operation using a control input signal and empowers the user to choose between various design constraints as per system requirements.

Chapter 6 presents the need of the PUF and its various types. The design of novel ProHys PUF using ProHys switch is presented. The proposed PUF design gives a significant improvement in the parameters when compared to the existing PUF designs.

Chapter 7 highlights the conclusion and future scope of the proteretic circuits as an additional option to the designers to improve speed of the system. Further it describes the applications of prohys circuits that can be worked upon in the future.

Chapter 2

Literature Review on Hysteresis and Proteresis

2.1 Introduction

Hysteresis is a naturally occurring phenomenon, which was first noticed in ferromagnetic substances [15], where magnetic induction lags behind the magnetizing force. Later on, hysteresis was observed in several other phenomena, like in physics to encounter plasticity, friction, ferromagnetism, ferroelectricity, superconductivity, absorption are to name a few. It also exists in chemistry, biology, economics and even in psychology. Further, it appears in spin glasses, mechanical damage and fatigue [16; 17]. Also in electrochemical domain for design of lithium ion batteries [18] and solar cells [19].

Hysteresis for electronic devices are generally designed using schmitt trigger circuits. Schmitt trigger generates two triggering voltages known as upper triggering voltage and lower triggering voltage [20]. Schmitt trigger circuits are designed to control hysteresis with respect to current [21] and voltage [22], which are used for retinal sensing [23] and in frequency doubler [24]. It has a low power variant for low power applications [25]. Hysteresis has countless applications in the fields of medicine, sensors and electronics.

Proteresis works on the principle opposite to that of hysteresis. Analogous to hysteresis, proteresis is also a naturally occurring phenomenon. Its behaviour advances the effect of the response and leads the switching action. The inherent delay caused by hysteresis is eliminated in proteresis. Using proteresis, the response of the device is advanced improving the overall speed

of the system. Generally, the triggering points (i.e upper and lower) of hysteresis are reversed which makes the system faster in transition without losing its noise immunity characteristics [26; 27].

Proteresis is observed in the magnetic topology of a dirac cone [28], the magnetic loop of a mixed spin Ising system [29] and in anti-ferromagnetic alloys [30; 31]. It is also observed in nanoparticles like Cu_{2O}/CuO and cobalt [32; 33], polycrystalline-silicon thin-film transistors [34] and in different kinds of drugs [35].

However, implementation of proteretic effect have not been studied extensively in CMOS except for an old study on transition accelerator circuit [36], and the latest implementation of the proteretic device as a comparator for energy harvesting [37]. Commonly, the default behaviour of any electronic system is hysteretic, and when certain boundary conditions are imposed on it, the system can behave in proteretic mode.

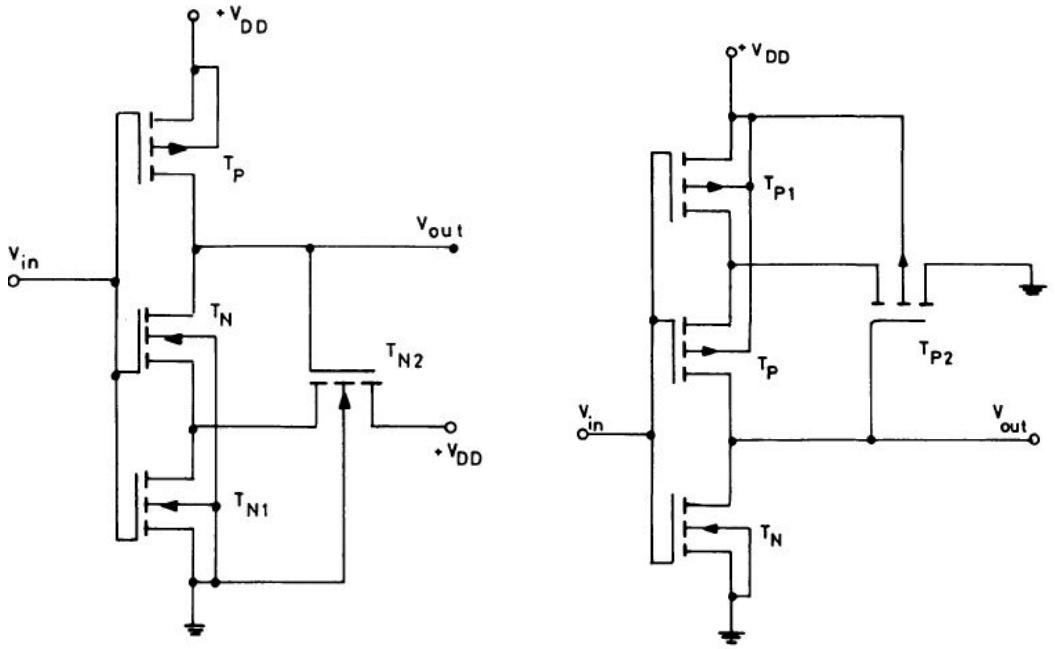
The broad scope of this thesis is in the area of CMOS analog IC design. The key objective of the work is to study the well-established phenomenon of hysteresis and then delve into the lesser known area of anti-hysteresis, also known as proteresis. This chapter intends to do a thorough literature survey on schmitt trigger based hysteretic circuits using their electrical characteristics. Further, a detailed study of proteretic devices is also presented.

2.2 Hysteresis models

CMOS schmitt trigger demonstrates two types of circuit design generating hysteresis, which are four transistor model and six transistor model. The four transistor model is designed using two variants, first consists of three NMOS transistors and one PMOS transistor, while the other consists of one NMOS and three PMOS transistors. The second type of Schmitt trigger model with three pairs of CMOS transistors is also described. These models are initially described by [38] and the accurate analysis of the integrated Single input schmitt trigger circuits are given in [39].

2.2.1 Schmitt trigger circuit using four transistor model

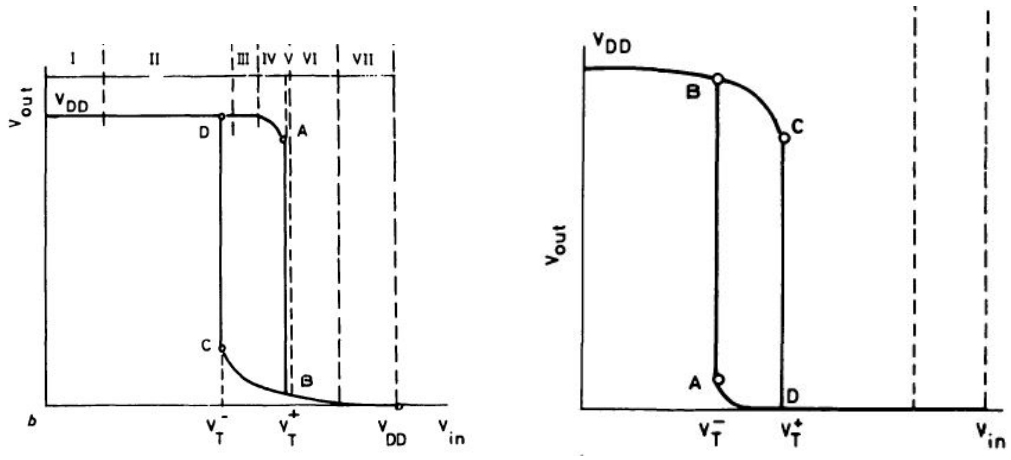
The hysteresis voltage depends on transistor geometry and supply voltage. The first type consists of only 4 transistors as shown in Fig. 2.1(a) and (b). Fig. 2.1(a) is designed using 3 NMOS transistors TN, TN1, TN2 with one PMOS transistor TP. This circuit fixes the lower triggering voltage at the midpoint of the supply voltage (V_{T-}) and the higher triggering voltage (V_{T+}) is achieved at the voltage greater than the supply voltage. Similarly, Fig. 2.1(b) is designed using three PMOS transistors TP, TP1 and TP2 with one NMOS transistor TN. It fixes the higher triggering voltage ad the midpoint of the supply voltage (V_{T+}) and the lower triggering voltage (V_{T-}) is achieved at the voltage less than the supply voltage as shown in Fig. 2.2. Thus, giving a small hysteresis loop which mainly depends on the noise immunity of the system.



(a) (b)

Figure 2.1: Circuit with (a) One PMOS and three NMOS transistors, (b) One NMOS and three PMOS transistors [38]

Hysteresis of both circuits in Fig. 2.1(a) and (b) depends on the ratio of the constants (β_n/β_p) of TN, TN1, TP and TP1, as well as on the geometries of TN2 and TP2, and the supply voltage (V_{DD}). These designs are used for dual-domain dynamic reference (DDDR) sensing scheme for reliable read operation in spin orbit torque magnetic random access memory (SOT-MRAM) where the four transistor model named as half Schmitt trigger is used for time domain



(a) (b)

Figure 2.2: VTC of (a) One PMOS and three NMOS transistors, (b) One NMOS and three PMOS transistors [38]

detection (TDD) unit and which are efficiently exploited to design the dynamic reference approach to generate data-dependent reference voltages [40].

The circuits using 4 transistor models demonstrate a narrow hysteresis window and hence have low noise immunity. A wider hysteresis window for the same supply voltage and the same geometry of transistors can be obtained if the circuits in Fig. 2.1(a) and (b) are combined in one circuit.

2.2.2 Schmitt trigger circuit using six transistor model

This section describes in detail about circuit threshold of six transistor schmitt trigger design and the switching analysis from one stable state to another when the circuit is in linear operation [41]. It calculates the transistor aspect ratios or device sizes by using threshold tolerances. The VTC of CMOS Schmitt trigger is shown in Fig. 2.3.

Based on the input signal, two input-output characteristics can be observed as shown in Fig. 2.3. If the input goes from low (0) to high (V_{DD}) voltage level, the output state is changed at V_{HL} where the output goes from high (V_{DD}) to low (0) and vice versa, it switches from low (0) to high (V_{DD}) at V_{LH}. The V_{HL} and V_{LH} can be found when the input and output voltages are equal at operating points OP1 and OP2. This gives a more broader window of noise immunity compared to four transistor model.

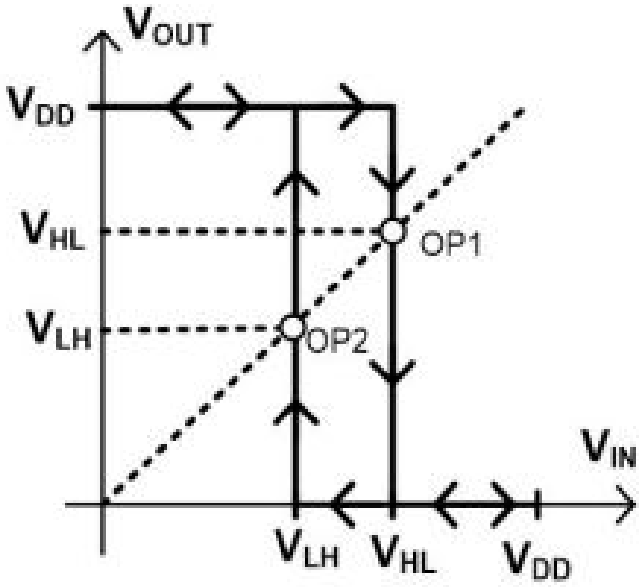


Figure 2.3: VTC of six transistor model [39]

This model is used in various applications like design of swarms of robots for single-hydrophone low-cost underwater vehicle swarming [42], in digital temperature sensor, suitable for thermal management in nanometer CMOS technologies [43], and in power detector system for milli-meter wave [44].

2.2.3 Adjustable schmitt trigger model

This section deals with the design of schmitt trigger with adjustable hysteresis loop using additional two external signals as inputs. One is used to control the upper triggering voltage and the other is used for the lower triggering voltage. It is divided into semi-adjustable and fully adjustable schmitt triggers. The former design keeps one control input fixed and varies the other, which keeps one triggering voltage constant at a time and varies the other triggering voltage. The latter varies both the control inputs, which in turn varies both the triggering voltages. Based on the variation of these control inputs the switching voltages can be adjusted. This also gives an improved hysteresis loop with better noise immunity [22].

These adjustable schmitt triggers are used to design a variation and noise-aware reliable dynamic logic gates [45] and in sigma-delta modulator [46]. Hysteresis is defined using different variants and types in the literature using various transistor models to improve the noise

immunity of the device. It also specifies the applications for each of the described models. The following section deals with proteresis models.

2.3 Proteresis models

Proteretic, a complimentary effect to well-known hysteresis, is an interesting phenomenon. If the hysteresis loop is considered as anticlockwise in nature then the proteresis loop behaves as reversed hysteresis and is clockwise in nature, similarly this is also true otherwise. Unlike in hysteresis, where the onset of switching happens after a delay, in proteresis the switching effect occurs early. Proteresis is given as anti-hysteresis, reverse- hysteresis, clockwise hysteresis and inverse hysteresis in different fields.

2.3.1 Proteresis in various fields

Proteresis is exihibited in varying conditions as described below. It exists in medicinal drugs, ferro-electric substances, dielectric materials, actuators, optical devices and many more.

2.3.1.1 Pharmacokinetics (PK) and pharmacodynamics (PD) medicines

Proteresis exists in various domains improving the aspect of hysteresis. This is initially discussed in Pharmacokinetics (PK) and pharmacodynamics (PD) drugs. PK deals with the study of what the body does to the drug i.e. the timeline of the drug's absorption, bioavailability, distribution, metabolism and how your body excretes it, and PD deals with the study of what the drug does to the body i.e. it refers to how the drug works and how it exerts its power on the body in terms of physical activity. The effect of three different drugs used for psychiatry patients - lorazepam, alprazolam and diazepam is discussed. This typical characteristic is used by doctors to prescribe medication to psychiatry patients based upon their behavioural patterns [47].

It is shown that the drug concentration in the body increases with time, reaches a peak and then gradually reduces with time and in completing this cycle hysteretic or proteretic features are demonstrated. It is observed that in the drug Diazepam, there is an early effect of the drug on the tracking activity of the volunteer and similarly there is an early offset indicating

the clockwise hysteresis (proteresis) response. This is in contrast to the other two drugs of Alprazolam and lorazepam where the drugs follow the conventional PD characteristics of late onset and late offset reflected as anticlockwise hysteresis. [48]. Further, it is used as intravenous tocilizumab following single-dose in patients with arthritis [49] and on subjects related to dose of venlafaxine on cardiac repolarization in healthy patients [50].

A similar modelling approach was seen to determine a dosage regime which maximizes the efficiency of torasemide drugs in dogs. Kinetic profiles of plasma concentration, torasemide excretion rate in urine (TERU) and diuresis were investigated in 10 dogs after single oral administrations at 3 dose levels. Domestic regulation was seen by a proteresis loop between TERU and diuresis [51].

2.3.1.2 Ferro-Electric barium stannate titanate ceramics

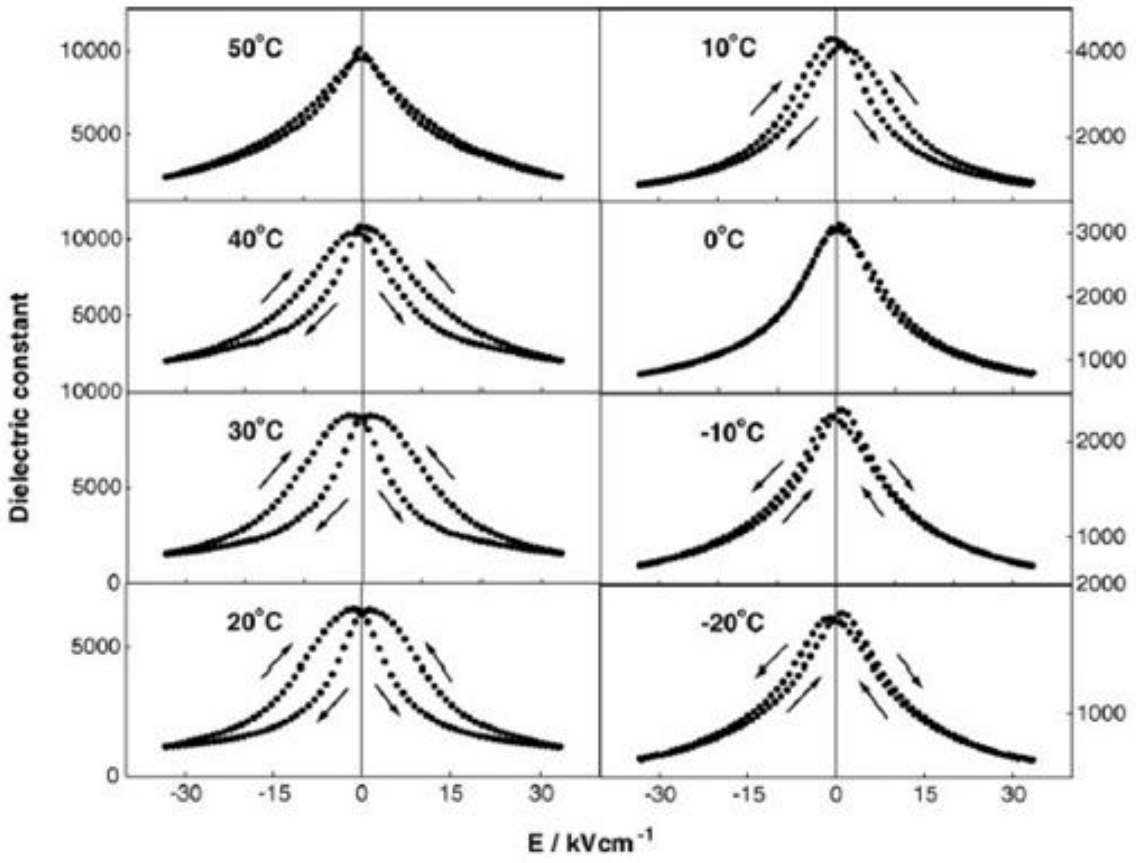


Figure 2.4: Variation of di-electric constant of BTS10 with respect to applied Electric Field at various temperature conditions from 50°C to -20°C [52]

It presents the variation in dielectric constant with respect to applied Electric field for the

Barium stannate titanate (BTS) material. In case of non-linear dielectric materials the dielectric constant can be controlled by adjusting the field strength. Such materials can be used to design dielectric amplifiers, frequency multipliers, phase shifters etc. in phased array antennas. The capacitance to voltage (C-V) characteristics of BTS demonstrated clockwise hysteresis (proteresis) in the temperature range of 10-40°C [52].

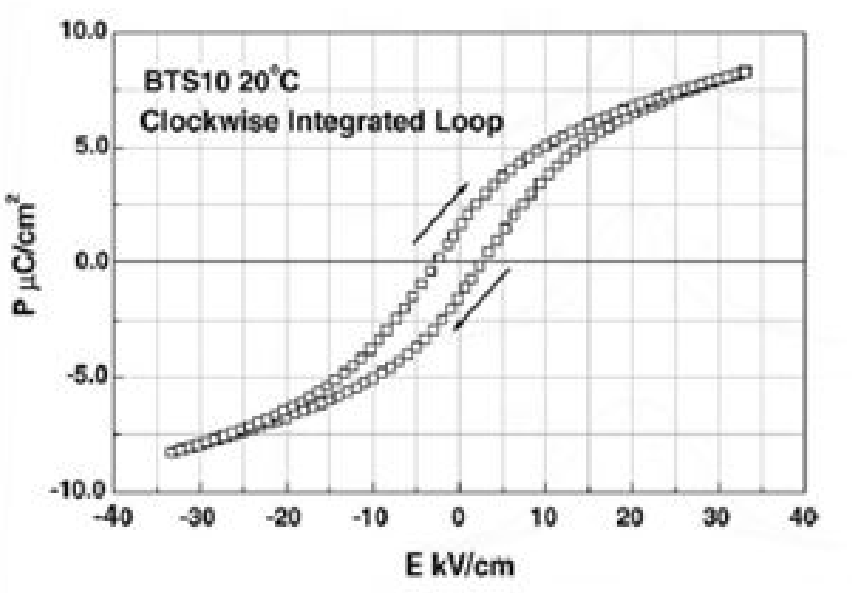


Figure 2.5: Clockwise integrated polarization hysteresis loop of BTS10 at 20°C [52]

It is observed in Fig. 2.4 that at -20°C and -10°C the curve is hysteretic in nature, at -0°C the C-V curve is hysteresis free. Now at temperatures of 10°C, 20°C, 30°C and 40°C the phenomena of reverse hysteresis (proteresis) is observed. As the electric field E is varied from -40 KiloVolt/cm to +40 KiloVolt/cm, it is observed that the di-electric constant has an early take off and when the field is brought back from 40 KiloVolt/cm to -40 KiloVolt/cm an early takeoff is again observed, thus making the loop demonstrate clockwise hysteresis or proteretic properties which is unobserved in other ceramic materials in normal conditions and even in BTS10 at other temperatures apart from 10°C to -40°C. The same is plotted to get the C-V curve shown in Fig. 2.5.

2.3.1.3 Actuator device models

The hysteresis phenomenon is widely used in mechanical applications as well, like dampers, actuators etc, the hysteretic process is a featured non-linearity that has a rate-independent memory effect. However, in reluctance actuators the eddy currents leads to a rate-dependent asymmetric

hysteresis effect. The same is overcome by feed-forwarding the input to a second stage and implementing a reverse hysteretic or proteretic design [53]. Another application of hysteresis is in dielectric elastomer actuator (DEA) wherein there is marked asymmetry in the hysteretic response due to visco-elasticity of the DEA. This asymmetry is mitigated by using an inverse-hysteretic or proteretic compensator where the input is fed forward to attain an overall linear response in the DEA [54]. The piezoelectric actuator proposed in [55] also discusses an adaptive projection algorithm wherein the inverse hysteretic model is applied and its parameters are automatically updated. A reference model is studied for piezoelectric micro-positioning platform (PMP) for high precision tracking and positioning applications [56].

2.3.1.4 Optical Systems

Proteresis also exists in optical devices and are gaining lot of interest due to their speed upsurge in comparison to their electronic counterparts. It is seen in all-optical phase and amplitude regenerator [57], all-optical neural network [58], all-optical neurosynaptic networks [59]. Further, it is designed using semiconductor ring lasers [60], and radio frequency bio-sensing systems [61].

A semiconductor optical amplifier (SOA) exhibits a delay due to relaxation dynamics of the system and hence increase the modulation rate. The simulation of all optical proteretic device is done in [62]. The results are presented in MATLAB for both hysteresis and proteresis as shown in Fig. 2.6. It shows non-inverting input-output relationship in optics where proteresis is given by blue and hysteresis by red curve describing the opposite nature.

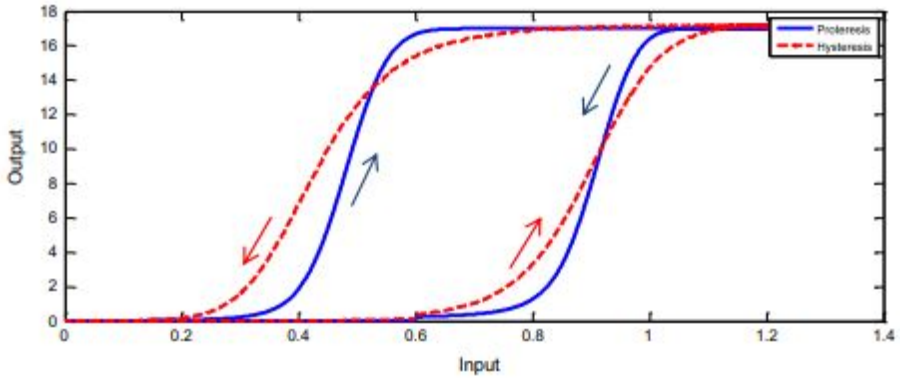


Figure 2.6: VTC of hysteresis and proteresis in optical domain [62]

Proteresis is experienced in all the major existing domains as described in detail in this

section. This phenomena is explored and utilized in latest applications. This can be further applied in circuits domain, where its existence is very limited. The following section discusses proteresis in the CMOS domain.

2.3.2 Proteresis in CMOS design

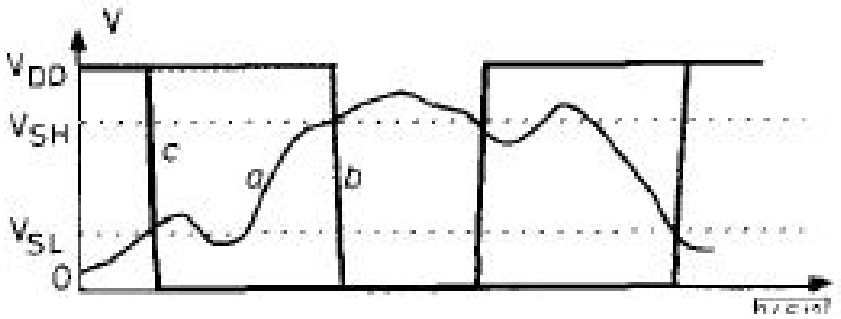


Figure 2.7: Transient response (a) Input signal, (b) Hysteretic output, and(c) Proteretic output [36]

Proteretic devices using CMOS circuits are very limited in the literature. Proteresis is achieved when some initial conditions are forced on the hysteresis. The basic premise of a Schmitt trigger circuit is to transform noisy or poorly shaped signals into well-shaped rectangular pulses. However, it should be noted that the Schmitt trigger is responsible for a noticeable delay between input and output transitions, especially when the input signal has long transition times as shown in Fig. 2.7 [36]. This gives a non-inverting proteretic response and the output switches from high to low at the higher triggering voltage as the input decreases and output switches from low to high at the lower triggering voltage as the input increases.

Further, the new schmitt trigger design is presented, which allows low voltage operation, with higher speed than existing hysteresis. This principle is extended to the design of a very compact window comparator [63]. Proteretic comparator is recently used in the design of an energy harvester circuit for wireless power transmitter based on a imbalance of the PMOS current mirror as a function of the comparator output [37].

The section described the proteresis phenomenon in various fields and builds the background to design CMOS IC‘s as an accelerator circuit thus speeding up the applications in which the phenomenon is used. The conditions required to maintain the system stability in proteretic phenomena are stringent and the same will be explored in the following sections.

Chapter 3

CMOS Implementation of Hysteretic and Proteretic Devices

This chapter deals with the CMOS circuit level implementation of hysteretic and proteretic devices. The design of a basic six transistor Schmitt trigger circuit which gives a hysteretic performance along with its design equations is presented. This design is then extended with a combiner to design the proteretic device. Finally, the issue of unstable output of proteretic device is resolved by adding a third stage of inverter or a Schmitt trigger circuit.

3.1 Hysteretic devices

This section deals with the design of schmitt trigger circuit generating hysteresis, taking into consideration the mathematical equations, based on the switching action of the device.

3.1.1 Circuit level implementation of schmitt trigger

The most common CMOS circuit that implements hysteretic operation is the Schmitt trigger circuit [41] shown in Fig. 3.1. It is a six transistor implementation with three NMOS transistors (MN1-MN3) and three PMOS transistors (MP1-MP3). The transistors MP3 and MN3 form the crux of the circuit. The aspect ratio of transistors MN3, MP3, MN1 and MP1 are crucial in deciding the falling edge voltage and rising edge voltage, respectively, which in-turn define the switching action of the circuit. The input signal to the circuit is given by V_{in} and the hysteretic

output is generated as V_1.

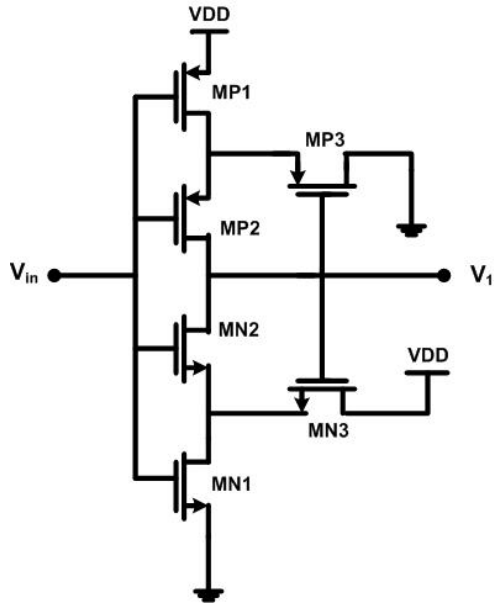


Figure 3.1: Schmitt trigger circuit [41]

The working of all transistors of Fig. 3.1 is based on the input voltage V_{in} of schmitt trigger is given in Table 3.1. When the input is logic '0' the NMOS transistors MN1 and MN2 are OFF and PMOS transistors MP1 and MP2 are ON. Due to this output V_1 is V_{DD} and consequently MP3 is turned OFF and MN3 is turned ON. The reverse operation is observed when V_{in} is given an input voltage of V_{DD}. The operation during the transition stages of voltage from logic 0 to logic 1 and vice-versa is discussed in the next section along with modelling equations for triggering voltage.

Table 3.1: Transistor operation of schmitt trigger circuit

V_{in}	**MP1**	**MP2**	**MP3**	**MN1**	**MN2**	**MN3**	**V_1**
0	ON	ON	OFF	OFF	OFF	ON	V_{DD}
V_{DD}	OFF	OFF	ON	ON	ON	OFF	0

3.1.2 Mathematical modelling of schmitt trigger circuit

The triggering voltage depends on the P sub-circuit and N sub-circuit. The rising edge is dependent on the flow of current through the P sub-circuit giving the lower triggering voltage

V_L. The N sub-circuit is responsible for the higher triggering voltage V_H of the schmitt trigger. The relationship between device dimensions on the triggering operation in terms of threshold voltages as described in [41] are distinctly laid out in equations (3.1) and (3.2) given below.

$$\frac{K_{MP1}}{K_{MP3}} = \left\{ \frac{V_L}{V_{DD} - V_L - |V_{TP}|} \right\}^2 \tag{3.1}$$

$$\frac{K_{MN1}}{K_{MN3}} = \left\{ \frac{V_{DD} - V_H}{V_H - V_{TN}} \right\}^2 \tag{3.2}$$

$$K_i = 0.5(\mu_{n/p} C_{ox}) \frac{w_i}{l_i} \tag{3.3}$$

Where, V_{TN} and V_{TP} are n-channel and p-channel threshold voltages. w and l are width and lengths of the transistors. V_{DD} is the supply voltage of the circuit. μ is the mobility of majority carriers. $C_{ox} = (\varepsilon_0 * \varepsilon_r)/t_{ox}$. ε_0 is the permittivity of free space, ε_{ox} is relative permittivity of SiO_2, t_{ox} is thickness of oxide layer between gate and channel.

The equations of rising edge (V_L) and falling edge (V_H) of the schmitt trigger using above equations are written as follows,

$$V_L = \frac{(V_{DD} + |V_{TP}|)\sqrt{\frac{(w/l)_{MP1}}{(w/l)_{MP3}}}}{(1 + \sqrt{\frac{(w/l)_{MP1}}{(w/l)_{MP3}}})} \tag{3.4}$$

$$V_H = \frac{V_{DD} + V_{TN}\sqrt{\frac{(w/l)_{MN1}}{(w/l)_{MN3}}}}{(1 + \sqrt{\frac{(w/l)_{MN1}}{(w/l)_{MN3}}})} \tag{3.5}$$

The circuit is designed using TSMC 180nm CMOS parameters based on the above equation, to obtain the w/l values of transistor aspect ratio given in Table 3.2. The rising and falling

edges are calculated using equation (3.4) and (3.5) for desired w/l values are to be $V_L = 0.4171V$ and $V_H = 1.382V$ and the same is practically observed using cadence simulation.

Table 3.2: Width and length (w/l) of all the transistors of the schmitt trigger circuit

Transistor	**Dimension (w/l)**	**Transistor**	**Dimension(w/l)**
MP1	2μ/180n	MN1	2μ/180n
MP2	10μ/180n	MN2	5μ/180n
MP3	10μ/180n	MN3	10μ/180n

3.1.3 VTC of schmitt trigger

The schmitt trigger circuit is simulated in CMOS TSMC 180nm technology to generate a response between input (V_{in}) and output (V_1) voltages to get the transfer function. The VTC of the schmitt trigger is shown in Fig. 3.2, demonstrates the rising edge V_L in red curve at 0.42V and falling edge V_H in blue curve at 1.38V. These values are close to the calculated values mentioned above. The loop voltage of hysteresis is calculated as $V_H - V_L = 1.38 - 0.42 = 0.96V$. This shows that the rising edge is less than the falling edge and the schmitt trigger behaves like a hysteretic device.

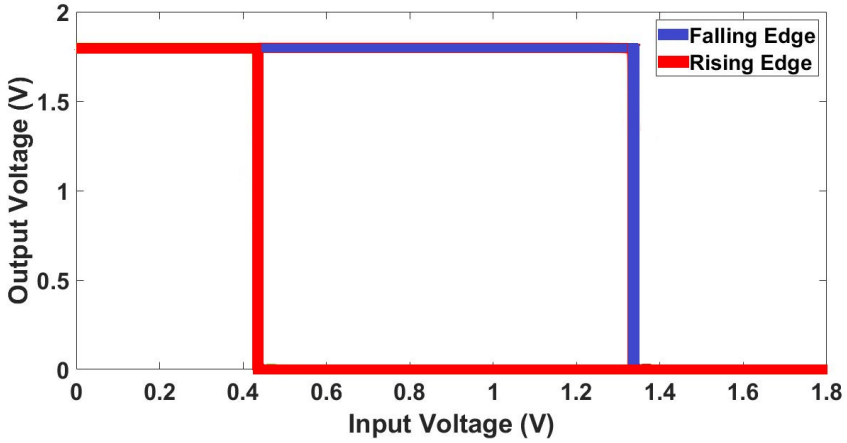


Figure 3.2: VTC of hysteretic schmitt trigger circuit

The values of lower (V_L) and higher (V_H) triggering voltages of schmitt trigger circuit for different process corners is simulated and is placed in Table 3.3. It is observed that the variation is minimal i.e. 0.03V in V_L and 0.04V in V_H.

Table 3.3: V_L and V_H values for Different Process Corners

Process Corners	**V_L(V)**	**V_H(V)**
FF	0.39	1.38
FS	0.39	1.34
SF	0.42	1.38
SS	0.42	1.34

3.2 Proteretic devices

The proteretic circuit is an extension of hysteretic circuit and the main challenge is to interchange the positions of the rising and falling edges. The first stage of proteretic will always be a hysteretic circuit and then its output is subsequently modified by mixing it with the input voltage which is fed forward for creating the effect of proteresis. Proteresis is achieved when some initial conditions are forced on the hysteretic block. These conditions are discussed in detail in this section.

3.2.1 Conditions for proteresis

The first stage of proteresis is always a schmitt trigger circuit which generates two triggering voltages (V_L and V_H). These voltages have to satisfy two main conditions to get proteresis. The conditions are

1. The lower triggering voltage (V_L) of the first stage comprising of schmitt trigger should be less than the n-channel threshold voltage V_{TN}.

$$0 < V_L < V_{TN} \tag{3.6}$$

2. The higher triggering voltage (V_H) of the first stage comprising of the schmitt trigger should be in the range from difference between supply voltage (V_{DD}) and p-channel threshold voltage (V_{TP}) and supply voltage.

$$(V_{DD} - |V_{TP}|) < V_H < V_{DD} \tag{3.7}$$

3.2.2 Circuit level implementation of intermediate proteresis

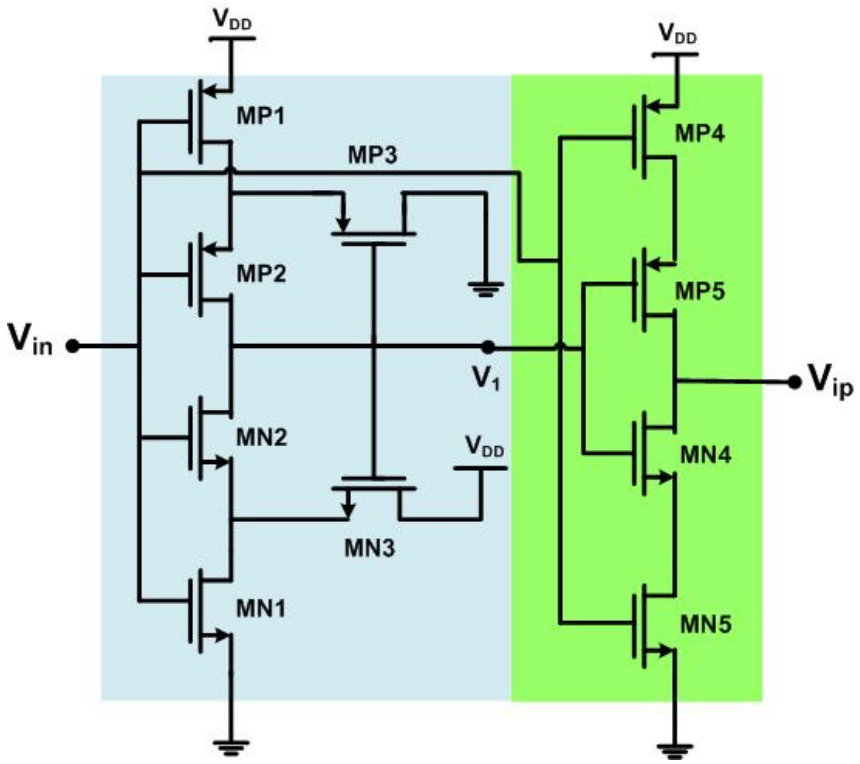


Figure 3.3: Circuit diagram of intermediate proteresis

The circuit diagram of intermediate proteresis is given in Fig. 3.3, which consists of two stages, first is the schmitt trigger and second is the summer stage. In first stage, conditions for proteresis are satisfied using triggering voltages given above. The input to the first stage is V_{in} and the output is V_1. This is followed by the second stage of summer. The summer circuit consists of two PMOS (MP4 and MP5) transistors and two NMOS (MN4 and MN5) transistors. The summer combines the output of the first stage V_1 and the input from the first stage is fed forward generating an intermediate proteresis output (V_{ip}).

This output is called as intermediate proteresis as it gives a high impedance (HI) state for few portions of input voltage V_{in}. However, the output is present in the undefined region of HI for a specific range of input signal, putting constraints on the design values of triggering voltages, thus leading to unstable operation of proteretic device. The second stage transistors switch on and off due to varying conditions of the first stage output (V_1) due to presence of two NMOS and two PMOS transistors in the summer.

The state transition diagram of the output V_{ip} is given in Fig. 3.4. It describes two different

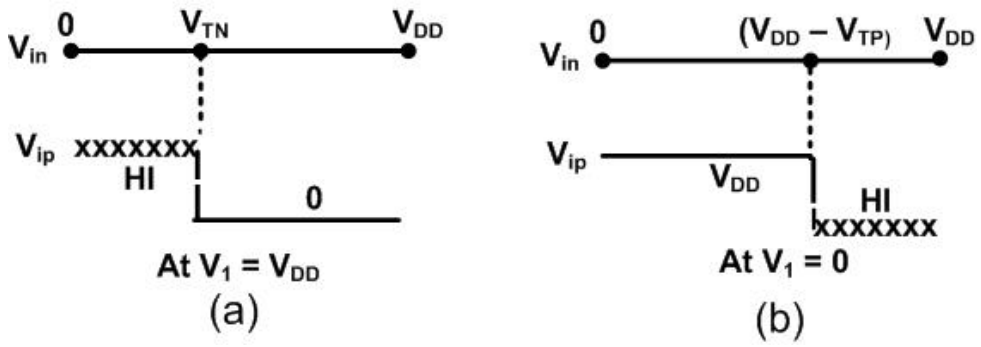


Figure 3.4: State transition diagram

states of output V_{ip}, one at $V_1 = V_{DD}$ and second at $V_1 = 0$, for V_{in} varying from 0 – V_{DD} and vice – versa. The detailed operation of the transistors of the second stage is given in the Table 3.4 with the specific range of input voltage V_{in} from region 1 (R1) to region 4 (R4).

Table 3.4: Transistor operation of second stage of proteretic circuit

V_{in}	**V_1**	**MP4**	**MP5**	**MN4**	**MN5**	**V_2**
$0 \leq V_{\text{in}} \leq V_{\text{TN}}[R1]$	V_{DD}	ON	OFF	ON	OFF	HI
$V_{TN} \leq V_{\text{in}} \leq V_{\text{DD}}[R2]$	V_{DD}	ON/OFF	OFF	ON	OFF	0
$0 \leq V_{\text{in}} \leq (V_{\text{DD}} - V_{\text{TP}})[R3]$	0	ON/OFF	OFF	OFF	OFF	V_{DD}
$(V_{DD}\text{-}V_{TP}) \leq V_{\text{in}} \leq V_{\text{DD}}[R4]$	0	OFF	ON	OFF	ON	HI

The ranges R1 to R4 as given in table above are as follows.

R1: When the transition is from 0 – V_{DD}, V_{in} is initially 0 and V_1 is V_{DD}, the second stage output V_{ip} is in HI state till V_{in} reaches V_{TN}.

R2: As V_{in} ranges from V_{TN} to V_{DD} and V_1 is V_{DD}, then V_{ip} comes to 0V.

R3: Similarly, when the transition is from V_{DD} – 0, as V_{in} varies from (V_{DD} - V_{TP}) to 0, V_{ip} rises to V_{DD}.

R4: When the transition is from V_{DD} – 0, for V_{in} from V_{DD} to (V_{DD} – V_{TP}), V_{ip} is in HI state.

The HI state for R1 and R4 makes the circuit unstable in this input range. It is desired to have a stable output (V_{DD} or 0) for the complete input voltage range. This stability issue is resolved by including a final stage to bring the intermediate proteresis output V_{ip} to either 0 or V_{DD}. This is done by adding a third stage to the present circuit. There are two different techniques used to stabilize the proteresis output. The first is by adding a simple inverter as a

third stage. This generates a comparatively small loop voltage. The second technique uses a schmitt trigger again at the third stage which increases the loop voltage, which in turn increases the noise immunity of the circuit. Both these techniques eliminates the HI state and generates a stable proteretic output.

3.3 Implementation of stable proteretic design

This section discusses about two different variants of stable proteretic device. First, is the variant which has first two blocks as schmitt trigger and summer, and third block as inverter. Second, has the same two blocks with the third block of schmitt trigger.

3.3.1 Proteresis using inverter as third stage

This technique uses the third stage as a simple inverter shown in Fig. 3.5, which generates a stable proteretic output V_{out}. The detailed circuit diagram of the proteretic device using inverter is given in Fig. 3.6. The stability issue is resolved by including a final stage inverter that maintains the output at stable 1 or 0 without allowing it to slip into a high impedance state.

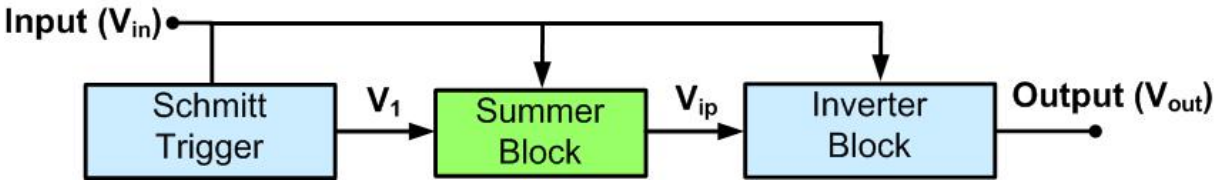


Figure 3.5: Block diagram of proteretic device using inverter as third stage

The design includes an output inverter stage whose output V_{out} is shorted to the intermediate proteresis output V_{ip}. Due to this arrangement, the inverter driven by feed-forward input V_{in}, will function such that either MP6 or MN6 will be ON, to pull-up or pull-down the output V_{out} to V_{DD} or 0V, whenever it is in HI state, thus stabilizing the proteretic design for entire voltage swing.As mentioned in the previous section in R1 and R4 there is a HI state. For R1, MP6 is ON and MN6 is OFF, pulling up HI state to V_{DD} and in R4, MP6 is OFF and MN6 is ON, moving HI state to ground (0). Thereby, eliminating the HI state.

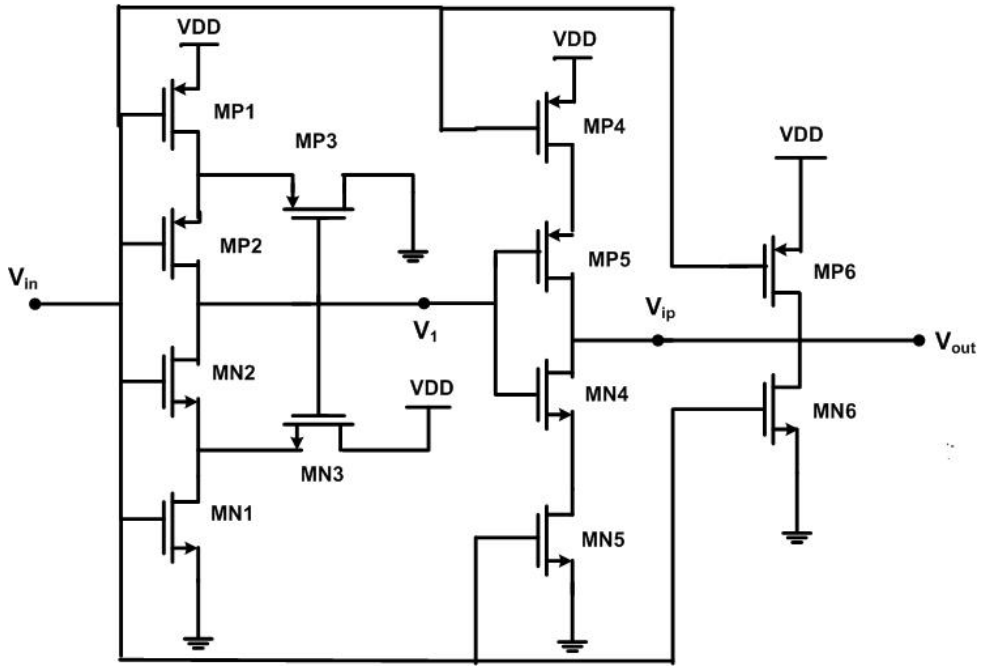


Figure 3.6: Circuit diagram of proteretic device using inverter as third stage

3.3.1.1 VTC of proteretic circuit with inverter as third stage

The VTC of the proteretic circuit is shown in Fig. 3.7, which complements the hysteretic circuit with the falling edge (red curve) at 0.8V and rising edge (green curve) at 1V. This technique gives the loop voltage as 0.2V. It also indicates the proteretic loop width (loop voltage) is shorter when compared to hysteretic loop width with this variant. This section establishes that the proteretic circuit gives an advanced response when compared to the hysteretic one and the proteretic loop is smaller than that of the hysteretic loop.

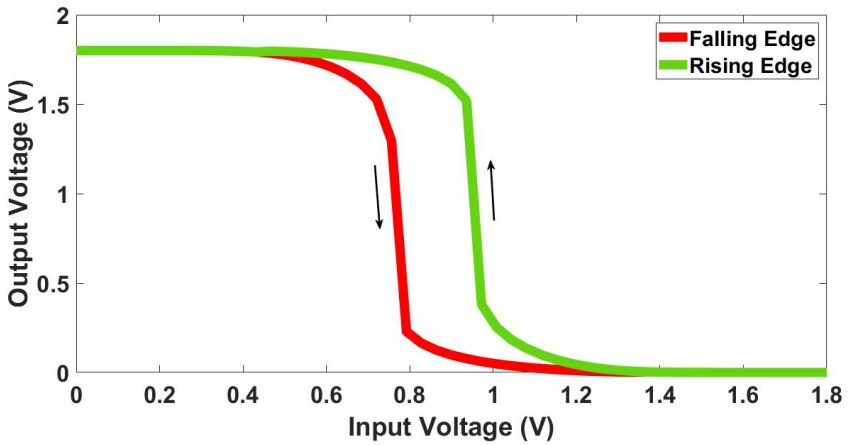


Figure 3.7: VTC of proteretic circuit with inverter as third stage

3.3.2 Proteresis using schmitt trigger as third stage

This technique uses the third stage as schmitt trigger shown in Fig. 3.8, which generates a stable proteretic output V_{out}. The detailed circuit diagram of the proteretic device using schmitt trigger is given in Fig. 3.9. The stability issue is resolved by including a final stage as schmitt trigger that maintains the output at stable 1 or 0 without allowing it to slip into a HI state.

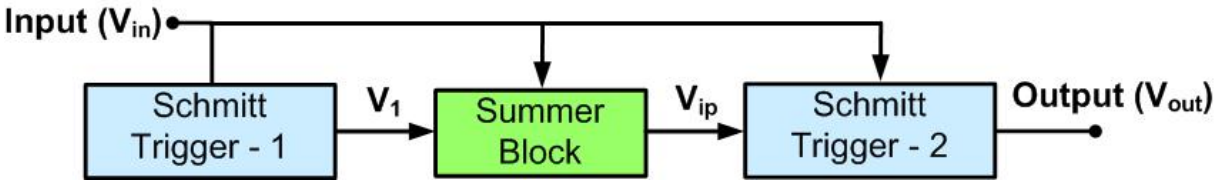


Figure 3.8: Block diagram of proteretic device using schmitt trigger as third stage

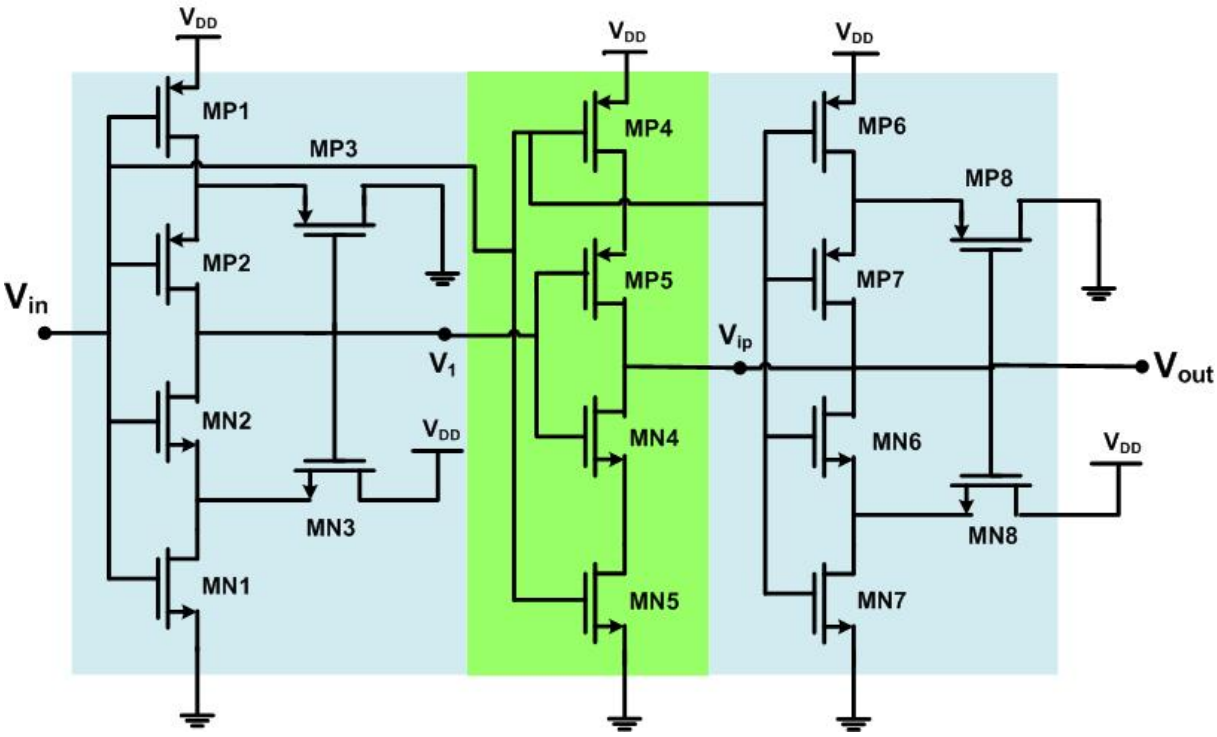


Figure 3.9: Circuit diagram of proteretic device using schmitt trigger as third stage

The third stage consists of six transistor design from MP6 – MP8 and MN6 – MN8 similar to first stage. The switching operation of the third stage schmitt trigger is as follows,

- **As V_{in} changes from 0 to V_{DD}, the observations for the range 0 < V_{in} < (V_{SD7} + V_{TP6}):** MP6 and MP7 are ON, MP8 is also ON, V_{out} = V_{DD} (HI state is shifted to V_{DD}).

- **When ($V_{SD7} + V_{TP6}$) < V_{in} < ($V_{DD} - V_{TP6}$):** MP7 is OFF, MP6 and MP8 are ON. Further, IDSP6 = IDSP8, forming a feedback path. By equating the currents and on simplification, we get the rising edge voltage (V_{R2}) as given in equation (3.8)

$$V_{R2} = \frac{V_{DD} + V_{TP6} + \sqrt{\frac{\beta_{MN7}}{2\beta_{MP8}}} V_{TN7}}{(1 + \sqrt{\frac{2\beta_{MN7}}{\beta_{MP8}}})} - \frac{\sqrt{\frac{\beta_{MN7}}{2\beta_{MP8}}}(V_{DD} - V_{TP6})}{(1 + \sqrt{K_{pm}})(1 + \sqrt{\frac{\beta_{MN7}}{\beta_{MP8}}})} \tag{3.8}$$

Where, K_{pm} = $(w/l)_{MP6}/(w/l)_{MP8}$, V_{SD7} = drain-source voltage of transistor MP7, β_n/β_p = $(\mu_n/\mu_p)[(w/l)_n/(w/l)_p]$, V_{TP6} = threshold voltage of MP6, I_{DSP6} = drain-source current of MP6, and I_{DSP8} = drain-source current of MP8.

As V_{in} changes from V_{DD} to 0, when V_{in} = V_{DD} and V_{ip} = HI, transistors MN6, MN7 and MN8 are ON, V_{out} = 0 (HI state is transferred to 0). At 0 < V_{in} < V_{TN7}, transistors MN6 and MN7, V_{out} = V_{DD}. At V_{TN7} < V_{in} < (V_{TN6} + V_{DS7}), MN7 is on and MN6 is off. Similarly, as mentioned earlier, IDSN8 = IDSN7, forming a feedback path. By equating the currents and on simplification, we get the falling edge voltage (V_{F2}) as given in equation (3.9)

$$V_{F2} = \frac{V_{DD} + V_{TP6} + \sqrt{\frac{\beta_{MN8}}{\beta_{MP8}}} V_{TN7}}{(1 + \sqrt{\frac{\beta_{MN8}}{\beta_{MP8}}})} - \frac{V_{DD} + V_{TP8}}{(1 + \sqrt{K_{nm}})(1 + \sqrt{\frac{\beta_{MN8}}{\beta_{MP8}}})} \tag{3.9}$$

Where, K_{nm} = $(w/l)_{MN7}/(w/l)_{MN8}$, V_{TN7} = threshold voltage of MN7, V_{TP8} = threshold voltage of MP8. IDSN8 = drain-source current of MN8, and IDSN7 = drain-source current of MN7. This technique generates an increased loop voltage of the proteretic device improving the noise immunity of the system.

3.3.2.1 Effect of device dimension of proteretic operation

The device dimensions play a very crucial role in the above CMOS design. For a minor variation of the transistor sizes the operation will shift from proteretic to hysteretic. Based upon the circuit conditions, the device dimensions have been carefully hand calculated for a V_{DD} = 1.8V. Table 3.5 gives the device dimensions of all transistors of the circuit design. It specifies the aspect ratios of the proteretic device, these values are substituted in equation (3.4) and (3.5), to obtain the values for rising and falling edges of the hysteresis. Further, substituting values in equation (3.8) and (3.9), the values for rising (V_{R2}) and falling edges (V_{F2}) of the proposed proteretic

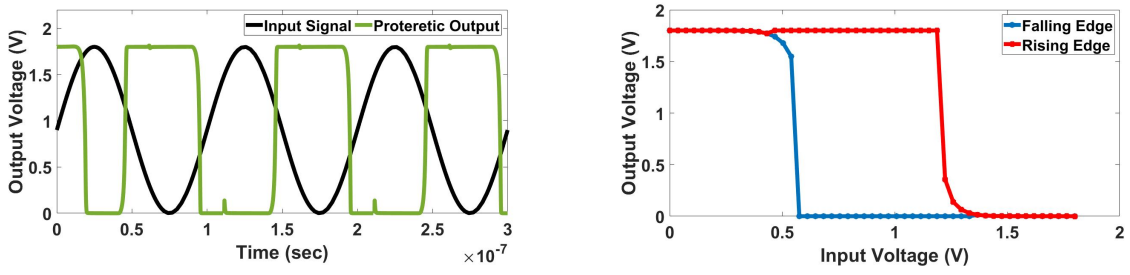
device are obtained as V_{R2} = 1.389V and V_{F2} = 0.4992V. The loop voltage is defined as the difference between the triggering voltages and is calculated as 0.8898V.

Table 3.5: Width and length (w/l) of all the transistors of proteretic device

Transistor	**Dimension (w/l)**	**Transistor**	**Dimension(w/l)**
MP1	2µ/180n	MN1	2µ/180n
MP2	10µ/180n	MN2	5µ/180n
MP3	10µ/180n	MN3	10µ/180n
MP4	20µ/180n	MN4	20µ/180n
MP5	20µ/180n	MN5	8µ/180n
MP6	2µ/180n	MN6	240n/180n
MP7	5µ/180n	MN7	2µ/180n
MP8	10µ/180n	MN8	20µ/180n

3.3.2.2 VTC of proteretic circuit with schmitt trigger as third stage

The transient analysis and VTC of the proteretic device using above transistor dimensions at 10MHz input frequency are presented in Fig. 3.10. The transient analysis shown in Fig. 3.10(a) portrays the falling edge and rising edge from the second wave onwards, as latency is seen in the first wave and proper proteretic operation as per specifications will start from the second cycle.



(a) (b)

Figure 3.10: (a) Transient response for 10MHz input and (b) VTC of proteretic device using schmitt trigger as third stage

The values of rising and falling edge of proteresis are shown in Fig. 3.10(b). The VTC shown in Fig. 3.10(b) indicates the switching of voltages of the proposed proteretic device to

be V_{F2} = 0.52V (blue curve) and V_{R2} = 1.27V (red curve) respectively. It has a loop voltage of 0.75V, which is more than first variant of proteretic device using inverter as third stage. These values are in confirmation that $V_{R2} > V_{F2}$. The design is tested for varying input frequencies from 1KHz to 10MHz and is found to be operating flawlessly over the entire range. However, beyond 10MHz, it is observed that the response starts deteriorating, this is attributed to the increased capacitance at the node V_{ip}.

The comparative analysis based on performance parameters of stable proteretic devices and schmitt trigger (ST) circuit are given in Table 3.6. It is observed that the Proteretic Device using Schmitt trigger (PDST) gives a better FOM and power consumption characteristics than Proteretic Device with inverter (PDI), however, there is an area trade-off.

Table 3.6: Performance Comparison of stable Proteretic Devices (PD)

Parameters	**ST**	**PDI**	**PDST**
Area Occupied	13µm X 5.5µm	41µm X 30µm	41µm X 35µm
Power Consumed	0.138mW	0.372mW	0.333mW
Operating Frequency Range	1kHz - 1GHz	10kHz - 10MHz	10kHz - 10MHz
Figure of Merit (FOM) at 10MHz	72.4	26.88	30.03

3.4 PVT variations of Schmitt Trigger (ST), Proteretic Device using Inverter (PDI) and Proteretic Device using Schmitt Trigger (PDST)

The process variation for SS, FF, SF, FS and TT corners are included. Also, the supply voltage (V_{DD}) is varied from 1.7 to 1.9 V and a stable output is demonstrated. Finally, the temperature variation for a range from 0 – 100 °C is plotted. All the variations are plotted with respect to voltage transfer characteristics (VTC) in the figures below.

3.4.1 PVT variations for ST Circuit

This section describes the PVT variations for schmitt trigger circuit. The Table 3.7 gives the variation of lower and upper triggering voltage of ST at different process corners. Fig. 3.11 shows the VTC of ST design with different process corners.

Table 3.7: V_L and V_H values for Different Process Corners of ST

Process Corners	**V_L(V)**	**V_H(V)**
TT	0.42	1.38
FF	0.39	1.38
FS	0.39	1.34
SF	0.42	1.38
SS	0.42	1.34

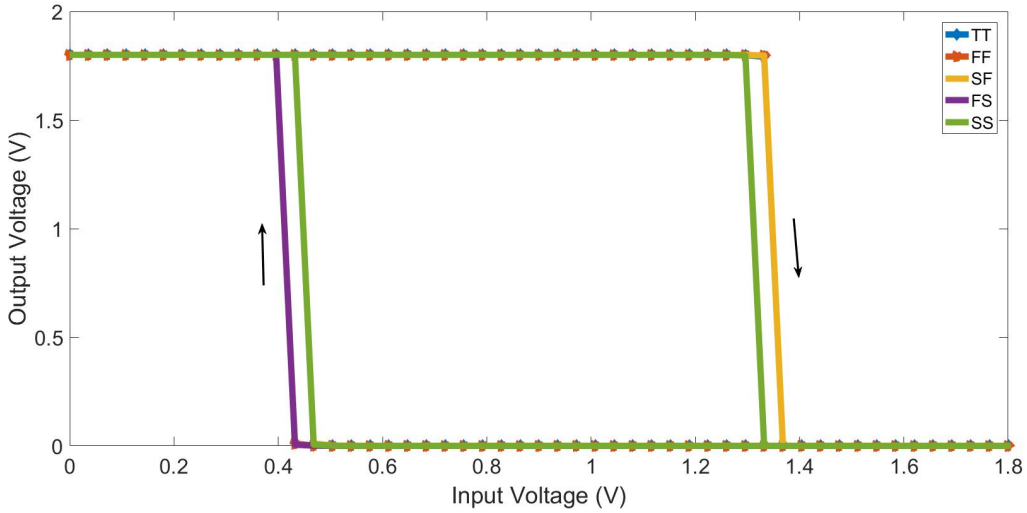


Figure 3.11: VTC variation for different process corners of ST circuit

The ST trigger design for temperature variation for lower and higher triggering voltage is noted in Table 3.8. The Fig. 3.12 gives the VTC of ST design with temperature variation from 0 – 100 °C. This shows that there is no variation in the ST triggering voltages with temperature variation.

Table 3.8: V_L and V_H for temperature variation of ST

Temperature (°C)	**V_L(V)**	**V_H(V)**
27	0.42	1.38
0	0.42	1.38
20	0.42	1.38
40	0.42	1.38
60	0.42	1.38
80	0.42	1.38
100	0.42	1.38

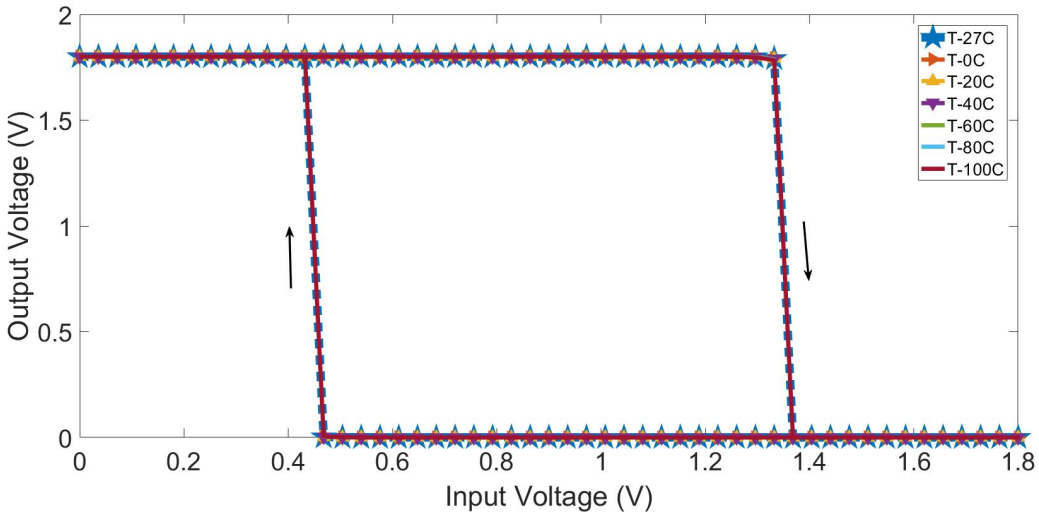


Figure 3.12: VTC variation for temperature 0 – 100 °C of ST circuit

3.4.2 PVT variations for proteretic device using inverter (PDI) Circuit

The Fig. 3.13 gives the VTC of PDI design with different process corners. The following is the Table 3.9 incorporating values of V_L and V_H of the design. The variation in process corners of PDI is 0.07V for lower triggering voltage and 0.08V for higher triggering voltage.

The Fig. 3.14 gives the VTC of PDI design with temperature variation from 0 – 100 °C. The following is the Table 3.10 incorporating values of V_L and V_H of the PDI design. This shows that there is no variation in the lower triggering voltages (V_L) and slight variation in upper triggering voltage (V_H) of maximum value 0.0423V with temperature variation of proteretic device using inverter.

Table 3.9: V_L and V_H values for Different Process Corners of PDI

Process Corners	**V_L(V)**	**V_H(V)**
TT	0.8	1
FF	0.76	1.04
FS	0.73	0.92
SF	0.88	1.08
SS	0.83	0.97

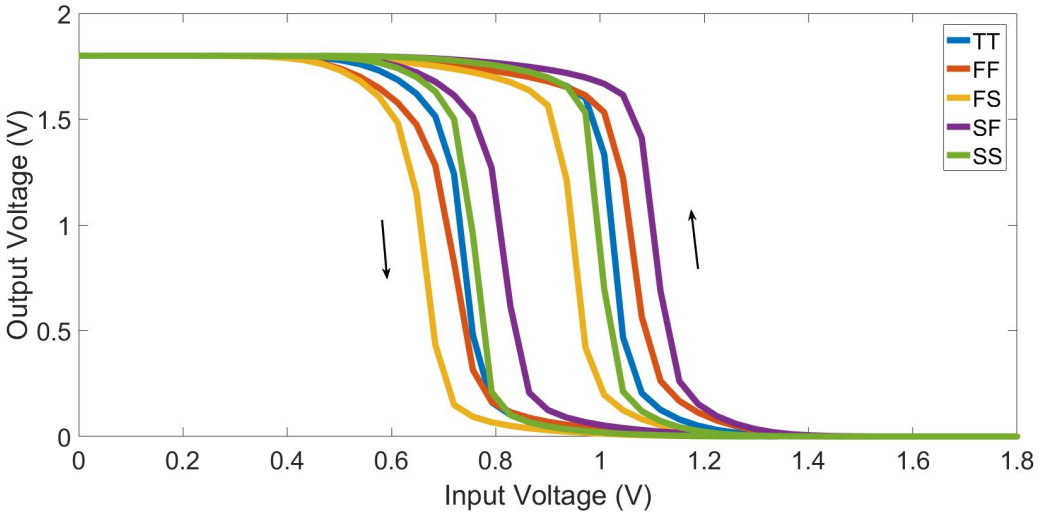


Figure 3.13: VTC variation for different process corners of PDI circuit

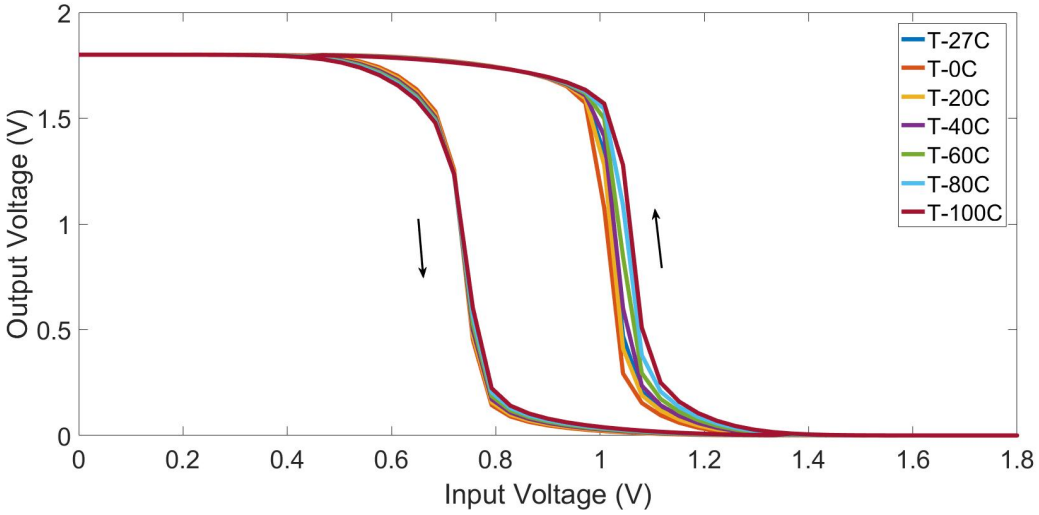


Figure 3.14: VTC variation for temperature 0 – 100 °C of PDI circuit

Table 3.10: V_L and V_H for temperature variation of PDI

Temperature (°C)	**V_L(V)**	**V_H(V)**
27	0.7	1
0	0.7	0.98
20	0.7	1.015
40	0.7	1.02
60	0.7	1.032
80	0.7	1.0423
100	0.7	1.05

The Fig. 3.15 gives the VTC of PDI design with supply voltage varying from 1.7 – 1.9V. The following is the Table 3.11 incorporating values of V_L and V_H of the design.

Table 3.11: V_L and V_H values for supply voltage variation of PDI

Supply Voltage (V)	**V_L(V)**	**V_H(V)**
1.7	0.762	0.926
1.75	0.785	0.961
1.8	0.8	1
1.85	0.821	1.033
1.9	0.834	1.075

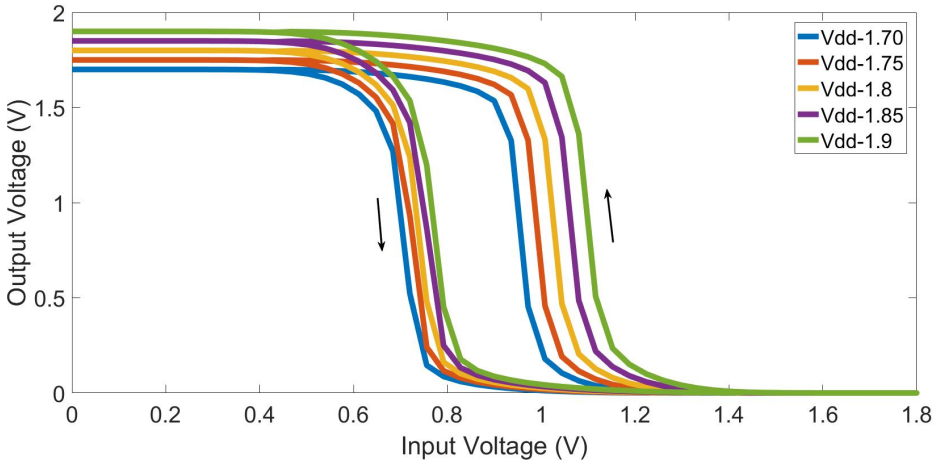


Figure 3.15: VTC variation for supply voltage 1.7 – 1.9V of PDI circuit

3.4.3 PVT variations for proteretic device using schmitt trigger (PDST) Circuit

The Fig. gives the VTC of PDST design with different process corners. The following is the Table 3.12 incorporating values of V_L and V_H of the design and the pictorial representation of VTC is shown in Fig. 3.16.This representation gives an overview that proteretic device using schmitt trigger is robust in nature.

Table 3.12: V_L and V_H values for Different Process Corners of PDST

Process Corners	**V_L(V)**	**V_H(V)**
TT	0.52	1.27
FF	0.505	1.3
FS	0.49	1.12
SF	0.605	1.31
SS	0.578	1.159

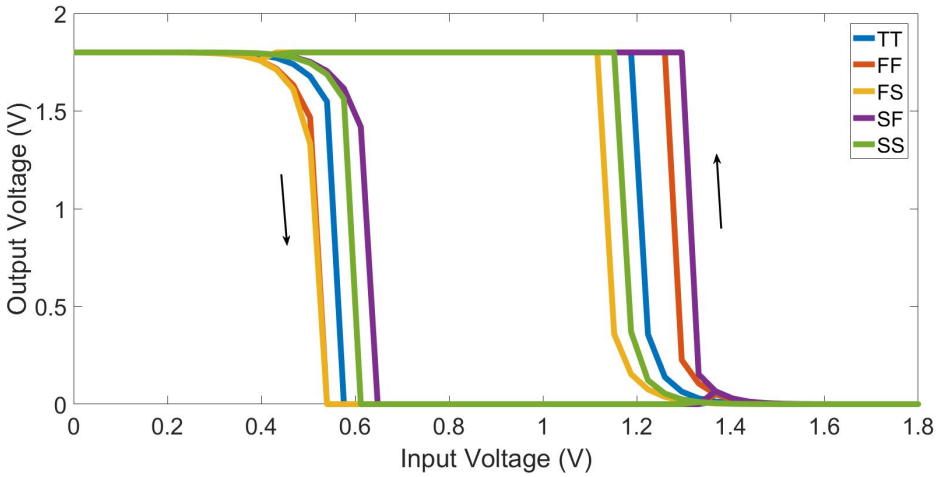


Figure 3.16: VTC variation for different process corners of PDST circuit

The Fig. 3.17 gives the VTC of PDST design with temperature variation from 0 – 100 °C. The following is the Table 3.13 incorporating values of V_L and V_H of the design.

The Fig. 3.18 gives the VTC of PDST design with supply voltage varying from 1.7 – 1.9 V. The following is the Table 3.14 incorporating values of V_L and V_H of the design.

Table 3.13: V_L and V_H for temperature variation of PDST

Temperature (°C)	**V_L(V)**	**V_H(V)**
27	0.7	1.27
0	0.7	1.2
20	0.7	1.202
40	0.7	1.27
60	0.7	1.27
80	0.7	1.29
100	0.7	1.29

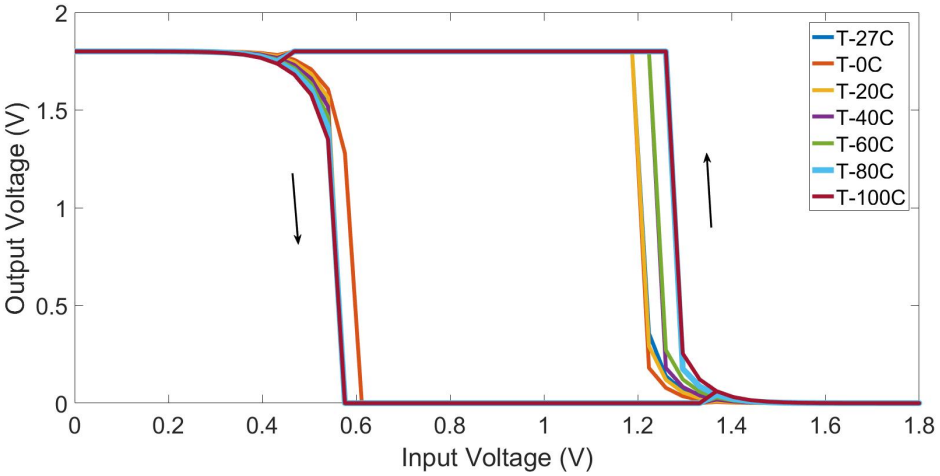


Figure 3.17: VTC variation for temperature 0 – 100 °C of PDST circuit

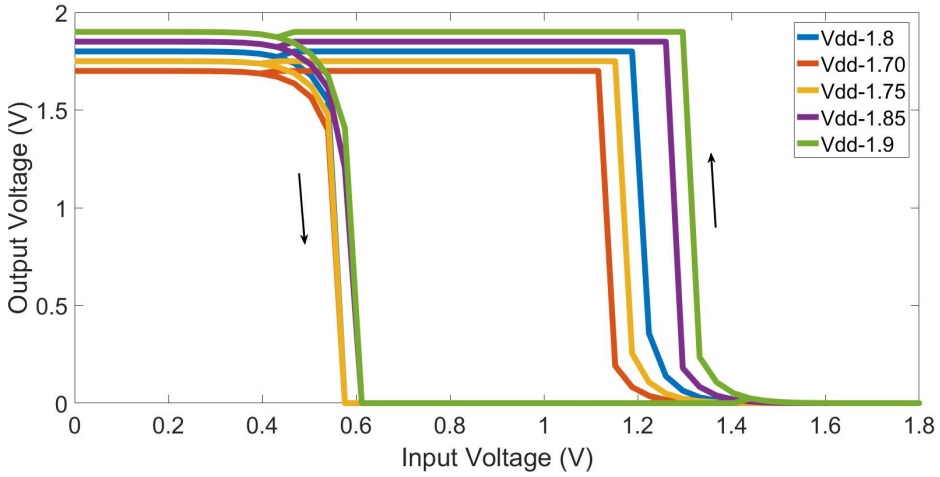


Figure 3.18: VTC variation for supply voltage 1.7 – 1.9V of PDST circuit

Table 3.14: V_L and V_H values for supply voltage variation of PDST

Supply Voltage (V)	**V_L(V)**	**V_H(V)**
1.7	0.762	1.12
1.75	0.785	1.169
1.8	0.8	1.27
1.85	0.821	1.35
1.9	0.834	1.39

3.5 Comparative performance analysis for PVT variation for ST, PDI and PDST

The Fig. 3.19 describes the comparative performance analysis of lower and higher triggering voltages of ST, PDI and PDST at different process corners. It is seen that the variation is maximum in proteretic device using schmitt trigger circuit and minimum in schmitt trigger. This randomness is further used in designing a physical Unclonable function (PUF).

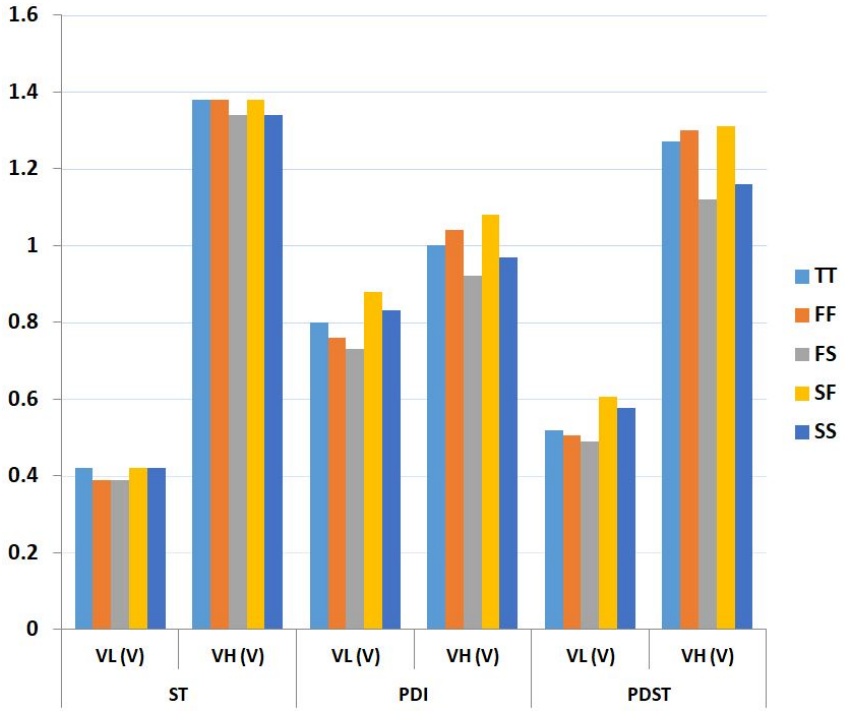


Figure 3.19: Variation of triggering voltages for ST, PDI and PDST for different process corners

The second comparison between the three devices is for temperature variation in the range

0 – 100 °C shown in Fig. 3.20. It is seen that maximum variation for PDST is of 0.077V for V_L and 0.07V for V_H.

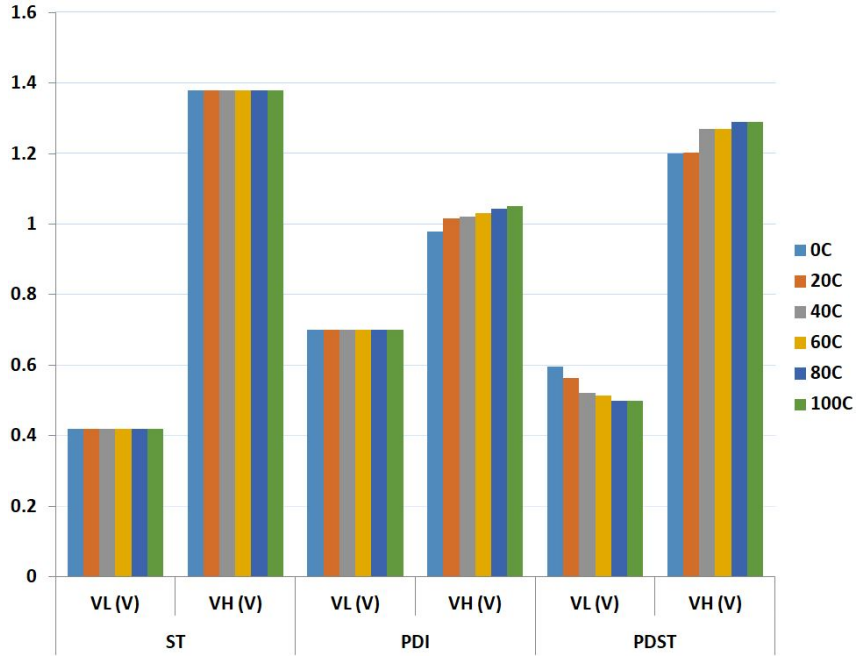


Figure 3.20: Variation of triggering voltages for ST, PDI and PDST for temperature range 0 – 100 °C

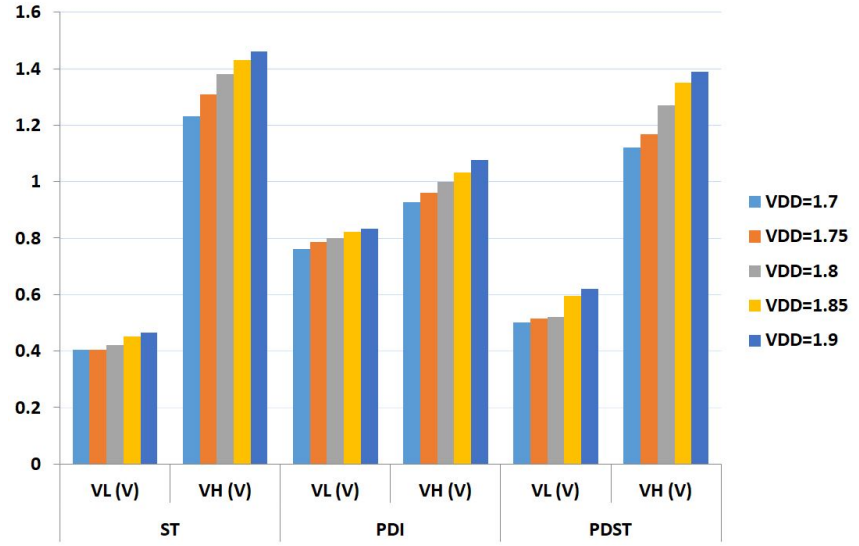


Figure 3.21: Variation of triggering voltages for ST, PDI and PDST for supply range 1.7 – 1.9V

The final comparison is for supply voltage variation from 1.7 – 1.9 V shown in Fig. 3.21 . It is seen that, as these circuits are digital in nature and gives a high or ON value as supply itself. The variation accordingly in triggering voltages are noted in the performance comparison

for all the three circuit designs.

3.6 Variation of the function (V_H-V_L) for Schmitt trigger and proteretic circuits

The variation discussed in this section is based on lower and higher triggering voltages of the circuits and its effect depending on power consumption and supply voltage.

3.6.1 Power consumption of ST, PDI and PDST with respect to the function (V_H-V_L)

The function of (V_H-V_L) is given as ΔV, and the variation of the difference for ST, PDI and PDST with respect to power consumption is given in the table 3.15. The difference function is the loop voltage generated with the difference in triggering voltages. The increase in loop voltage is experienced as increasing the (W/L) of the transistors in the circuit which leads to increase in current flow through the circuit leading to more power consumption. It is observed from the table that as the value of function increases the power consumed is also increasing for all the 3 designs.

Table 3.15: ΔV with Power consumption of ST, PDI and PDST

ST		PDI		PDST	
ΔV(V)	**Power Consumed (μW)**	**ΔV(V)**	**Power Consumed (μW)**	**ΔV(V)**	**Power Consumed (μW)**
0.92	88.22	0.14	232.45	0.581	215.8
0.95	96.15	0.19	304.7	0.63	285.9
0.96	138.41	0.2	372.4	0.705	333.6
0.97	197.2	0.24	381.9	0.75	374.9
0.99	216.6	0.28	435.7	0.795	405.4

3.6.2 Supply Voltage Variation of ST, PDI and PDST with respect to the function (V_H-V_L)

The function of (V_H-V_L) is given by (ΔV) with supply voltage of ST, PDI and PDST is shown in the Fig. 3.22. The supply voltage is varied from 1.7 – 1.9 V. It is seen that, as these circuits are digital in nature and gives a high or ON value as supply itself. The variation accordingly in loop voltage (ΔV) is noted in the performance comparison for all the three circuit designs. Further, the operating window of the supply voltage for schmitt trigger is in the range 0.8 – 2.2 V, whereas for proteretic devices the range is 1.4 – 2.2 V.

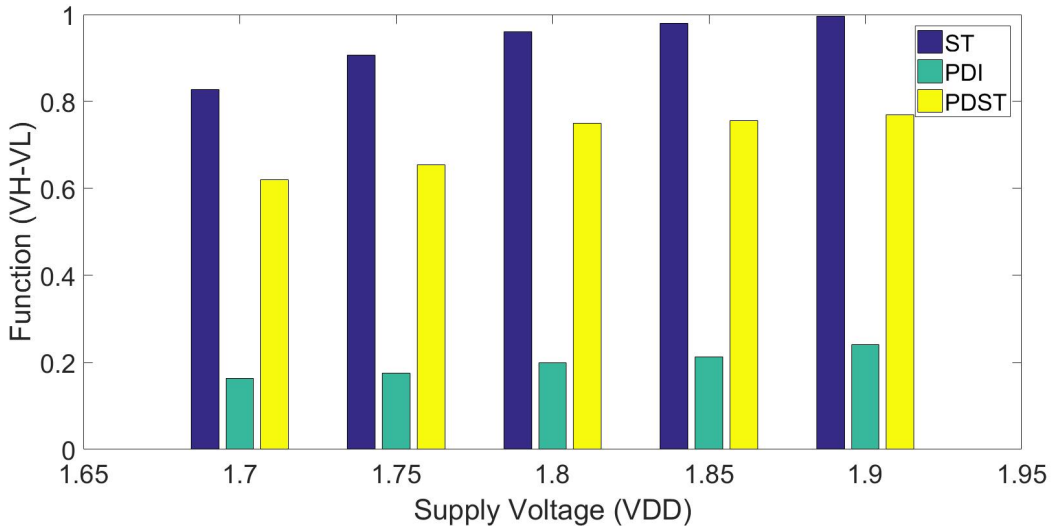


Figure 3.22: Supply Voltage variation in the range 1.7 – 1.9 V Vs Function (V_H – V_L) for ST, PDI and PDST.

Hysteresis is experienced in the normal operation of schmitt trigger in a range starting from frequency 10kHz – 1GHz (as noted), whereas, for proteresis output few conditions has been levied on the schmitt trigger (as it is used in the proteretic circuit as stage 1) to generate proteresis output. This proteretic output is maintained in the range of operating frequency from 10KHz – 10MHz. After this range it gives hysteresis output by default for the proteretic circuit. This is due to the variation of triggering voltage range used in stage 1 i.e. schmitt trigger in proteretic circuit.

In this chapter the design of both hysteretic and proteretic devices in CMOS TSMC 180nm technology is demonstrated. A complete mathematical modelling of the design equations is

presented and the same is utilised to achieve the aspect ratios of the transistors. The design of proteretic device in two different approaches and simulation results are presented. The simulation results indicate stable operation of proteretic device up to a frequency of 10MHz. Further, the PVT variations of ST, PDI and PDST is done with the comparative analysis of all the three forms of variations.

Chapter 4

Ramp Generator Design - A System Level Comparative Analysis of Hysteretic and Proteretic Device Performance

This chapter deals with the design of a CMOS ramp generator circuit which is commonly used in switching power supplies, analog to digital converters, CMOS image sensors and others. The main objective of this design is to demonstrate a system design using a comparator with hysteretic characteristics and then with proteretic characteristics and illustrating a comparative analysis between the performance of the two circuits. It is desired to establish the fact that every system where hysteretic devices are used can also be designed using the proposed proteretic device and the resultant performance improvement in terms of speed of the circuit, can be established. This opens a gateway to high-speed circuit design for all conventional systems currently based on hysteresis.

4.1 Introduction to ramp generator

Ramp generators are widely used in various applications like switching power supply, analog to digital converters [8], CMOS Image sensors [64], and others. It has been observed that the operational speed of the overall system is restricted by the frequency of the ramp generator and various techniques have been proposed to speed up the system design [5]. A critical component of the ramp generator is the comparator circuit which is primarily a schmitt trigger based circuit

with hysteretic properties [9]. While efforts have been made to speed up this circuit by various methodologies, this chapter proposes the approach of replacing a hysteretic comparator with a proteretic comparator. This is the first attempt to design a ramp generator using proteretic comparator. Further, other forms of ramp generator circuit are placed in the following section.

4.2 Other forms of Ramp Generator Circuit

This section describes different types of ramp generators and its working. These circuit designs are based on various techniques generating ramp signals using switched capacitors, ADC's and resistor-ladder topology.

4.2.1 Fully differential switched-capacitor ramp generator

A BIST circuit is designed to test the linearity of pipeline ADC. The proposed ramp generator is implemented using switched capacitor circuits in the fully differential mode. The key aspect of the design is that step size of ramp signal is controlled such that it is equivalent to the least significant bit of the ADC under test. The step size and width are designed at such small values that it gives an impression of a ramp waveform [65].

4.2.2 Ramp Generator for Single-Slope Look Ahead Ramp (SSLAR) ADC

A column-parallel CMOS Image sensors have a crucial component of an ADC which is characterized as SSLR ADC. The design allows a wide range of output voltage and is implemented using switched capacitor circuits in 0.5 micron CMOS technology [66].

4.2.3 Ramp Generator using resistor-ladder for CMOS Image Sensor with a Column-Level Multiple-Ramp Single-Slope ADC

The key feature of this ramp generator is that instead of generating a single ramp waveform, it generates multiple waveforms but all are of the same slope. This ramp generator is used in

design of multiple-ramp single-slope ADC in a CMOS image sensor. While power consumption increases by 24%, this circuit is able to achieve an increase of frame rate by 2.8x. It is implemented in 0.25 micron CMOS technology [67].

4.2.4 Very Linear Ramp-Generators for High Resolution ADC BIST and Calibration

This paper implements a slow-slope ramp generator for which a large capacitor is charged through a small DC current. This ramp generator is used in the test a high-resolution (12 bit) ADC and calibrate the same [68].

4.3 Design of ramp generator circuit using operational amplifier

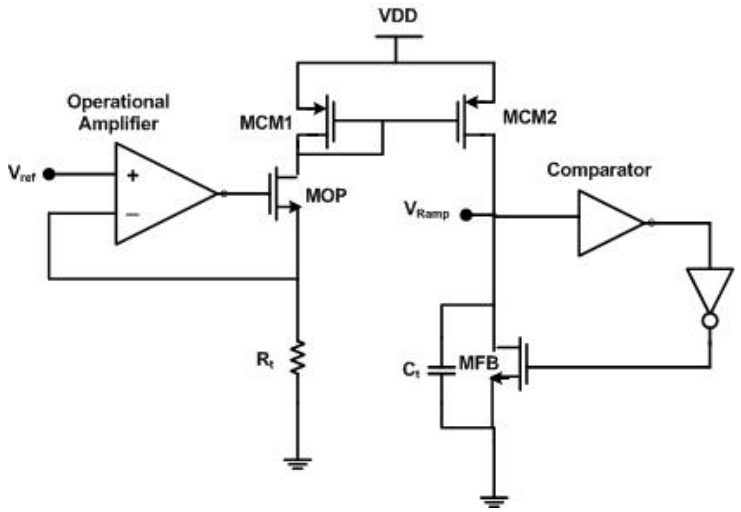


Figure 4.1: Ramp generator circuit [9]

The ramp generator circuit shown in Fig. 4.1 consists of an operation amplifier driving an NMOS transistor MOP of the current mirror circuit in which the transistor MFB and capacitor C**t** play a vital role in ramp signal generation. The ramp signal is generated by the charging and discharging of the capacitor, controlled by the switching of transistor MFB, which is in turn controlled by the comparator output.

Thus, it is seen that comparator performance determines the speed of the ramp generator. The transistor MFB is turned ON and OFF based on the output of the comparator, which compares the ramp voltage at its input to its internal pre-set threshold voltages (V**H** and V**L**) based on transistor dimensions and ultimately generates a square wave. The frequency of the ramp wave is determined by equation (4.1) given below.

$$f = \frac{V_{ref}}{R_t C_t (V_H - V_L)} \tag{4.1}$$

Where, V**ref** is the reference voltage given to the operational amplifier. R_t and C_t are the resistor and capacitor and V_L and V_H are lower and higher triggering voltages of the comparator. It is evident from the above equation that the difference between the triggering voltages is inversely proportional to ramp signal frequency.

4.3.1 Operational amplifier design for ramp generator

The operational amplifier used in the design of ramp generator is shown in Fig. 4.2. It consists of five PMOS transistors (T_1 - T_5) and three NMOS transistors (T_6 - T_8), with current source (I_R) and compensating capacitor C_c. The non-inverting input is given by reference voltage (V_{ref}) of the ramp generator circuit. The supply voltage given to the circuit is V_{DD} with inputs V_{IN1} and V_{IN2} generating output V_{OA}.

4.4 Ramp generator using hysteretic comparator

The operation of the ramp generator using the hysteretic Schmitt trigger circuit is shown in Fig. 4.3. Initially, the transistor MFB is presumed OFF and the capacitor C_t is charging. Due to this, the voltage V_{Ramp} gradually increases. As long as V_{Ramp} is small than the voltage required to switch ON both NMOS transistors MN1 and MN2 are off and both PMOS transistors MP1 and MP2 are ON and the output V_{HYS} is V_{DD} . This output of the comparator is inverted by not gate, and a logic 0 is present at the input of switching transistor MFB. The capacitor C_t continues to charge and V_{Ramp} gradually increases. As the voltage V_{Ramp} increases and crosses the switching threshold of the Schmitt trigger, both MN1 and MN2 will turn on, and

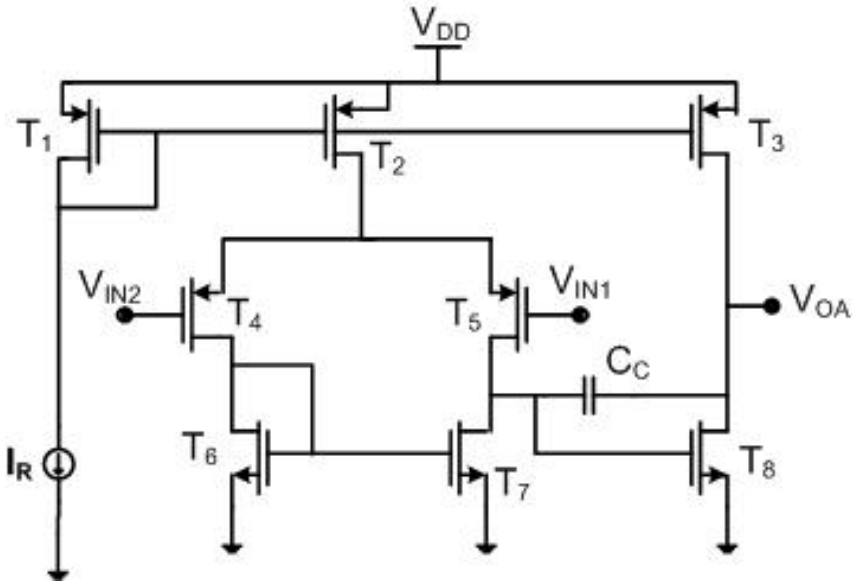


Figure 4.2: Operational amplifier circuit

output V_{HYS} will be pulled down to 0V. It causes the voltage at the input of MFB to switch to logic 1, and the transistor is turned ON. It leads to the quick discharge of capacitor C_t and the ramp voltage V_{Ramp} starts decreasing. On its way back, as V_{Ramp} crosses the lower switching threshold, the entire circuit returns to its initial operation and generates the next cycle.

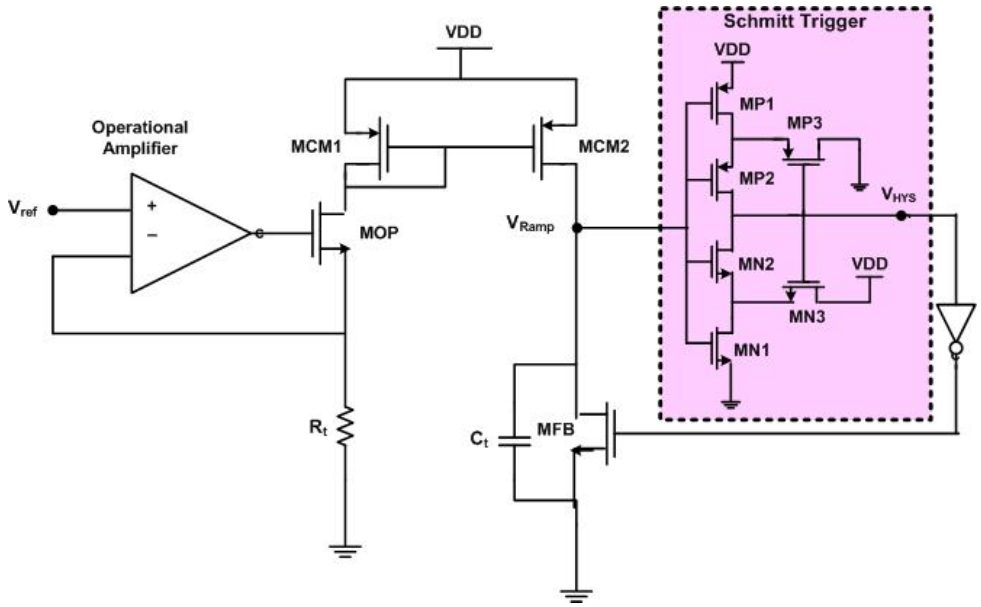


Figure 4.3: Ramp generator using schmitt trigger (Hysteretic) Circuit

The values of the load capacitor and resistor of the ramp generator using hysteretic comparator is given in Table 4.1. The loop voltage of the schmitt trigger circuit is considered from the previous chapter. The values when substituted in equation 4.1 generates a frequency of ramp

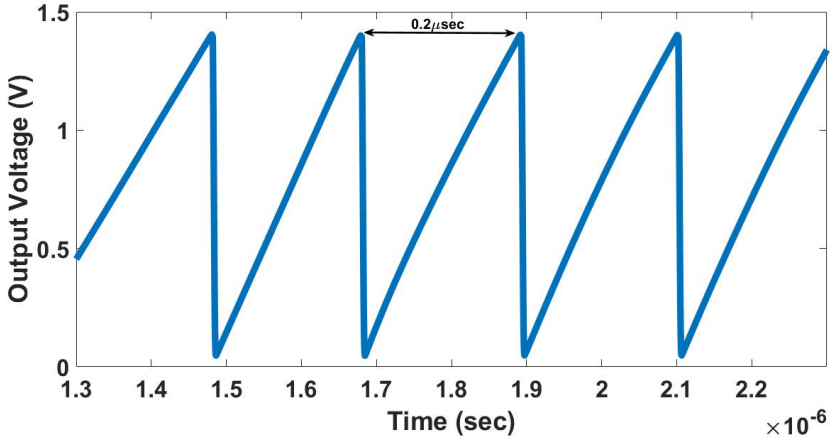


Figure 4.4: Ramp signal at Frequency of 5MHz as Output of hysteretic ramp generator

signal around 5MHz. Further, this is simulated on TSMC 180nm CMOS process to generate output of the ramp generator using a Schmitt trigger circuit is as shown in Fig. 4.4, where a ramp signal swing of 0 to 1.4V is observed and the time period of ramp wave is 0.2µsec, indicating a ramp signal frequency of 5MHz, which is close to the calculated value.

4.5 Ramp generator using proteretic comparator

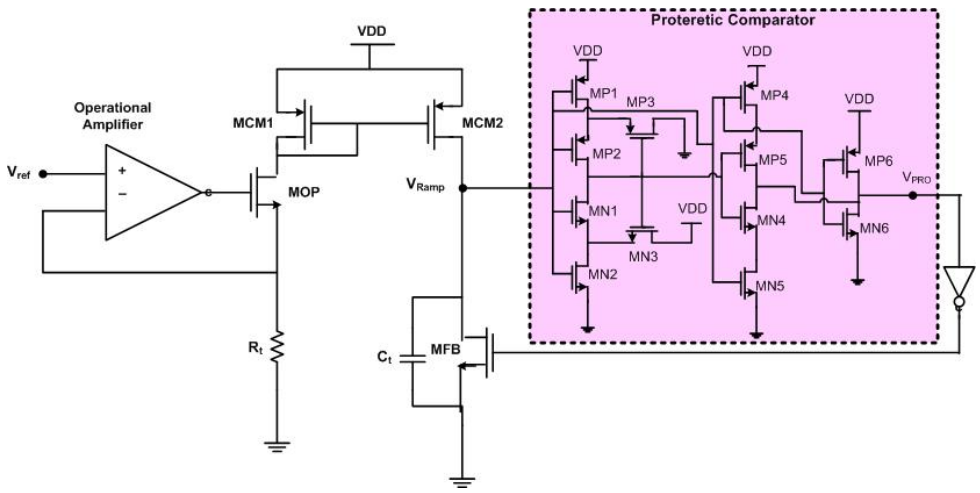


Figure 4.5: Ramp generator using proteretic circuit

In this design the hysteretic comparator in ramp generator is replaced with a proteretic circuit designed in chapter 3 as shown in Fig. 4.5. The area of the comparator is increased by using 12 transistors in the proteretic circuit instead of 6 transistors, as in the hysteretic circuit.

The ramp generator's overall operation is similar to the case of the hysteretic ramp generator, except that V_{PRO} drives MFB instead of V_{Hys}. However, a fast switching proteretic comparator with a small proteretic loop is an ideal replacement for the hysteretic circuit in applications where speed is of essence.

The theoretical value of frequency of the ramp generator using proteretic comparator is calculated considering the values given in Table. 4.1. The loop voltage of the proteretic circuit is taken as 0.2V (from the previous chapter, considering third stage as inverter). The values when substituted in equation (4.1) generates a frequency of ramp signal around 6.25MHz, this is occurring at a trade-off in terms of the circuit area and power consumption.

Table 4.1: Parameter values of ramp generator circuit

Parameter	**Value**
MOP, MCM1, MCM2, MFB	2μm/180nm
V_{ref}	0.5V
C_t	5pf
R_t	80Kohms

The layout of the ramp generator with a proteretic circuit is shown in Fig. 4.6. The area occupied is 47µm X 52µm, which is slightly greater than the area occupied by hysteretic comparator 47µm X 43µm due to six more transistors used in the proteretic circuit.

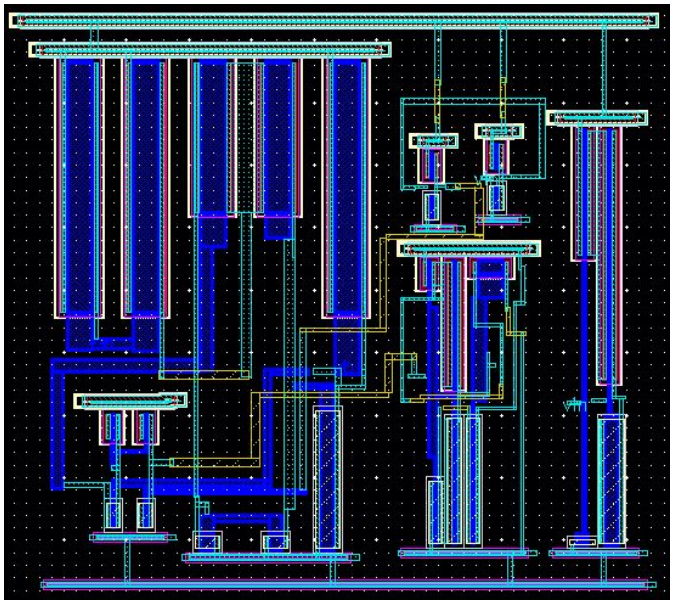


Figure 4.6: Layout of ramp generator using proteretic comparator

Further, the post layout simulation results on TSMC 180nm CMOS process to generate output of the ramp generator using a proteretic comparator is as shown in Fig. 4.7. The speeding up effect is evident in Fig. 4.7, wherein a ramp signal of frequency 6.25MHz is seen. This work establishes that without making significant changes in the overall system and replacing the hysteretic circuit with a proteretic circuit, frequency of the ramp signal is improved from 5MHz to 6.25MHz.

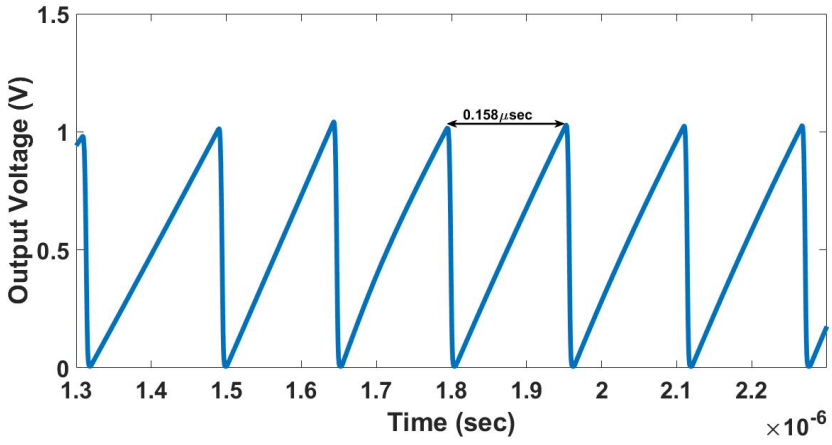


Figure 4.7: Ramp signal output of proteretic device at 6.25MHz

Fig. 4.8 demonstrates the ramp output of the proteretic ramp generator for a temperature range of 0°C to 80°C, indicating that the design is robust over the said temperature range.

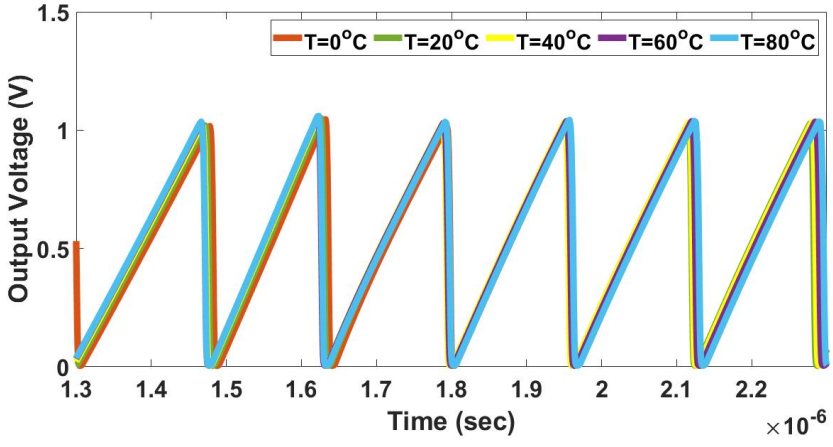


Figure 4.8: Ramp signal output of proteretic device for a temperature range of 0°C to 80°C

4.6 Comparative analysis of hysteretic and proteretic ramp generator

The simulation is performed on layout extracted design in TSMC 180nm CMOS process for a ramp generator using both hysteretic and proteretic devices with a supply voltage of V_{DD} = 1.8V. The early transition in proteresis has an accelerating effect on circuit performance and it leads to the improvement in frequency of the ramp generator.

Table 4.2: DC power consumed by ramp generators using ST and PDI

Sub-blocks	**DC Power (ST) [mW]**	**DC Power (PDI) [mW]**
Operational Amplifier	0.0764	0.0764
Inverter	0.002627	0.002627
ST/PDI	**0.1125**	**0.374**
Current Mirror	0.0214	0.0214
M_{op}	0.0088	0.0088
M_{FB}	0.0103	0.0103
Resistor	0.006225	0.006225
Total Power	**0.238**	**0.499**

The DC power consumed by the ramp generators using hysteretic and proteretic devices block wise are given in table 4.2. The varying factor is seen in ST/PDI. The Fig. 4.9 and 4.10 shows the consumed power percentage of each ramp generator by different blocks using schmitt trigger and proteretic device respectively. It is noted that maximum power consumption in ramp generator is through hysteretic or proteretic comparators, where 47% for ST based and 75% for proteretic based ramp generators. The comparison of hysteretic and proteretic ramp generators designed in this work is given in Table 4.3.

It is seen that the speed of the proteretic ramp generator is 25% more than the hysteretic. To consolidate the claim of performance improvement using proteretic and its trade-off, an attempt to analyze the circuit by increasing the size of the transistors in the hysteretic ramp generator, such that they become equal to the size of proteretic implementation is made and the following results are observed.

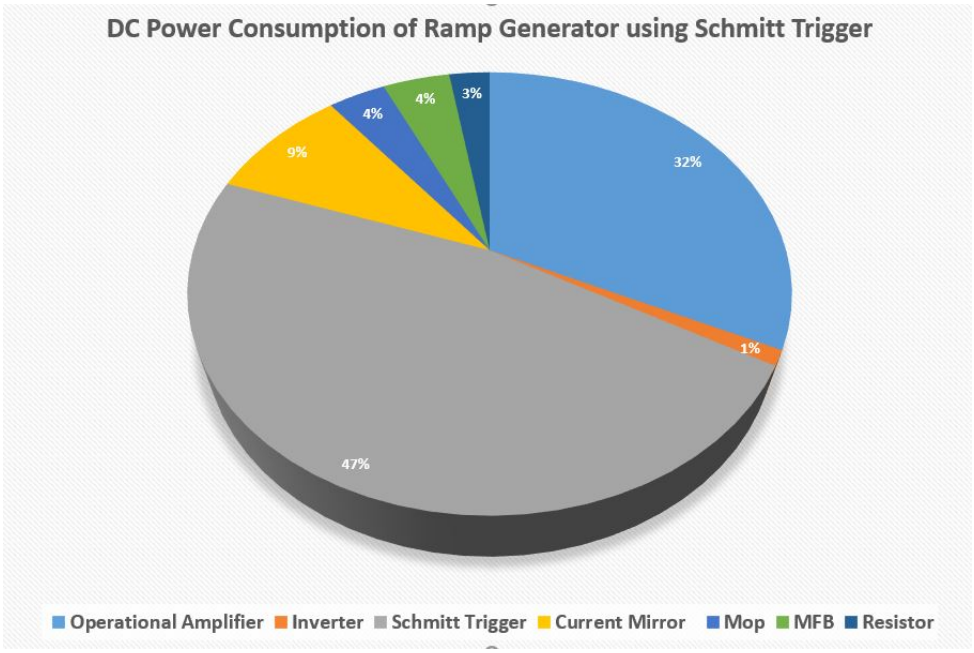


Figure 4.9: DC Power Consumption of Ramp Generator Using ST

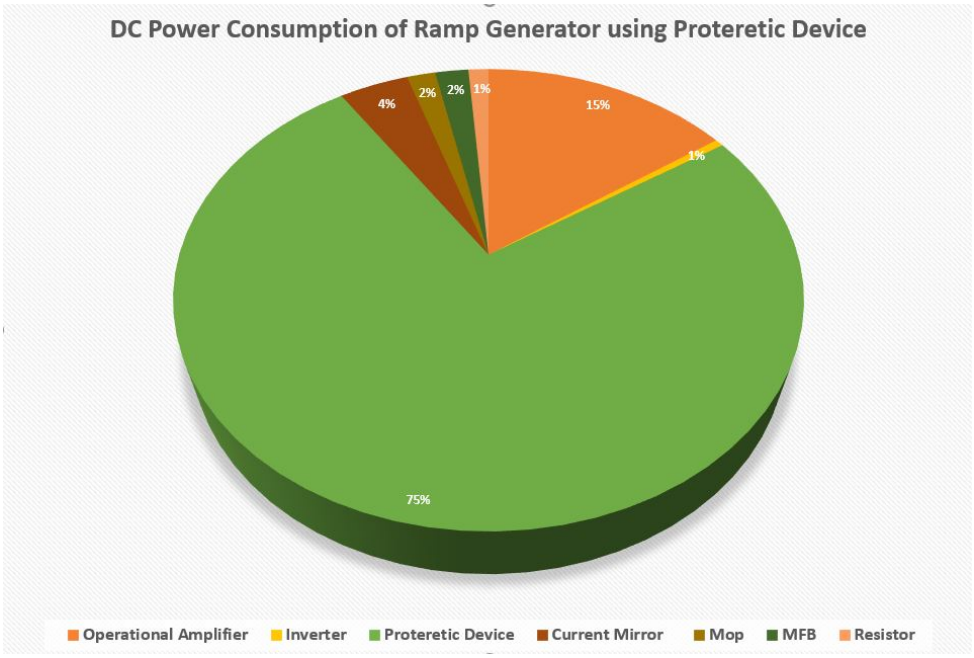


Figure 4.10: DC Power Consumption of Ramp Generator Using PDI

i. The two transistors of hysteretic comparator that affect design performance are MP1 and MN1 as seen in Fig. 4.3, these transistors decide the upper and lower triggering points of the VTC and hence the loop width. It is observed that the hysteretic comparator frequency increases from current value of 5MHz to 5.88MHz when size of MP1 and MN1 is increased by four times the current size. At this instant, the area of the hysteretic ramp generator becomes

Table 4.3: Comparison of hysteretic and proteretic ramp generator

Parameter	**Hysteretic Ramp Generator**	**Proteretic Ramp Generator**
Ramp Frequency	5MHz	6.25MHz
Power Consumed	238µW	499µW
Area Occupied	47µm X 43µm	47µm X 52µm

equal to the proposed proteretic ramp generator area of 47µm X 52µm.

ii. When the hysteretic transistor size is further increased to 5.5 times the current value, a ramp generator frequency of 6.25MHz is achieved. Clearly, the area of hysteretic is now greater than the proteretic design and power consumption has also increased to 1.741mW. However, when the size of MFB transistor was increased by 2x, 3x and 5x times the frequency of both hysteretic and proteretic ramp generators is reduced. Hence, indicating that the size of MFB transistor does not have a linear bearing on the overall operation of the ramp generator.

iii. The normalized Figure of merit (FOM) given in equation (4.2) is calculated at the same operating frequency of 6.25MHz for both circuits.

$$FOM(normalized) = Frequency/Power \tag{4.2}$$

FOM for proteretic ramp generator = 6.25MHz / 0.499mW = 12.52 and FOM for hysteretic ramp generator = 6.25MHz / 1.741mW = 3.58. Therefore, we get a 3x improvement in FOM in proteretic when compared to hysteretic ramp generator at same operating frequency.

The supply range window of operation for ramp generators using hysteretic and proteretic circuits lies on the similar ranges as per the working of ST which is in the range 0.8 – 2.2V and for PDI for the range 1.4 – 2.2V. The working of the ramp generators using both devices are based on those ranges.

4.7 Comparison of the proposed ramp generator circuits with other state-of-the-art designs

This section describes the comparison of proposed ramp generators using both hysteresis and proteresis with the state-of-the-art designs, which is shown in table 4.4. This gives a better FOM with a trade-off in area and power for ramp generator with proteresis.

Table 4.4: Comparison of the proposed Ramp Generator Circuits with the existing state-of-the-art circuits

Parameter	**[65]**	**[66]**	**[68]**	**RG with Hysteresis**	**RG with Proteresis**
Area Occupied (mm^2)	0.1	2.5	0.1089	0.002021	0.0024444
Power Consumed (mW)	-	8	0.1	1.741*	0.499
Ramp Frequency (MHz)	0.2	20	1-10 KHz	6.25	6.25
Normalized FOM (MHz/mW)	-	2.5	-	3.58	12.52

*Power Consumed at 6.25MHz frequency

This chapter presents the implementation of a proteretic ramp generator and its detailed performance analysis. As this paper is the first of its kind that proposes a ramp generator based on proteresis, a comparison with the other state of art is not possible. The current design occupies an area of 47µm x 52µm generating a frequency of 6.25MHz with a power consumption of 499µW. It is established that the proteretic comparator has better frequency response and FOM than the hysteretic comparator based ramp generator. Hence, the use of proteretic comparators can be explored for designing high speed CMOS circuits in place of traditionally used hysteretic comparators.

Chapter 5

Design and Implementation of Proteresis - Hysteresis (ProHys) Switch

A proteretic device is supposed to speed up the system without losing the benefit of noise immunity as discussed in previous chapter in the design of ramp generator. Hysteretic and proteretic devices are bi-stable and their interstate switching depends on triggering voltages. The devices proposed in the literature can be clearly classified to work either as hysteretic or proteretic. This is the first attempt to design a circuit that switches between two opposite characteristics of hysteresis and proteresis exhibiting both techniques. The application for ProHys switch is in the design of Physical Unclonable Functions (PUF).

5.1 Design methodology of ProHys (proteresis-hysteresis) switch

Hysteresis is a naturally occurring phenomenon in umpteen situations, whereas proteresis is a rarely occurring one. However, both have their pros and cons, and it aims to design a circuit that can work in both hysteresis and proteresis mode and is named the ProHys switch with its block diagram seen in Fig. 5.1. The design comprises of three main blocks, Schmitt trigger block, adder block, and switch block. All three blocks are fed by the input signal (Vin), and the control input (V_{ctrl}) is given to the control circuit of the switch block. If V_{ctrl} is low, the circuit operates in proteretic mode, and if V_{ctrl} is high, the circuit operates in hysteretic mode.

The design comprises of three main blocks, Schmitt trigger block, adder or a combiner block, and switch block. The detailed circuit diagram of each block is given in Fig. 5.2. The

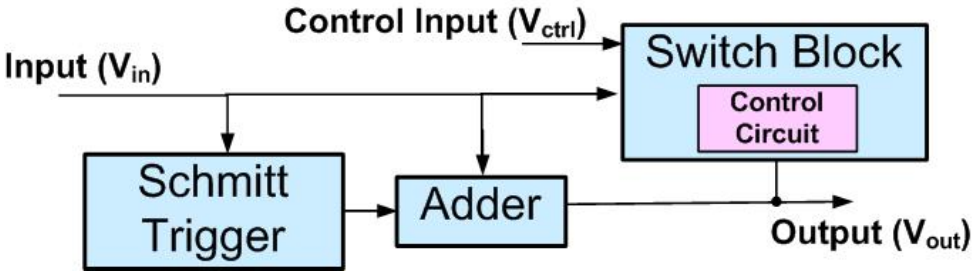


Figure 5.1: Block diagram of ProHys switch

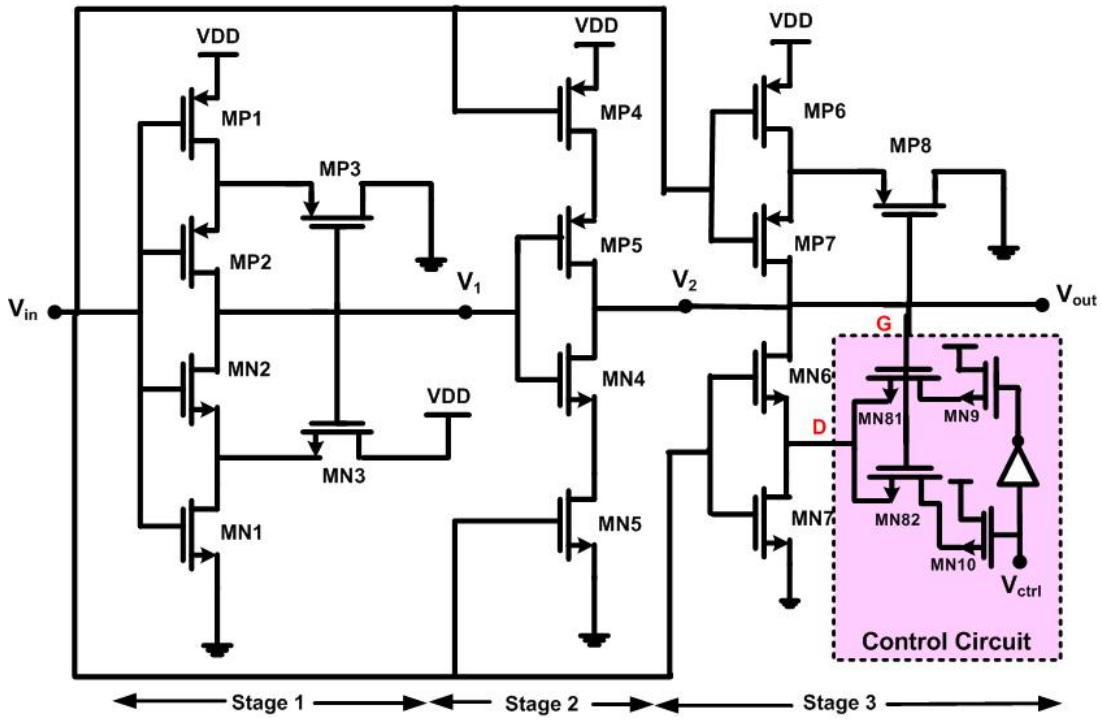


Figure 5.2: Transistor level implementation of complete ProHys circuit

proposed ProHys switch has first two stages as schmitt trigger circuit and an adder as discussed in detail in chapter 3. The ouput of the first stage is V_1 and the intermediate proteresis output of the second stage is given as V_2. The third stage of Fig. 5.2 is a switch block with a control circuit generating the final proteretic response V_{out}.

5.2 Switching operation of the proposed ProHys block

It is evident that the switch block is loosely based on Schmitt trigger, wherein the PMOS transistor influences the rising edge. The falling edge is dependent on the NMOS transistor circuit in general and the control circuit in specific as seen in Fig. 5.3(a). The position of rising edge

depends on MP8 and it is fixed. However, the position of falling edge depends on either MN81 and MN82. If the current flows through MN82 the falling edge is delayed and leads to hysteresis and if current flows through MN81, falling edge is advanced and leads to proteresis. The V_{ctrl} signal will switch ON MN9 or MN10 based on the selected mode of operation.

When V_{ctrl} is high, the transistors MN10 and MN82 are in saturation and provide a path for the current to flow and discharge the point G, as seen in Fig. 5.3(b). When V_{ctrl} is low, the transistors MN9 and MN81 are in saturation and provide a discharge path, as seen in Fig. 5.3(c). The dimension of MN81 and MN82 is such that the current flowing can be controlled and in-turn affects the positioning of the falling edge at an early point in proteresis or a later point in hysteresis.

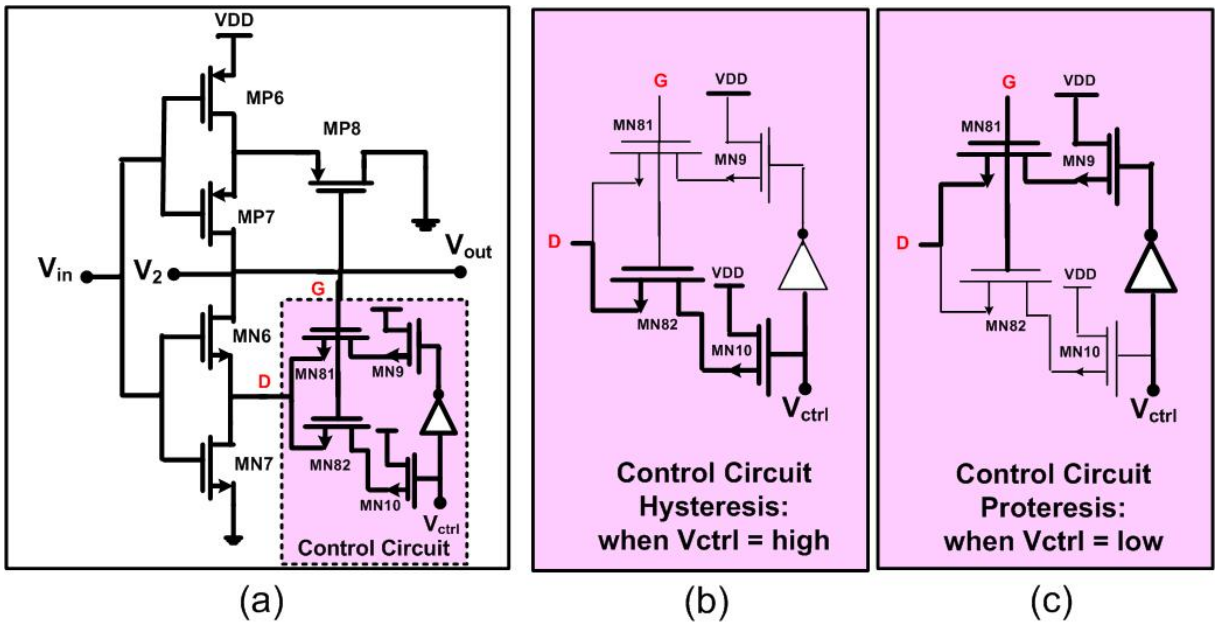


Figure 5.3: (a) Switch block with control circuit, (b) Hysteresis operation using control circuit, and (c) Proteresis operation using control circuit

Earlier techniques involved using an inverter circuit at the output of stage 2 in a feedback loop to stabilize the output [36]. The proposed circuit describes a novel output stage comprising of three PMOS (MP6, MP7, MP8) and six NMOS transistors (MN6, MN7, MN81, MN82, MN9, MN10). It is understood that V_2 is shorted to V_{out}, but the PMOS (MP6, MP7, MP8) will work in a feedback loop to pull V_{out} to V_{DD} (i.e., rising edge) when it is in HI state, and the NMOS circuit (MN6, MN7, MN81, MN82, MN9, MN10) will act as a feedback loop to pull down the output to zero (i.e., falling edge) when it is in HI state. More specifically, the operation of MN81 and MN82 is decided by transistors MN9, MN10, and V_{ctrl}.

5.2.1 Derivation of falling and rising edge of the ProHys switch

This section derives the equations for rising and falling edges in both hysteretic and proteretic modes of operation considering the device dimensions and the control input signal.

5.2.1.1 Case 1: PMOS network is conducting and NMOS network is OFF

At V_{in} = 0 and V_2 = HI, MP8 is ON (in saturation). V_{in} changes from 0 to V_{DD}, the following observations are made.

• When $0 \leq V_{in} \leq (V_{SD7} + V_{TP6})$: MP7 and MP6 are ON, MP8 is also ON, $V_{out} = V_{DD}$ (HI state is shifted to V_{DD}).

• When $(V_{SD7} + V_{TP6}) \leq V_{in} \leq (V_{DD} - V_{TP6})$: MP7 is OFF, MP6 and MP8 are ON. $I_{DSP6} = I_{DSP8}$, forming a feedback path. By equating the currents and on simplification, we get the rising edge voltage (V_{RE}) as given in equation (5.1),

$$V_{RE} = \frac{V_{DD} + V_{TP6} + \sqrt{\frac{\beta_{n7}}{2\beta_{p8}}} V_{TN7}}{(1 + \sqrt{\frac{2\beta_{n7}}{\beta_{p8}}})} + \frac{\sqrt{\frac{\beta_{n7}}{2\beta_{p8}}}(V_{DD} - V_{TP6})}{(1 + \sqrt{K_p})(1 + \sqrt{\frac{\beta_{n7}}{\beta_{p8}}})} \tag{5.1}$$

Where, K_p = ((WP6/LP6)/(WP8/LP8)), V_{SD7} = drain-source voltage of transistor MP7, V_{TP6} = threshold voltage of MP6, I_{DSP6} = drain-source current of MP6, and I_{DSP8} = drain-source current of MP8.

5.2.1.2 Case 2: When $V_{in} = V_{DD}$

Based on V_{ctrl} this case can be divided into case 2A and case 2B. Initially, when the control input is zero (V_{ctrl} = 0) and finally, when control input is V_{DD} ($V_{ctrl} = V_{DD}$).

Case 2A: V_{ctrl} = 0, transistor MN9 is ON and MN10 is OFF. As $V_{in} = V_{DD}$ and V_2 = HI, transistors MN6, MN7 and MN81 are ON, V_{out} = 0 (HI state of V_2 is transferred to 0). At $0 \leq V_{in} \leq V_{TN7}$, transistors MN6 and MN7 are off, $V_{out} = V_{DD}$. At $V_{TN7} \leq V_{in} \leq (V_{TN6} + V_{DS7})$, MN7 is on and MN6 is off.

Similarly, as mentioned earlier, $I_{DSN81} = I_{DSN7}$, forming a feedback path. By equating the currents and on simplification, we get the falling edge voltage for proteresis (V_{PFE}) as given in

equation (5.2),

$$V_{PFE} = \frac{V_{DD} + V_{TP6} + \sqrt{\frac{\beta_{n81}}{\beta_{p8}}} V_{TN7}}{(1 + \sqrt{\frac{\beta_{n81}}{\beta_{p8}}})} - \frac{V_{DD} + V_{TP8}}{(1 + \sqrt{K_{n1}})(1 + \sqrt{\frac{\beta_{n81}}{\beta_{p8}}})} \tag{5.2}$$

Where, K_{n1} = ((WN7/LN7)/(WN81/LN81)), V_{TN7} = threshold voltage of MN7, V_{TP8} = threshold voltage of MP8.

Case 2B: $V_{ctrl} = V_{DD}$, transistor MN9 is OFF and MN10 is ON. $V_2 = V_{out} = V_{DD}$, when MN82 is conducting and slowly will pull down the output to zero. The same calculation is repeated for transistor MN82, we get the falling edge voltage for hysteresis (V_{HFE}) as given in equation (5.3),

$$V_{HFE} = \frac{V_{DD} + V_{TP6} + \sqrt{\frac{\beta_{n82}}{\beta_{p8}}} V_{TN7}}{(1 + \sqrt{\frac{\beta_{n82}}{\beta_{p8}}})} - \frac{V_{DD} + V_{TP8}}{(1 + \sqrt{K_{n2}})(1 + \sqrt{\frac{\beta_{n82}}{\beta_{p8}}})} \tag{5.3}$$

Where, K_{n2} = ((WN7/LN7)/(WN82/LN82)).

We observe that by changing the flow of current through MN81 and MN82, we can obtain two separate falling edges of V_{HFE} and V_{PFE} leading to hysteresis or proteresis response respectively.

Practical consideration: Consider, V_{DD} = 1.8V, and using equations (5.1), (5.2) and(5.3), V_{RE} is fixed at 0.9V. The transistor dimensions of MP8 and MP6 decide the rising edge value. V_{FE} varies for hysteresis and proteresis. For Hysteresis, V_{HFE} = 1.1V (delayed falling edge) with transistor dimensions as follows, MN81 = 10μ/180n, MN7 = 5μ/180n, For Proteresis, V_{PFE} = 0.7V (early falling edge) with transistor dimensions as follows, MN82 = 240n/180n, MN7 = 5μ/180n.

5.3 ProHys switch simulation results

The layout of ProHys switch is shown in Fig. 5.4 and it occupies an area of 41μm x 48μm with a power consumption of 1.18mW. The post-layout simulation is performed on layout extracted design at an input signal (V_{in1}) which has a frequency of 10MHz with a supply voltage of 1.8V.

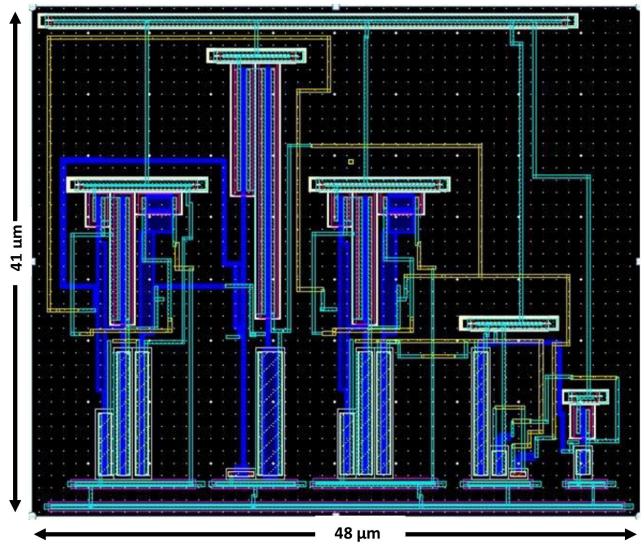


Figure 5.4: Layout of ProHys switch

The response of ProHys Switch using above dimensions is depicted by the VTC of hysteresis and proteresis shown in 5.5. The values of triggering voltages are V_{RE} = 0.9V, V_{HFE} = 1.12V (for hysteresis), V_{PFE} = 0.7V (for proteresis). The noise immunity is given as the loop width in VTC of proteresis and hysteresis which is 0.2V in both states. The transient response of the output (V_{out}) is plotted for both hysteretic and proteretic states shown in Fig. 5.6 . It is evident that the proteretic response (green signal) is advanced when compared to the hysteretic response (violet signal).

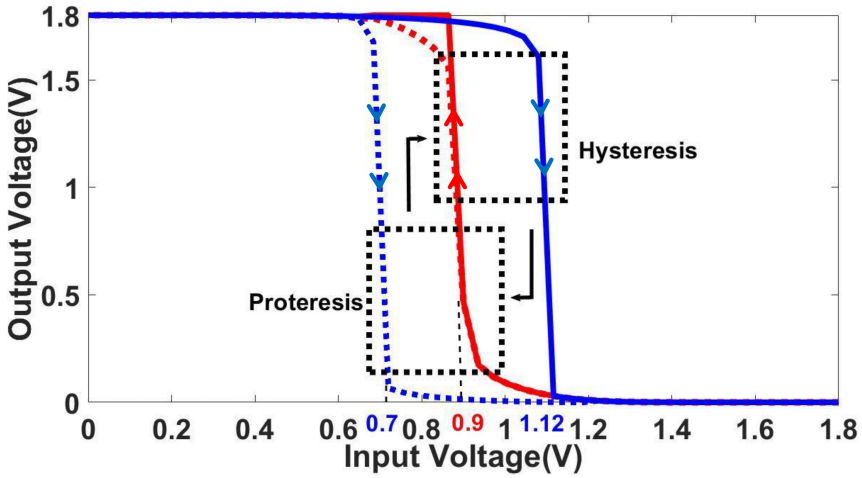


Figure 5.5: VTC of ProHys switch

The transient response of ProHys Switch at input signal frequency of 10MHz with varying control input (V_{in2}) is shown in Fig. 5.7. As the control signal V_{in2} is high, the switch is in

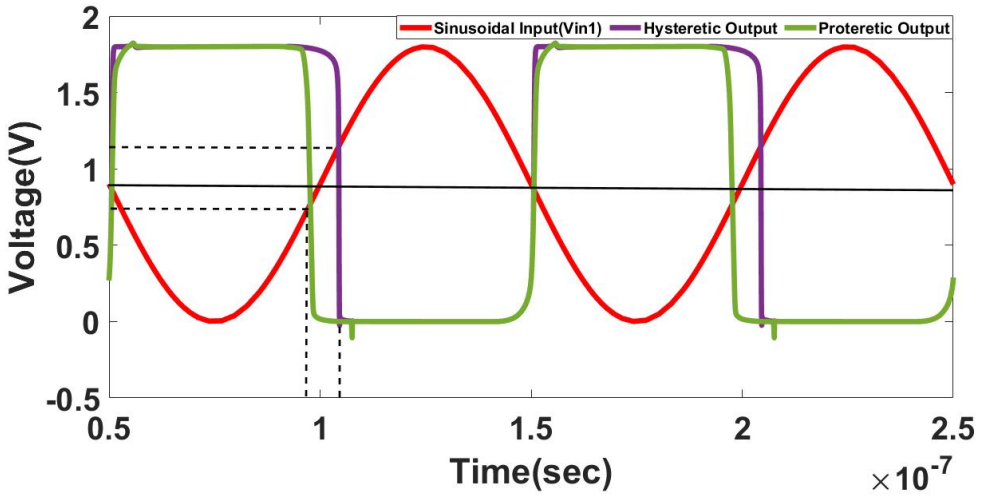


Figure 5.6: Transient analysis of ProHys switch at input signal frequency 10MHz with hysteretic and proteretic output (v_{out})

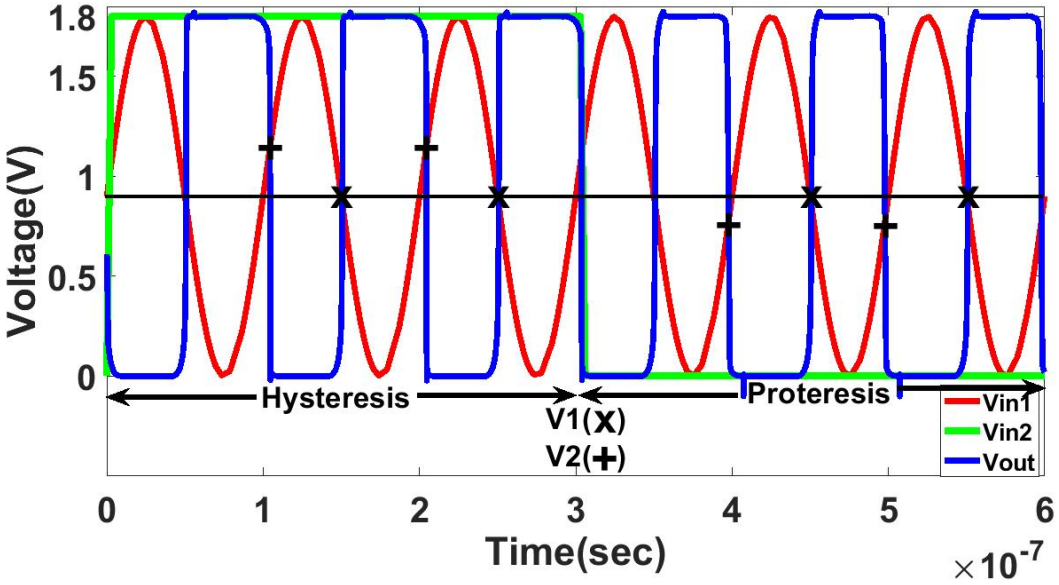


Figure 5.7: Transient analysis of ProHys switch at input signal frequency 10MHz with varying control input (V_{in2})

hysteretic mode, which is from 0μsec to 0.3μsec. On careful observation, it is depicted that as long as control signal V_{in2} = 1.8V (high), the output demonstrates a falling edge at 1.1V (V_{2H}) denoted by (+) symbol and rising edge at 0.9V (V_{1H}) denoted by (X) symbol. However, as the switch changes from high to low i.e. V_{in2} = 0V (low), the switch is in proteretic mode, which is seen from 0.3μsec to 0.6μsec. It is depicted that the output demonstrates a falling edge at 0.7V (V_{1P}) denoted by (+) symbol and rising edge at 0.9V (V_{2P}) denoted by (X) symbol. Latency of one cycle is noted in both cases. It is observed that at plain sight it is difficult to identify

hysteresis and proteresis from transient response. For this purpose, an important concept of differential voltage (ΔV) is introduced as seen in Fig. 5.8. It is calculated as the difference in the rising and falling edges of both hysteresis and proteresis as given in equations (5.4), (5.5) and (5.6).

$$\Delta V = FallingEdge - RisingEdge \tag{5.4}$$

$$\Delta V = V_{2H} - V_{1H} = +0.2V = Hysteresis \tag{5.5}$$

$$\Delta V = V_{1P} - V_{2P} = -0.2V = Proteresis \tag{5.6}$$

The Fig. 5.8 demonstrates a positive voltage for ΔV for hysteresis and negative voltage for ΔV for proteresis and both the phenomenon can be easily identified. To ascertain the robustness of the circuit, the ProHys performance is observed at a temperature variation of -20°C to 100°C as seen in Fig. 5.9.

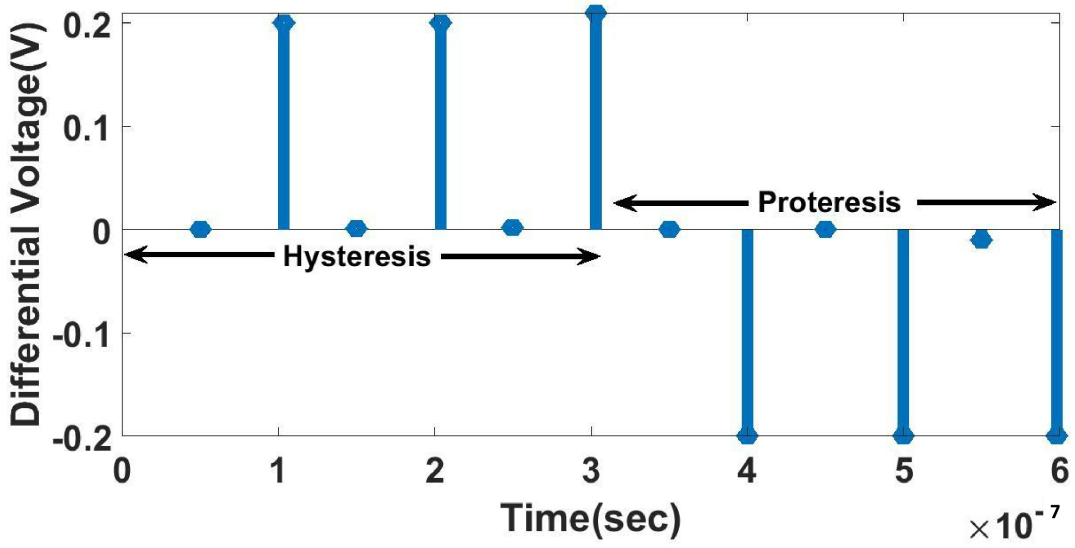


Figure 5.8: Transient analysis of differential voltage of the switch

This section described a circuit level implementation of a ProHys switch, which operates in two states, hysteresis and proteresis. The post-layout simulation results indicate that the

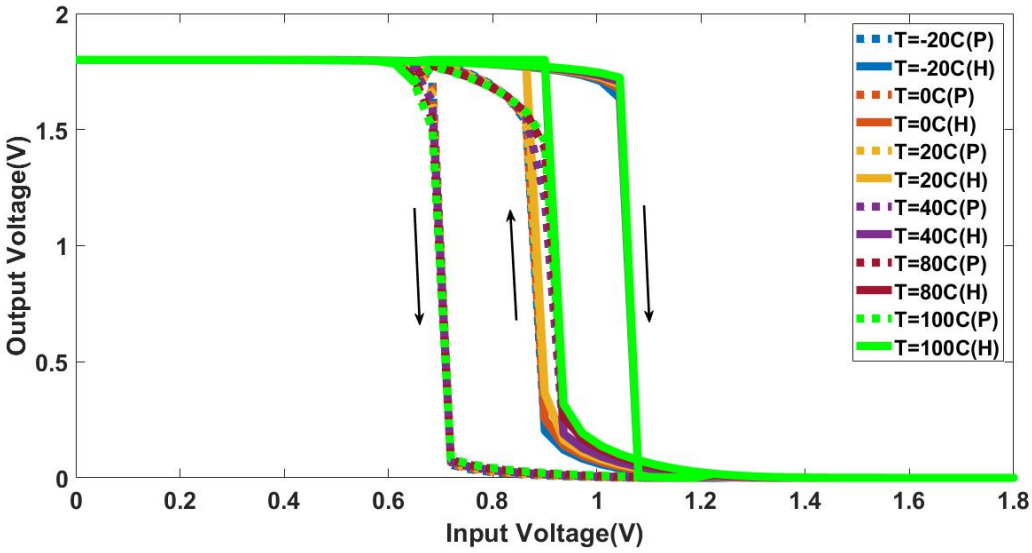


Figure 5.9: VTC for temperature variation of ProHys switch from -20°C - 100°C where P-Proteresis and H-Hysteresis

circuit exhibits switching up to an input frequency of 10MHz. The noise immunity of the device is 0.2V in both states. The design occupies an area of 41µm x 48µm with a power consumption of 1.18mW.

Chapter 6

ProHys PUF: A Proteresis - Hysteresis Switch based Physical Unclonable Function

With IC's becoming pervasive in all key industries and applications, PUF's has gained immense popularity for securing the IC's by providing unique identification code to each chip. Designing a highly efficient PUF with optimal values of uniqueness and reliability is a significant challenge. Uniqueness depends on process variations during chip fabrication, and reliability depends on the chip's ability to resist changes to supply voltage and temperature variations. Multiple PUF designs that employ reliability enhancement circuits and security algorithms achieve these design characteristics. Nonetheless, these techniques are design overheads. This thesis presents a novel PUF based on the ProHys switch. It deals with hysteresis and proteresis mode of operation, which are complementary to each other. The Prohys PUF befittingly satisfies both uniqueness and reliability criteria, without any additional circuitry or security algorithms.

6.1 Physical Unclonable Function (PUF)

The design of secure integrated circuits is of prime importance in the current era of hardware cloning, counterfeiting and intrusion. There is a need for a safe, cost-effective solution to enable hardware authentication. Activities such as device authentication and secret key generation in cryptography for resource constrained platforms such as RFID's can be too costly. PUF's have

emerged as innovative circuits for this purpose. This section demonstrates the use of PUF‘s for highly secure data transfer and storage, which is difficult to clone by an unauthorised entity.

PUF is a very effective method of ensuring hardware security, as it relies on the chip manufacturing process variations for the generation of secret keys [69]. Earlier, an externally generated hardware key would be stored in a non-volatile RAM inside the chip, and the same would be used for authentication. It is again susceptible to micro-probing and hacking. PUF can overcome the above issues as the key is generated internally due to the intrinsic attributes of every chip and is unique [70]. Uniqueness and reliability are two key performance indicators that ascertain the effectiveness of a PUF design. Uniqueness is the PUF's ability to identify an IC uniquely, and it is directly dependent on its sensitivity to process variations. It should ideally be 100%. Reliability is the stability of this unique ID concerning variations in environmental conditions like supply voltage fluctuations and temperature changes, and it should ideally be 100% [71; 72]. The input of PUF is called a challenge, and its output is the response. Depending on the number of challenge response pairs (CRP), the PUF's are classified as strong PUF [73; 74] and weak PUF [75; 76]. Strong PUF's are those in which the response is related exponentially to the challenges and weak PUF in which the response is related linearly to the challenges. Based on the conventional design approach, the PUF's are classified as MUX/Arbiter PUF [77; 78], Ring Oscillator PUF [79; 80], and SRAM-based PUF [81; 82; 83]. Early papers on PUF design using the above methods have established acceptable results in terms of uniqueness and reliability.

In contrast to conventional PUF's, new designs that highlight the need for out-of-box thinking and provide better performance results have been proposed recently. A new PUF based on thyristor sensors employs time difference amplifiers, comparators, and extra securing algorithms like voting mechanism and diffusion algorithm to achieve a highly stable and efficient response [84]. PUF circuits are susceptible to temporal noise leading to a high native bit error rate. An effort to improve the BER using cascode current mirror array PUF is established [85]. Meanwhile, a cross-coupled comparator PUF is presented in [86] that leverages the effect of PTAT and CTAT in the bit cell design to improve immunity against temperature variations. Also, using current-starved inverters with a negative temperature coefficient helps mitigate variations in ring oscillator frequencies with temperature [87]. Parallel efforts are in progress to design novel PUF's using divergent methods like printed electronics, in which a printed differential circuit PUF is developed [88]. An interesting attempt to PUF design using

chaos-based logic gates and standard logic gates with less design overhead is explored [89]. A curious design attempt to exploit domain-wall memory (DWM) has led physical magnetic systems to design spintronic PUF [90; 91].

The issue with the aforementioned PUF's is that they do not score well with both reliability and uniqueness, and either of the two parameters is compromised. This chapter presents a novel scheme of PUF design around a concept of CMOS Prohys switch introduced in Chapter 5. The focus is to provide a simple CMOS circuit that is random enough to provide high uniqueness and robust enough to provide high reliability, without the need for any added overheads of voting mechanisms or securing algorithms. To the best of our knowledge, it is the first attempt to design a PUF based on the prohys phenomenon. An attempt is made to establish the competitive edge of this PUF design over contemporary designs.

6.2 Features of a PUF

- PUFs significantly increase physical security by generating volatile secrets.
- PUF do not require any special manufacturing process or programming and testing steps.
- The characteristics of a PUF are to be

  (a) Robust (stable over time),

  (b) Unique (no two PUF's are the same),

  (c) Easy to evaluate (to be feasibly implemented),

  (d) Difficult to replicate (so the PUF cannot be copied) and

  (e) Very difficult or impossible to predict (so the responses cannot be guessed).

6.3 Performance parameters of PUF

The key design parameters of PUF are uniqueness and reliability, but their requirement is diametrically opposed. Uniqueness demands that the process variations of every chip should be so random that it leads to a totally unpredictable response and no other chip should generate a similar response. On the other hand, the reliability parameter demands that the variation of

the chip response with respect to temperature and supply voltage should be minimal or zero. Hence, it is quite challenging to design a chip that meets both criteria at the same time and many efforts have been made in this regard to achieve near ideal values of uniqueness (100%) and reliability (100%).

6.3.1 Reliability

The reliability of PUF is measured by varying temperature and supply voltage conditions for a standard input digital signature. The ideal response remains fixed to these external variations. The change in output will happen if a bit flip occurs in the response, the probability of occurrence of this bit flip is called P_{intra}. All the bits of a PUF response have the same value of P_{intra}, since each bit is generated independently by the same PUF instance. As a result, P_{intra} is used to represent the intra-chip variation for the entire response, which is considered to be L bits. The average Hamming distance (HD) is a crucial parameter that is used to measure the intra-chip variations of the PUF, which is in terms of P_{intra} [69].

The averaged HD or intra chip variation is described by equation (6.1),

$$P_{\text{intra}} = \frac{1}{m}\sum_{i=1}^{m}\frac{HD(R_{\text{x}},R_{\text{y}})}{L} \times 100\% \tag{6.1}$$

Where R_x and R_y denote two measurements of the PUF under variant conditions, m is the number of hamming distance comparisons. The averaged intra-chip variation directly impacts the value of P_{intra}, if the responses are sampled sufficient number of times. As smaller intra-chip variation means better reliability, the reliability indicator is defined as,

$$Reliability(R) = 1 - P_{\text{intra}} \tag{6.2}$$

The ideal value for P_{intra} is 0% leading to ideal reliability being 100%.

6.3.2 Uniqueness

A measure of inter-chip variation is a suitable means to calculate the uniqueness of PUF. This is ascertained by comparing the digital signature of one PUF to that of another. The probability that the bits generated by the same challenge for different PUF instances is defined as P_{inter}. Since uniqueness is a measure of inter-chip performance, all possible chip combinations should be considered. Therefore, the expected value of inter-chip variation or average inter-chip HD for K ProHys PUF's is described in the equation (6.3) below [69],

$$P_{\text{inter}} = \frac{2}{(K-1)K} \sum_{i=1}^{K-1} \sum_{j=i+1}^{K} \frac{HD(R(i),R(j))}{L} \times 100\% \tag{6.3}$$

$$Uniqueness(U) = 1 - |2P_{\text{inter}} - 1| \tag{6.4}$$

For two different PUF instances i and j, whose responses R_i and R_j are of length L each, the uniqueness for K PUF's is defined as shown in equation (6.4). Since P_{inter} = 50% represents the best uniqueness for a PUF. A uniqueness value of 100% implies that PUF responses across the measured device set are random.

6.4 Different types of PUF

There are mainly two kinds of conventional PUF's, first is the MUX/Arbiter based PUF and the second type is ring oscillator based PUF (RO PUF) other than memory PUF's. This section discusses in detail about the two basic PUF structures with their pros and cons.

6.4.1 Mux/Arbiter PUF

An arbiter/MUX based PUF is described in Fig. 6.1 consists of series of muxes whose select lines are controlled by challenges leading to different delay paths between input and output. It has a multi-bit input X, generating a single bit output Y based on delay difference between the

paths. The input bits determine the delay paths by controlling the muxes [71].

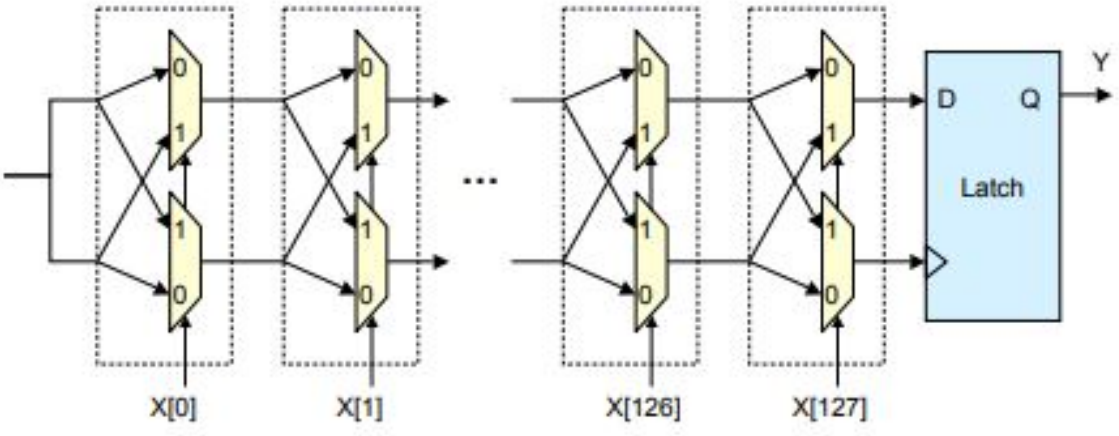


Figure 6.1: A MUX/Arbiter based PUF [71]

The experimental results of the circuit shown in Fig. 6.1, generates a probability of 23% (inter-chip variation).The MUX circuit measures the delay difference, the PUF is robust with respect to environmental variations. The inter-chip variation of Arbiter PUF is 23%, allowing for the identification of individual chips. A symmetric layout for the circuit in Fig. 6.1 would increase inter-chip variation to 50%.

Further, the statistical analysis of MUX-based PuF's are described in detail for different types of Feed-Forward MUX (logic reconfigurable PUF) and their modified versions [69]. The three variants for the same are feed-forward overlap (FFO), feed-forward cascade (FFC), whose ending stage of a feed-forward path will be the starting stage of another feed-forward path and finally, feed-forward separate (FFS) where different feed-forward paths are separate; thus, no stage overlap exists between the two feed-forward paths. They improve security by adding non-linearity to original MUX, which uses the racing result of an intermediate stage as a select line to a later state. All MUX based structure can be used as reliable secret keys for authentication and identification within certain limits of error tolerances. The statistical analysis between the above mentioned MUX using key performance indicators helps in choosing the appropriate MUX based on its application.

6.4.2 Ring Oscillator (RO) PUF

The PUF design based on delay loops (ring oscillators) and counters shown in Fig. 6.2 is named as RO PUF. On Comparison to the MUX based PUF, RO PUF has an easier implementation for ASIC's and FPGA's. On the contrary, the RO PUF is slower, larger and consumes more power to generate bits than the MUX based PUF. Therefore, the two designs are opposite to each other, the MUX PUF is used for RFID's and the RO PUF is used in FPGA's.

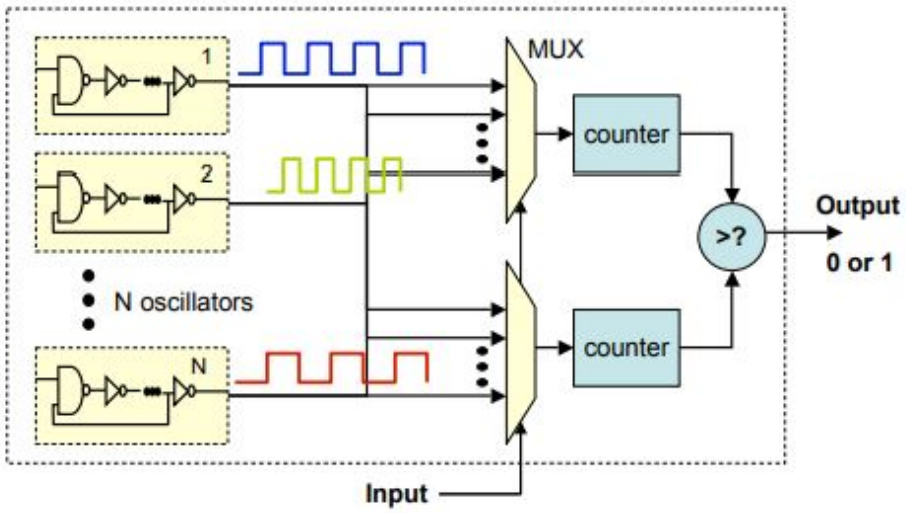


Figure 6.2: Ring Oscillator based PUF Circuit [71]

Fig. 6.2 describes an RO delay circuit which consists of identical delay loops (ring oscillators) where each RO oscillates at a particular frequency. Based on manufacturing variation, each unit oscillates with a slightly different frequency. In order to generate fixed bits, RO pairs are selected, and their frequencies are compared to generate an output response bit. The response bits for the same sequence of RO pair comparisons will differ from die to die. The difference in frequencies are determined by manufacturing variation and an output response bit is equally likely to be either of one or zero if random variations dominate.

The RO frequencies change significantly as the environmental conditions changes. The PUF output changes only if the ordering of the two RO's are being compared. Fig. 6.3 shows how many bit-flips that occur due to environmental changes. Assume that RO in blue is faster than RO in green at room temperature. As the temperature increases, both RO's slow down, with blue slowing down faster than the green, due to this different device parameters. The RO's flip when the temperature changes. This flip causes an error in the generated response bit. The RO

frequencies change significantly as environmental conditions such as temperature and voltage change.

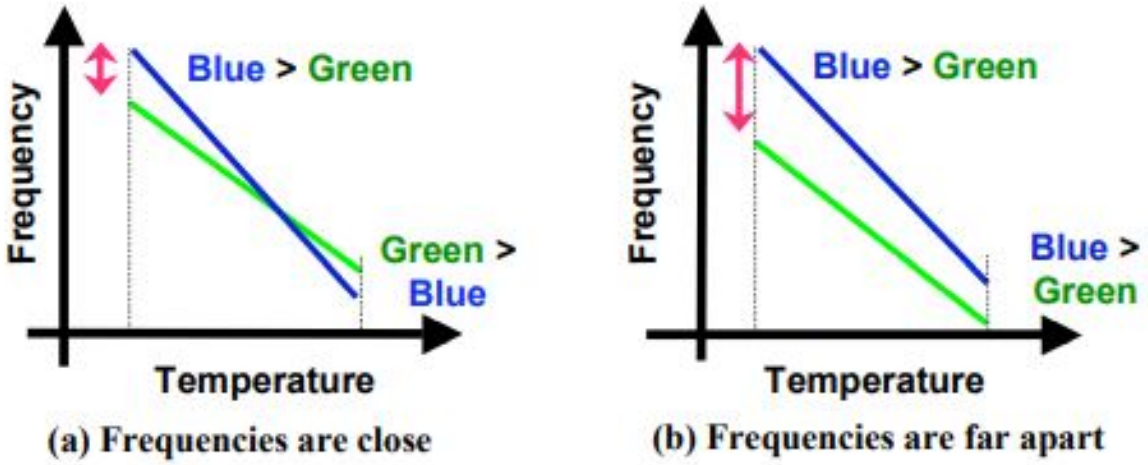


Figure 6.3: Temperature Vs frequency Vs output bit flip [71]

Effect of temperature and voltage variation as per Fig. 6.3 depends on, the frequency of RO changes with temperature and voltage variations. Bit Flip errors results due to these changes. It is concluded from adjacent figure that RO whose frequency is far apart are less likely to flip the bit. Hence, frequency should be carefully selected.

The experiments for RO PUF for 15 FPGA's of exactly the same model wit 1024 ring oscillators in each FPGA as a 16-by-64 array. Each RO has five inverters and one AND gate. The inter-chip variation for 128 bits that are produced from each PUF (FPGA) has an average inter-chip variation of 46.15% with 92.3% uniqueness. The intra-chip variation under various temperature (-20°C to 120°C) and voltage (±10%) changes comes upto 0.48% with reliability 99.52% [71].

6.5 Feasibility of the proposed ProHys switch as PUF

As discussed in the introduction, a crucial parameter for PUF design is the randomness in the output based on changes in process variations of integrated circuits. This section gives a detailed analysis of the proposed prohys switch to work as a PUF. Fig. 6.4 depicts the voltage transfer characteristics of the prohys switch and the behavior of its falling and rising edges at the FF, SS, SF, and FS corners. Fig. 6.4(a) and Fig. 6.4(b) depict the falling edge and the rising edge

variation in the hysteretic mode indicating the randomness in the switching voltages to process corners. Similarly, Fig. 6.4(c) and Fig. 6.4(d) show the corner analysis in proteretic mode.

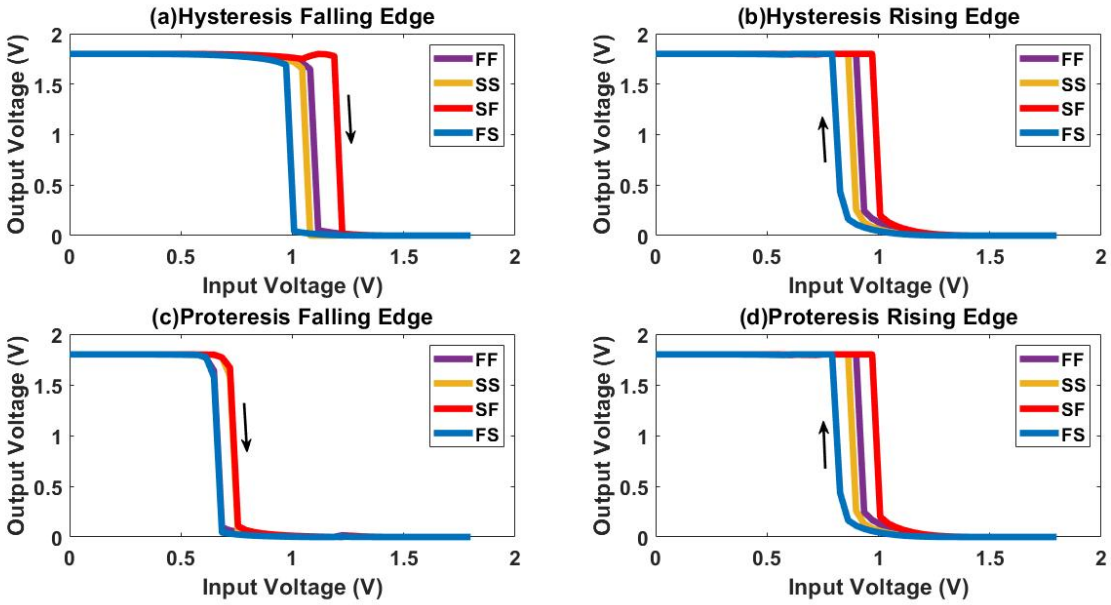


Figure 6.4: Falling and rising edges of hysteresis and proteresis at different process corners

Table 6.1: Switching voltages of hysteresis and proteresis at different process corners

Process Corners	**V_{HFE} (V)**	**V_{HRE} (V)**	**V_{PFE} (V)**	**V_{PRE} (V)**
FF	1.13	0.94	0.67	0.94
SS	1.1	0.91	0.739	0.91
SF	1.21	1	0.739	1
FS	0.99	0.81	0.68	0.81

The value of V_{HFE}, V_{PFE}, V_{HRE}, and V_{PRE} at different corners are given in Table 6.1. It is observed that the rising edges in both modes occur at the same voltage. However, marked variation is seen in V_{HFE} between 0.99V to 1.13V for hysteretic mode and V_{PFE} between 0.67V to 0.73V for proteretic mode. The corner analysis of the transient response of the ProHys switch is shown in Fig. 6.5 and Fig. 6.6, wherein a sinusoidal input signal (V_{in}) at a frequency of 10MHz is applied to the switch. The switch operates in proteresis mode when V_{ctrl} = 0V and hysteresis mode when V_{ctrl} = 1.8V (V_{ctrl} is not shown in the figure). Fig. 6.5 is the transient response in the hysteretic mode, where the falling edge is steady. There is a slight variation of the rising edge, demonstrating the stability of the hysteretic mode of operation.

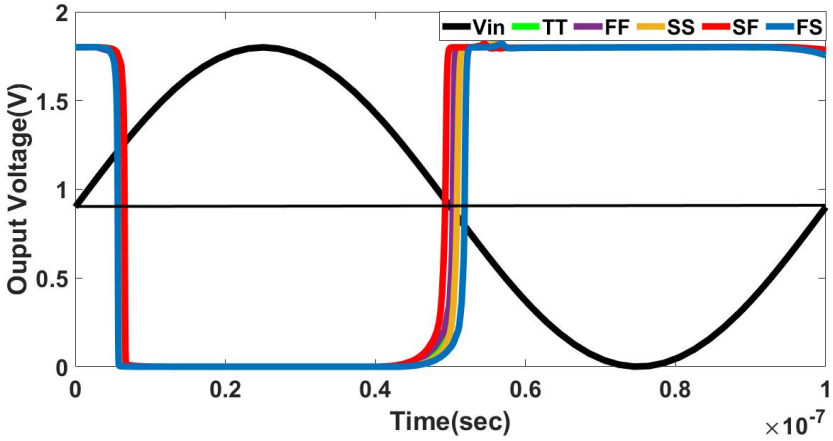


Figure 6.5: Transient analysis of ProHys switch at input signal frequency 10MHz in the hysteretic mode of operation at different corners

Fig. 6.6 illustrates the transient response of the proteretic mode at various corners. The output response in TT and FF mode is falling at values greater than 0.9V, and the remaining corners (SF, FS, FF) have the falling edges at a value less than 0.9V. This variation of falling edge for proteretic mode is a random feature that can further enhance the output to V_{DD} and 0 by using an inverter block in the subsequent stage. There is a slight variation in the rising edge, which is not very significant. Thus, leading to an unpredictable combination of 1's and 0's, which is the essential requirement to design the building block of a PUF.

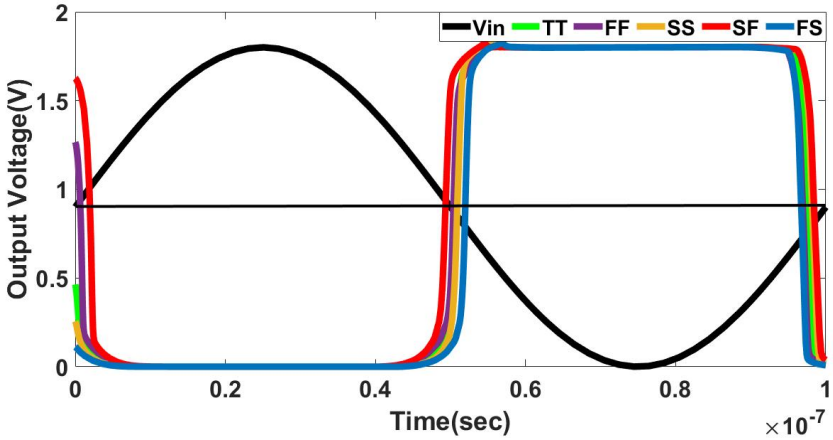


Figure 6.6: Transient analysis of ProHys switch at input signal frequency 10MHz in the proteretic mode of operation at different corners

6.6 Architecture of proposed ProHys PUF

Fig. 6.7 shows the block diagram of the proposed PUF cell based on the prohys switch. The PUF cell consists of two 2:1 muxes, two prohys switches and one D flip flop. A four-bit input challenge consisting of A, B, X and Y is applied to the PUF cell. Two signals A and B are given as multiplexer inputs and two inputs X and Y are connected to the select line of multiplexers. The outputs of two mux which will be either 1 or 0 will be given to control inputs (V_{ctrl}) of ProHys switch leading to the flipping of mode between proteretic and hysteretic. The output of the prohys switch, which works in the proteretic mode has variable falling edges. Due to two prohys switches, there is a possibility of four modes – HH, HP, PH and PP where P stands for proteretic and H for hysteretic. This indicates that there is uncertainty in 75% of the overall possibilities. Only the HH combination will have a fixed predictable output. The output of Prohys switch of path one is given to the input terminal D and path two to the clock of the delay flip flop (DFF), as shown in Fig. 6.7. The variation in voltage values of prohys switch is consolidated by the DFF that can generate a stable response bit.

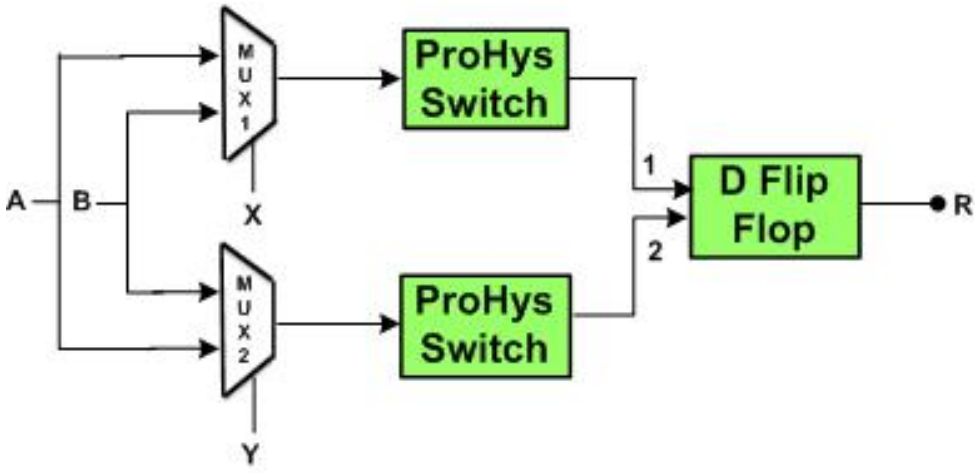


Figure 6.7: Block diagram of single PUF cell

The architecture of the proposed ProHys PUF is given in Fig. 6.8, wherein a PUF challenge $C_0 – C_{N-1}$ is divided into sub-challenges each of size four bits known as a quadruple (C_Q) and given to the PUF cell. Each PUF cell generates one response bit and considering that there are M PUF cells, we get M response bits R_0 - R_{M-1}. In order to generate M bit response, we need a 4M bit challenge. Each sub-challenge (C_Q) comprises of a quadruple given in equation

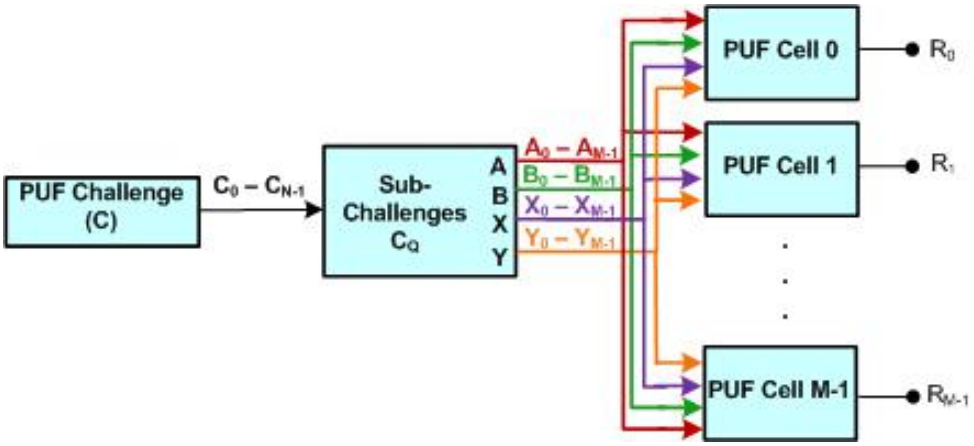


Figure 6.8: ProHys PUF block diagram

(6.5),

$$C_Q = (A, B, X, Y) \tag{6.5}$$

Where, C_Q is the Qth sub-challenge of challenge C, and A, B, X, Y = (0, 1, 2, ..., M-1). PUF response is based on intrinsic process variations of PUF cell with the challenge C, generating equation (6.6),

$$R = f(C_Q) \tag{6.6}$$

Where, R is the response generated by the PUF cells.

It is pertinent to mention that the PUF architecture is highly reliable to variations in temperature and voltage due to the robust design of the ProHys switch. However, the design, when implemented on another IC will lead to variations due to process corners as shown above and caters to improve the uniqueness of one chip to the other such that no two different IC will give the same response for a give input challenge.

6.7 Results and Discussion

This section discusses the results obtained by the proposed ProHys PUF using performance parameters explained earlier in this chapter. Monte-Carlo simulation is a strategic tool to analyze

the PUF performance. This work focuses on analyzing the performance of ProHys PUF, incorporating the process and environmental variations. The proposed ProHys PUF is implemented in TSMC 180nm 1.8V CMOS process and proof of concept is demonstrated by post-layout simulations. The design implements a 128-bit input challenge to generate 32-bit output response. Here, 32 PUF cells comprising of 64 Prohys switches, and each PUF Cell has two prohys switches. The layout of the PUF chip is shown in Fig. 6.9 and the area occupied is 328μm X 200μm with a power consumption of 68.24mW.

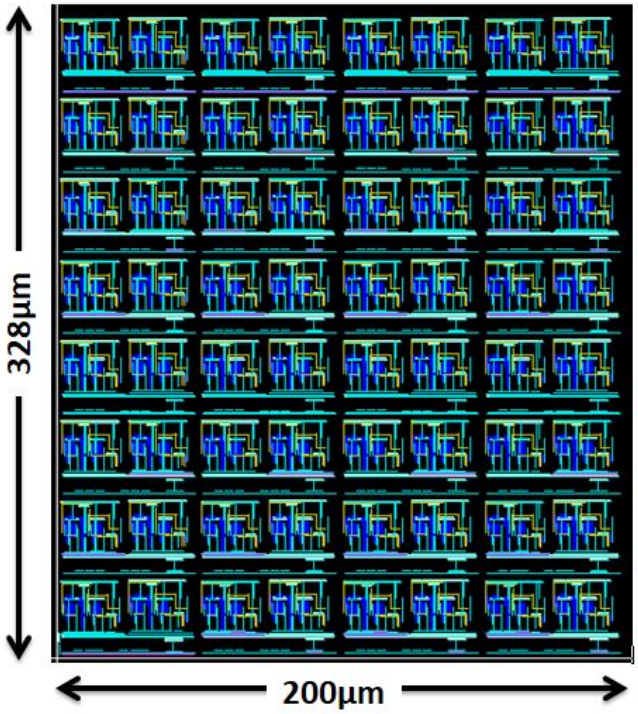


Figure 6.9: The Layout of the proposed ProHys PUF

6.7.1 Reliability of the proposed ProHys PUF

This section presents reliability aspect of the prohys PUF using 1000 monte-carlo simulations indicating 1000 PUF chip instances (1000 monte-carlo runs) to test at various temperatures from -40°C to 100°C with a supply voltage of 1.8V. Further, the same process is repeated by varying supply voltage from 1.7V to 1.9V at 27°C temperature. Fig. 6.10 shows the reliability of ProHys PUF with respect to temperature. It is observed that the worst reliability is seen at the extreme temperature conditions as 97.8% and 97.9% at 100°C and -40°C, respectively.

The reliability of ProHys PUF with respect to supply voltage is shown in Fig. 6.11. The

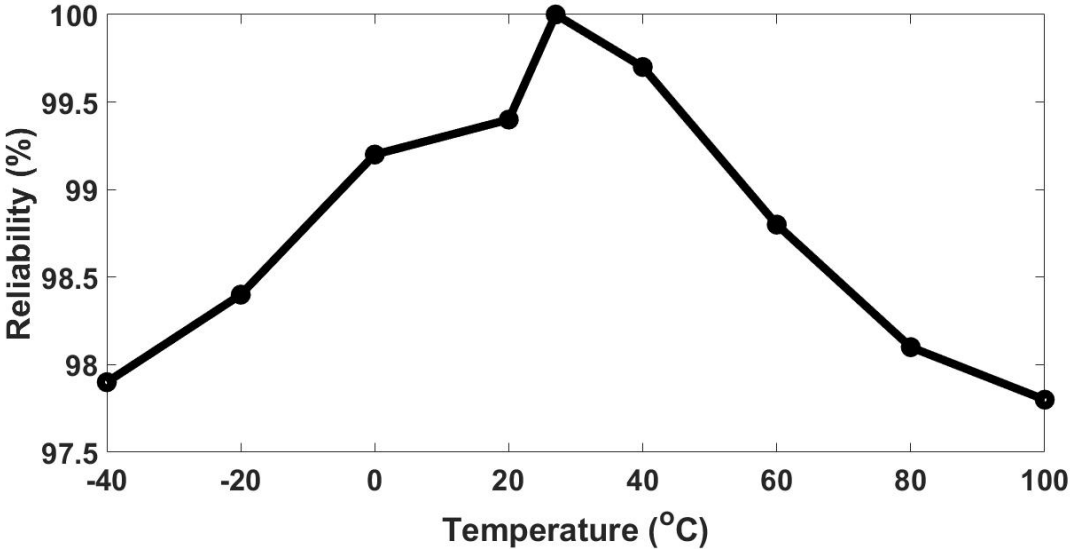


Figure 6.10: PUF Reliability versus temperature

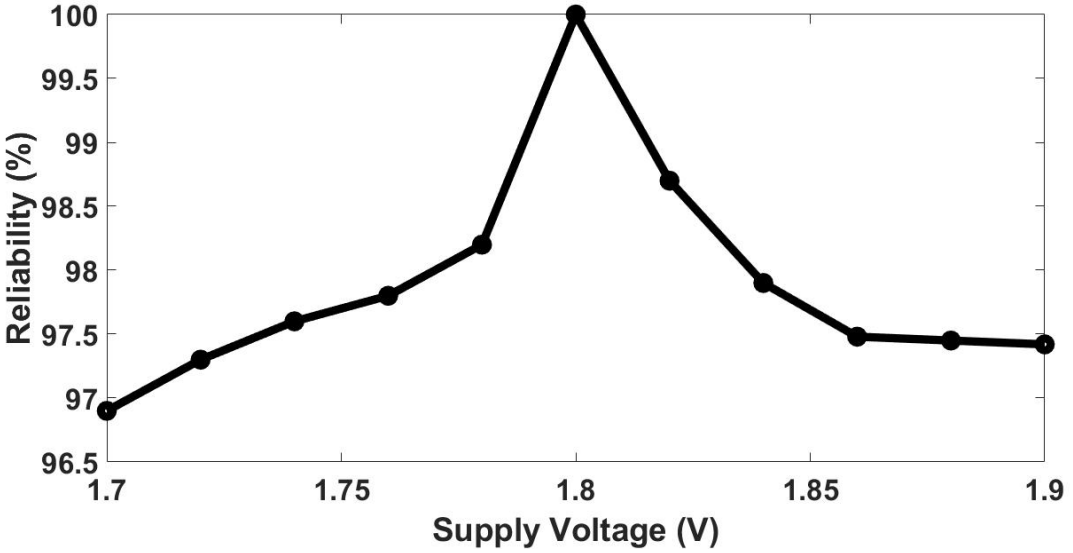


Figure 6.11: PUF Reliability versus supply voltage

value of reliability is noted by varying supply voltage at $\pm$0.1V to the proposed ProHys PUF at 27°C. The worst reliability is 96.9% at 1.7V and increases for the other values of the supply voltage. These values of reliability for both supply and environmental variations are close to the ideal value making it a good candidate for PUF design. The proposed ProHys PUF has good reliability without using any reliability enhancement circuits compared to the present state of art designs.

6.7.2 Uniqueness of the proposed ProHys PUF

The statistical distribution of hamming distance, also known as inter PUF HD, is shown in Fig. 6.12. This captures the variations in the fabrication process at 27°C and 1.8V supply voltage, which enables a unique identification of an IC in a given population. Fig. 6.12 demonstrates the measured histogram of the Hamming distance between 1000 chip instances. The mean of the Hamming distance distribution for PUF instances of the proposed Prohys PUF is measured to be 49.85%, thus leading to uniqueness of 99.7%.

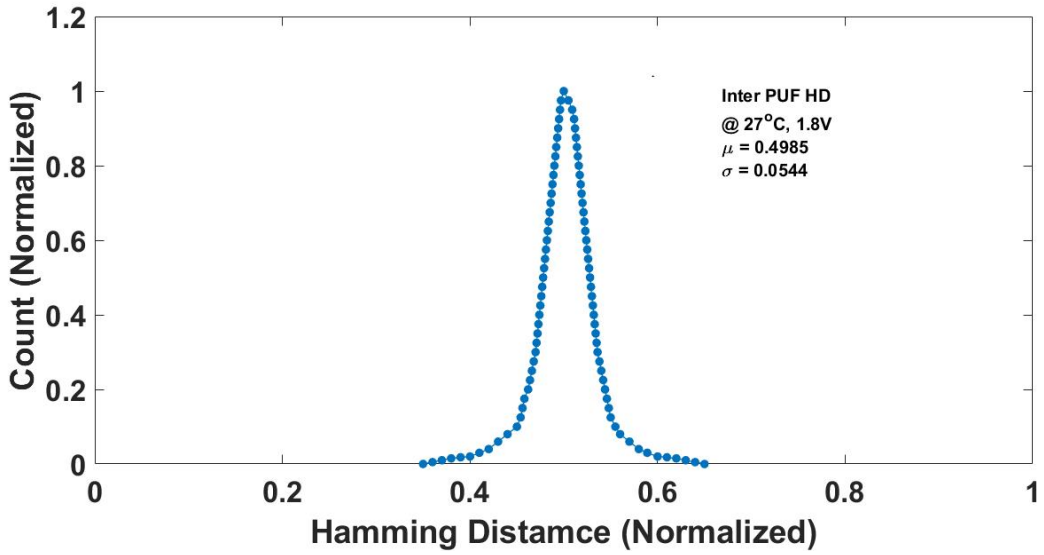


Figure 6.12: Inter-PUF HD at normal operating conditions (27°C / 1.8V)

6.8 Comparison of the ProHys PUF with present state - of - the - art implementations

This section discusses the comparative analysis of the proposed ProHys PUF with the present state-of-the-art and the same is presented in Table 6.2. It is observed that the RO-based PUF [71] has good average reliability of 99.5% but falters on the uniqueness aspect with a low value of 92.3%. On the contrary, the Duty Cycle-based PUF [80] has high uniqueness of 98.6%, but its reliability reduces to 92%. In contrast to the above two designs, the proposed ProHys PUF provides high reliability of 96.9% and uniqueness of 99.7%. In addition, the thyristor

PUF [84] is unable to achieve reliability equivalent to ProHys PUF even after using extra voting mechanism circuitry. Hence, the proposed ProHys PUF stands out in terms of performance parameters of reliability and uniqueness and is an ideal candidate for securing the integrated circuits.

Table 6.2: Performance comparisons with state-of-the-art PUF implementations

Parameter	**[71]**	**[77]**	**[80]**	**[84]**	**[91]**	**[92]**	**This Work**
Tech. (nm)	90	90	22	180	40	65	180
$V_{DD}(V)$	1.1	-	0.95	1.8	1	1.2	1.8
Type	RO	ST	DC	Thyristor	Spintronics	ST Inv	ProHys
TR (°C)	-20∼ 120	-10∼ 100	0∼ 100	-40∼ 100	-45∼ 100	-40∼ 120	-40∼ 100
VR (V)	1.08∼ 1.2	1.08∼ 1.2	0.9∼ 1	1.7∼ 1.9	0.9∼ 1.1	1∼ 1.4	1.7∼ 1.9
BER (%)	0.48	-	0.7	3.2	3.93	6.80	3.1
R (%)	99.52	-	92	96.8	96.07	93.2	96.9
U (%)	92.3	99	98.6	99	98	99	99.7
E (fj/bit)	-	957	-	-	-	55.91	213
TP (Mb/s)	-	2800	-	1	-	160	320
Area (mm^2)	NA	0.109	0.015	21.75	0.2451	4.1478	65.6

TR-Temperature Range, VR-Voltage Range, R-Reliability, U-Uniqueness, ST-Schmitt Trigger, DC-Duty Cycle, BER-Worst Bit Error Rate, E-Total Energy, TP-Throughput.

In this chapter, the design of ProHys PUF is proposed, which is used to generate enhanced performance parameters. ProHys Switch generated output is noted to have random behavior at different process corners making it a suitable candidate for PUF design. Monte-Carlo simulation confirms the design has good uniqueness and reliability. Simulation results generate a 32-bit response of the proposed PUF. It gives the intra-chip hamming distance of 49.85% at 1.8V, 27°C, generating a uniqueness of 99.7%. The worst reliability is at extreme conditions of temperature and supply voltage variations. The minimum reliability is 96.9% for temp variation of -40°C – 100°C and supply voltage variations 1.7V – 1.9V. These results validate the proposed PUF to be efficient, robust and stable with good reliability without using enhancement circuits. This can be further used in device authentication and secret key generation applications.

Chapter 7

Conclusion and Future Work

This thesis presents the circuit level design of a proteretic comparator in TSMC CMOS 180nm technology. Initially, the circuit would remain stable for only a specified range of input voltage, however this has been overcome by providing additional circuity at the output terminal. The design of the proteretic device is complicated to its hysteretic counterpart with an increased number of transistors and input feed-forward mechanism. The outcome of this completion is that a high-speed output is achieved for the design of a ramp generator with a proteretic device compared to a hysteretic device. The circuit speed performance increases by 25%, and the trade-off is a marginal increase in area and power. Thus, the thesis establishes that in systems where speed is a design constraint and area and power can be compromised, the best option is to implement a proteretic comparator rather than a hysteretic comparator. This work also proposes the design of a novel circuit that exhibits both proteretic and hysteretic characteristics called the prohys switch. The mathematical modeling of the prohys switch with its circuit implementation, and corner analysis is presented. It is observed that there is an element of randomness in the falling edge of prohys switch at various corners and this fact is leveraged to design a physical unclonable function (PUF). The last part of this thesis presents the design of a novel prohys PUF. The challenge of designing an efficient PUF with optimal values of uniqueness and reliability is addressed. Typically, additional circuitry that implements reliability enhancement and security algorithms that improve reliability are in vogue. The prohys PUF proposed here given the reliability of 96.9% and uniqueness of 99.7%, which has a competitive edge on the existing designs. The proposed prohys PUF achieves a high value of both reliability and uniqueness without using any reliability enhancement circuits or security algorithms and can be considered a significant contribution to state of the art.

Future Work

The superiority of proteretic design is established by implementing a high frequency ramp generator. A similar exercise can be done in all other circuits implementing a hysteretic comparator. Specially, the high-speed sigma-delta analog to digital converters. It will be befitting to observe the improvement in the overall circuit performance of an ADC when implemented with a proteretic design. The prohys switch proposed in this thesis is an important piece of contribution. Every system that has a comparator operation can be implemented with a prohys switch, and the user can be given the option to choose between the proteretic or hysteretic modes based on the design constraints in the field. For high-speed operation, the user can switch to proteretic mode, and for low power mode, the user can switch to hysteretic mode. Finally, the proposed design of prohys physical unclonable function is robust and can be used to secure any device. But, of late, PUF's are becoming vulnerable to machine learning attacks and are getting compromised. It remains of interest in the future to observe the robustness of the prohys PUF against machine learning attacks.

Related Publications

International Journals

1. **Salma Khan**, Syed Azeemuddin, Mohammed Arifuddin Sohel, 2022,"Proteretic Device: Modelling and Implementation in Electronics and Optical Domain ", *Semicond. Sci. Technol. Volume 37, Number 5*, DOI: 10.1088/1361-6641/ac6200

2. **Salma Khan**, Syed Azeemuddin, Mohammed Arifuddin Sohel, 2022,"ProHys PUF: A Proteresis - Hysteresis Switch based Physical Unclonable Function ", *Integration The VLSI Journal, Volume 89, Pages 207-216*, DOI: https://doi.org/10.1016/j.vlsi.2022.12.009

International Conferences

3. **Salma Khan**, Syed Azeemuddin, Mohammed Arifuddin Sohel, 2021, "High-Speed CMOS Ramp Generator using Proteretic Comparator ", *International Asia Pacific Conference on Circuits and Systems (APCCAS), IEEE*. DOI: 10.1109/APCCAS51387.2021.9687792

4. **Salma Khan**, Syed Azeemuddin, Mohammed Arifuddin Sohel, 2021,"CMOS Implementation of a Proteresis-Hysteresis (ProHys) Switch ", *International Midwest Symposium on Circuits and Systems (MWSCAS), IEEE*. DOI: 10.1109/MWSCAS47672.2021.9531694

5. **Salma Khan**, Syed Azeemuddin, Mohammed Arifuddin Sohel, 2020,"A low power low ripple Schmitt trigger based PWM Boost Converter for Energy Harvesting Applications ", *India Council International Conference (INDICON), IEEE.*
   DOI: 10.1109/INDICON49873.2020.9342419

Patents

6. Syed Azeemuddin, **Salma Khan**, 2021,“Proteresis-Hysteresis Switch Based Physical Unclonable Function (PUF) Circuit and a PUF System ”, *Indian Patent Published*, Application No. 202141049742.

7. Syed Azeemuddin, **Salma Khan**, 2021,“Design of a Ramp Generator Using CMOS Proteretic Comparator ”, *Indian Patent Published*, Application No. 202141060106.

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