Innovative Solutions for LDO Design Challenges in the Era of Expanding 3D NAND Flash Arrays: A Multi-Loop FVF Driver Topology Approach

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by

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CERTIFICATE

It is certified that the work contained in this thesis, titled 'Innovative Solutions for LDO Design Challenges in the Era of Expanding 3D NAND Flash Arrays: A Multi-Loop FVF Driver Topology Approach" by Ashish Papreja, has been carried out under my supervision and is not submitted elsewhere for a degree.

Date	Adviser: Prof. Syed Azeemuddin

To Whom It May Concern

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Abstract

In the current digital era, there has been an exponential surge in the demand for data storage and retrieval. This escalating need is propelled by a diverse range of applications, spanning from cloud computing and data centers to mobile devices and embedded systems. NAND flash memory, a non-volatile storage technology, plays a pivotal role in meeting these demands and is extensively employed in solid-state drives (SSDs), memory cards, and various other applications. Its notable feature is its high storage density, enabling the storage of substantial volumes of data in a compact and efficient form factor.

Industries have recently favored 3D NAND Flash over Traditional NAND Flash, where the "3D" denotes the vertical stacking of memory cells in multiple layers, akin to a skyscraper, to amplify storage density. While this stacking brings benefits, it presents challenges for analog circuit design engineers. As the number of layers increases, so does the load capacitance, introducing complexities in design as each new generation witnesses a rise in Load Capacitance. This challenge persists despite the growing number of vertical layers, particularly affecting the development of a robust and stable Low Dropout Regulator (LDO) amidst the increasing load capacitance in each generation. Moreover, the escalating layer count necessitates a proportionate increase in the number of LDOs to adeptly supply power to this expansive distributed network.

To tackle the aforementioned challenges, the thesis introduces a novel LDO featuring a Flipped Voltage Follower based driver (FVF), deviating from conventional drivers. This innovative design offers increased robustness, especially when applied to a 3D NAND Flash memory array, surpassing the capabilities of traditional architectures. The thesis advocates for a dual-loop scheme to enhance the transient performance metrics of the LDO. This proposed scheme not only diminishes settling time but also reduce the overshoot/undershoot voltage in comparison to existing state-of-the-art designs. Moreover, the thesis demonstrates how this structural approach can be extended to efficiently handle extensive distributed loads.

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Chapter 1

Introduction

1.1 Motivation

The advent of Artificial Intelligence has ushered in an era of unparalleled data complexity and volume. AI algorithms and models, designed to analyze vast data sets, have stretched the limits of conventional storage systems. Therefore, there is a pressing need for scalable and efficient memory solutions within data centers to sustain AI-driven innovation. NAND Flash technology played a pivotal role in addressing these burgeoning demands [1]. NAND Flash memory is a non-volatile memory used for storing data. It stores data by using floating-gate transistors and programmable threshold voltage levels.

A NAND flash memory cell consists of a series of transistors organized in a grid-like fashion, with multiple memory cells connected in series to form a NAND string. Each memory cell within the string stores a single bit of data (either 0 or 1). The fundamental component of NAND flash memory is the floating-gate transistor [2]. This transistor has two gates: a control gate (CG) and a floating gate (FG) as shown in Fig. 1.1. The floating gate is isolated from the other parts of the transistor by a thin insulating layer also called as isolators. The threshold voltage is programmed by storing electrons in Floating gate. The more the number of electrons the higher is the threshold voltage. The data here is stored in the form of electrons in floating gate. This prevent the leakage of electrons isolators are placed.

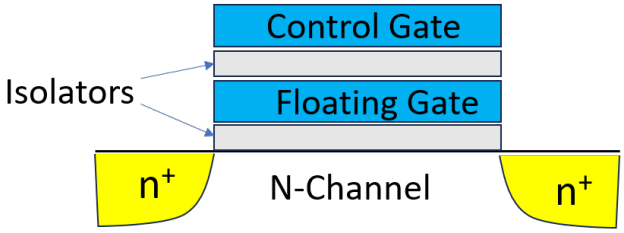

Figure 1.1: Demonstration of a basic NAND Cell with Control and Floating gate

The presence of electrons and the absence of electrons can be considered as two states which can be represented as 0 and 1. Here the states are called Program and Erase states [3]. Programming: To program a NAND memory cell, a higher voltage is applied to the control gate. This voltage is typically referred to as the program voltage (VP). Electrons are injected into the floating gate through a process called hot electron injection. This increases the threshold voltage of the transistor.

Erasing: To erase a NAND memory cell and return it to its default state, a higher voltage called the erase voltage (VE) is applied to the control gate. Electrons are removed from the floating gate, reducing the threshold voltage and returning the cell to a logic 0 state.

In addition to single-level cell (SLC) NAND, there are also multi-level cell (MLC) and triple-level cell (TLC) NAND configurations [4]. These store multiple bits of data in each cell by encoding different threshold voltage levels for each bit. MLC NAND, for example, can store two bits in a single cell by distinguishing between multiple threshold voltage levels as shown in Fig. 1.2. This way the density is further more increased within a compact form factor.

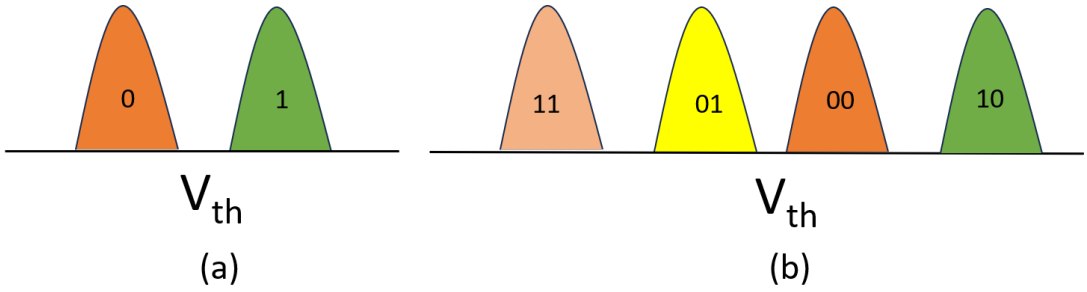

Figure 1.2: (a) SLC storing 1 bit of data with 1 program and 1 erase state, (b) MLC storing 2-bit od data with 3 program and 1 erase state

It is essential to note that the distribution range of the threshold voltage V_{th} remains consistent across various types of NAND flash memory cells, whether it be Single-Level Cell (SLC), Multi-Level Cell (MLC), Triple-Level Cell (TLC), or Quad-Level Cell (QLC). Over time, and with multiple read operations on a NAND cell, there is a potential for the V_{th} distributions to overlap, introducing errors in data retrieval.

To address this issue, Error Correction Code (ECC) [5] becomes a crucial tool in the correction of these distribution overlaps. ECC plays a pivotal role in rectifying errors, ensuring the integrity of the stored data despite the challenges posed by aging and repeated read operations. The data in NAND flash memory is typically stored in the form of gray code, a binary numeral system where only one bit changes at a time between consecutive values. This gray code representation facilitates more straightforward error correction processes, enhancing the reliability of data storage and retrieval.

As a trade-off between density and read time, QLC flash memory offers higher storage density compared to SLC but at the expense of longer read times. The decision between SLC and QLC, therefore, depends on the specific requirements of the application. While SLC is favored for applications where rapid data access is critical, QLC is chosen when maximizing storage capacity is paramount, even if it means sacrificing some read speed. In summary, the choice between SLC and QLC is dictated by the specific needs and priorities of the intended application.

The architectural configuration depicted in Fig. 1.3(a) illustrates the 2D structure of 3D NAND Flash. Within this structure, the crossing point of the word line and bit line represents a memory cell. In the traditional 2D NAND architecture, each plane utilized a separate word line (WL). However, a notable departure occurs in the 3D NAND Flash architecture, as illustrated in Fig. 1.3(b) [6]. In this configuration, all the word lines within a given plane are interconnected.

To elaborate further, this means that in the 3D NAND Flash architecture, the word lines within a plane are not isolated but rather linked together, creating a unified structure. This interconnection of word lines is a distinctive feature of 3D NAND architecture, enabling a vertical stacking of memory cells. In essence, if one were to take these interconnected word line plates and stack them vertically, it forms the basis of the 3D NAND architecture.

This departure from the 2D architecture to the 3D NAND structure is significant in terms of increasing memory density and overcoming some limitations associated with 2D NAND Flash. The vertical stacking of memory cells allows for a more efficient use of space and enhances the overall storage capacity and performance of NAND Flash memory devices.

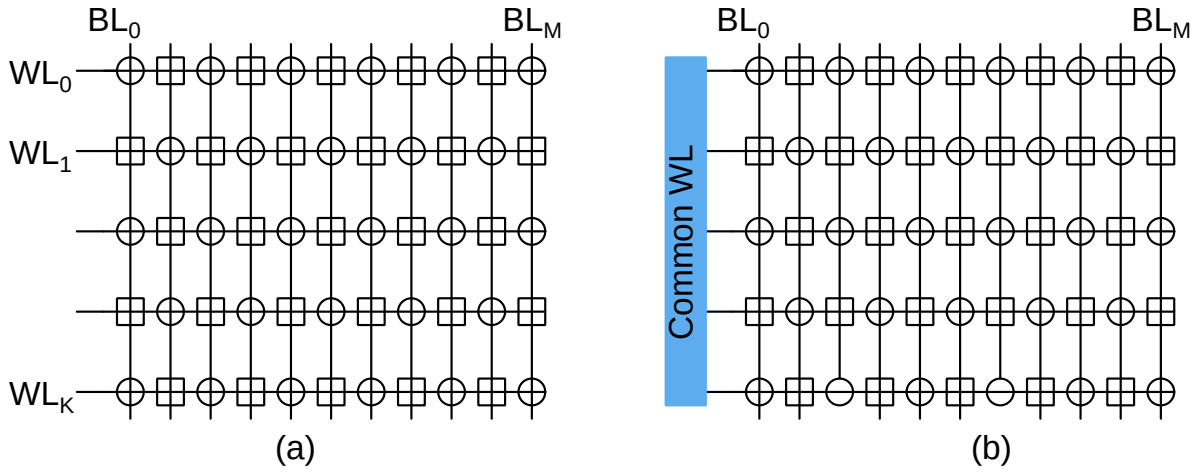

Figure 1.3: Architecture of (a) 2D NAND Flash with (b) 3D NAND Flash

The structure of a 3D NAND Flash memory is illustrated in Fig. 1.4. As each successive generation unfolds, the number of layers in this structure increases [7] [8]. However, this upward trend in layer count corresponds to a rise in effective load capacitance. Consequently,

the analog circuits responsible for driving the WL and BL experience a substantially greater load capacitance. Typically, a Low Dropout Regulator (LDO) is employed to furnish a regulated voltage supply to the WL and BL. It is evident that LDOs steering these BL and WL must exhibit the capability to manage such a significant load capacitance. Furthermore, the design must demonstrate robustness to accommodate additional load capacitance should the layer count increase in future generations. Addressing these challenges, this work introduces a digitally programmable multi-loop-based LDO utilizing a distributed Flipped Voltage Follower (FVF).

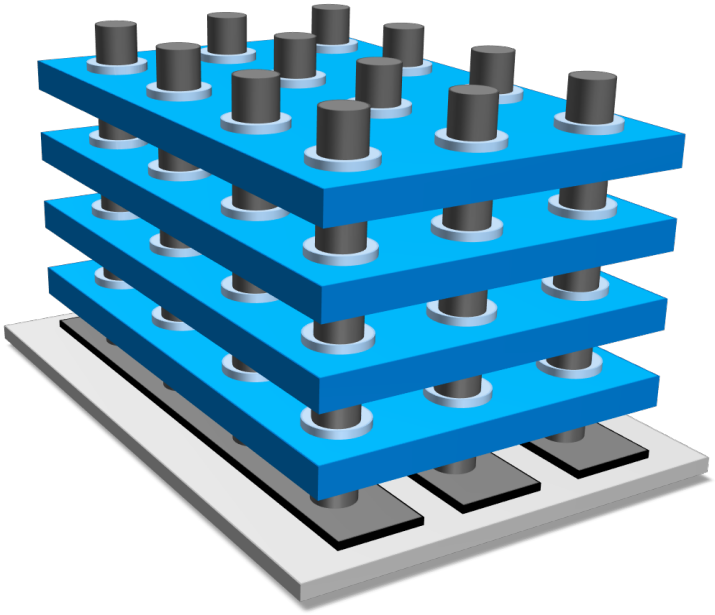

Figure 1.4: Depiction of 3D NAND Memory Array

1.2 Summary of Contributions

The main contribution of this thesis are presented in chapters mentioned below:

- Chapter 2
  - Traditional LDO's and Architecture Selection Factors:
    The chapter thoroughly discusses traditional Low Dropout Regulators (LDOs) and deliberates on the various factors influencing the choice of architecture for these regulators.
  - Issues with traditional architectures in driving large capacitive loads:
    The section delves into the challenges associated with conventional LDO architectures when confronted with the task of driving a substantial capacitive load.

  - Introduction of FVF as a new driver choice:

    A novel approach is presented, suggesting the utilization of the FVF as an alternative driver to efficiently handle and drive large capacitive loads in contrast to traditional architectures.

- Chapter 3

  - Issues with Conventional FVF Structure and Modifications:

    The chapter explores challenges associated with the traditional FVF structure and examines potential modifications that can be applied to enhance its performance.

  - Introduction of first cut programmable FVF driver (using V_{TH} cancellation technique):

    An approach is introduced, presenting the concept of a first-cut programmable FVF driver. This driver utilizes the V_{TH} cancellation technique to enhance its functionality.

  - Addition of trim functionality to counter PVT variations:

    The section proposes modifications that involve incorporating trim functionality at various points to mitigate the impact of Process, Voltage, and Temperature (PVT) variations.

  - Recycled Folded Cascode structure as error amplifier:

    The section discusses the utilization of a Recycled Folded Cascode Structure as the chosen Error Amplifier. This structure is selected for its effectiveness in driving distributed loads.

  - Presentation of programmable V_{TH} cancellation-based scheme:

    The last part of the chapter presents a comprehensive and programmable scheme based on V_{TH} cancellation, offering an effective solution to the challenges discussed in the earlier sections.

- Chapter 4

  - Introduction of a new multi-loop based LDO:

    The thesis introduces a novel multi-loop based Low Dropout Regulator (LDO), providing an innovative design for enhanced performance.

  - Design methodology for multi-loop system stability: The document outlines a comprehensive design methodology for ensuring the stability of a multi-loop system, addressing the intricacies involved in its implementation.

  - Extension of the scheme to drive distributed loads:

    Building upon the proposed multi-loop LDO, the work extends the scheme's application to effectively drive distributed loads, showcasing its versatility.

– Undershoot/Overshoot voltage reduction through Power-Grid structure:

  The thesis proposes a power-grid structure tailored for distributed loads, aiming to further reduce undershoot and overshoot voltages, thereby enhancing overall performance.

– Comparison with State-of-the-Art Design:

  The thesis concludes with a comprehensive comparison between the proposed multi-loop LDO and a state-of-the-art design, evaluating their respective strengths and weaknesses.

1.3 Structure of Thesis

In this thesis, I initially highlight the industry's transition towards innovative memory technologies, particularly the 3D NAND Flash Memory. However, the vertical stacking inherent in this technology poses significant challenges for analog designers striving to devise robust solutions for driving these expansive memory cells. The central focus of this thesis revolves around elucidating the challenges encountered by conventional structures when tasked with steering large memory arrays. Subsequently, the thesis introduces a novel approach aimed at addressing and overcoming these challenges.

- Chapter 2: This section meticulously examines the conventional Low Dropout Regulator (LDO) and underscores the necessity for a new driver in the context of emerging challenges.

- Chapter 3: This chapter introduces a preliminary programmable FVF Driver-based LDO. It delves into strategies to mitigate non-idealities by incorporating various options at different points within the structure. The chapter culminates in the proposition of a programmable and efficient LDO, leveraging a single-loop configuration with V_{TH} cancellation.

- Chapter 4: The final chapter evolves the LDO structure from a single-loop to a dual-loop scheme, demonstrating enhanced transient performance compared to existing configurations. The structure is extended to accommodate distributed loads using a distributed FVF cell connected through a shared Power Grid.

- Chapter 5: This concluding chapter encapsulates the summary of the thesis, offering key insights and findings. It also includes a section on related publications.

Chapter 2

Conventional LDO Regulators and the Need for a New Driver

The essential analog component for any memory system is providing a stable power supply to its associated word and bit lines. LDO regulators find common applications in integrated circuits due to their ability to deliver precise voltage regulation, low dropout voltage, compact dimensions, low noise characteristics, and efficient operation [9]. These attributes make LDO regulators well-suited for diverse on-chip power management tasks, accommodating variations in input voltage and load current requirements. In Figure 2.1, a fundamental model of a dropout regulator is depicted. It is conceptualized as an ideal voltage source. Key criteria for an ideal voltage source include:

- Low output impedance (Ideally Close to 0): Ensuring that the regulator can effectively provide a stable output voltage despite variations in load conditions [10].
- Ripple free output during current switching: The ideal voltage source should maintain a consistent output even when there are fluctuations in the load current, ensuring a stable power supply to the connected components.

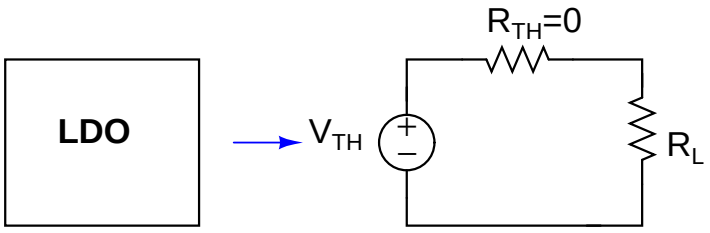

Figure 2.1: Thevnin Model of a Dropout Regulator

Certainly, evaluating the performance metrics of an LDO is crucial for selecting the most suitable one for a specific application[11] [12]. The next section discusses a few performance metrics of LDO that need to be considered before deciding on an architecture choice.

2.1 Key Performance Metrics of a Dropout Regulator

The fundamental metrics on which the performance of an oscillator is decided are:

1. Line Regulation: Line regulation measures how well the LDO can compensate for changes in the input voltage to ensure that the output voltage remains within specified limits [13].

$$LineRegulation = \frac{V_{out,max} - V_{out,min}}{V_{out,nom}} * 100 \tag{2.1}$$

2. Load Regulation: refers to the ability of the LDO to maintain a stable output voltage despite changes in the load current. In other words, load regulation measures how well the LDO can compensate for fluctuations in the current drawn from its output while keeping the output voltage within specified limits.

$$LoadRegulation = \frac{\Delta V_{out}}{\Delta I_{Load}} \tag{2.2}$$

3. Low dropout: A dropout refers to the difference between output voltage and input voltage; the smaller the dropout, the more the efficiency (η) [14]. LDOs with low dropout voltages can extract more usable energy from the battery, as they can operate efficiently even as the battery voltage approaches its minimum allowable level.

4. Output impedance : represents how the regulator's output voltage changes in response to changes in load current. A lower output impedance indicates better regulation and less voltage variation as the load current changes.

5. Stability:Since an LDO has to support various load current profiles, the structure should be stable across the entire range of load current variation and provide a ripple-free output.

6. Settling time indicates how fast the LDO reacts to any change in load current. This is directly proportional to the bandwidth of the LDO.

7. Undershoot voltage refers to a temporary decrease in the output voltage below its final, steady-state value when there is a sudden increase in the load current.

8. Overshoot voltage refers to a temporary increase in the output voltage above its final, steady-state value when there is a sudden decrease in the load current.

9. Power Supply Rejection Ratio (PSRR) quantifies how well the LDO can filter out disturbances on the input voltage and provide a stable output voltage.

$$PSRR(dB) = 20 \log \frac{\Delta V_{out}}{\Delta V_{in}} \tag{2.3}$$

The specified performance criteria will serve as a guide in the selection of the most suitable Low Dropout Regulator (LDO) for our particular applications. Subsequently, we will delve into an exploration of various prevalent circuit configurations utilized in the industry to formulate LDOs. The objective is to scrutinize their compatibility with emerging memory technologies, particularly the challenges posed by 3D NAND Flash Memory.

2.2 Broad Classifications of LDO

LDOs can be broadly classified into two main categories based on the characteristics of the capacitive load they are designed to drive[15]:

1. Output Capacitor Dominant Based LDO (Off Chip)
2. Output Capacitor-less Based LDO

These two classes offer distinct advantages and considerations, and the choice between them depends on the specific requirements and constraints of the application. The nature of the capacitive load, desired transient response, and overall system design goals will influence the selection of the appropriate LDO class.

2.3 Off-Chip Load Capacitor based LDO and its Characteristic

The structure of an Off-Chip Capacitor based LDO is illustrated in Figure 2.2. In this simplified representation, the capacitor is deliberately depicted as being physically distant from the Load Model I_{LOAD}, symbolizing its location off-chip. The placement of the capacitor off-chip implies that typical capacitor values for this configuration are in the range of very large capacitance, often in the nF or μF range. The working of off-chip Capacitor LDO is explained below:

- Output Capacitor (Off-chip): Instead of relying solely on an on-chip capacitance, an off-chip capacitor with a larger capacitance value is employed. This external capacitor is connected in parallel with the LDO's output as shown in Fig.2.2.
- Dominant Pole: The external output capacitor introduces a dominant pole into the LDO's control loop. This ensures that the system remains inherently stable by making the system effectively work as a first order system.
- Stability and Compensation: Designers need to carefully select the value of the external output capacitor and possibly add compensation components (such as a series resistor to add an zero) to ensure the LDO remains stable under various load conditions and input voltage variations.

- Load transient response : A larger capacitance value generally improves the regulator's ability to handle load transients and provide stable output voltage.

- Scalability problems : This is not suitable for memory array applications as you need multiple drivers across the chip. This makes this scheme unsuitable for such applications.

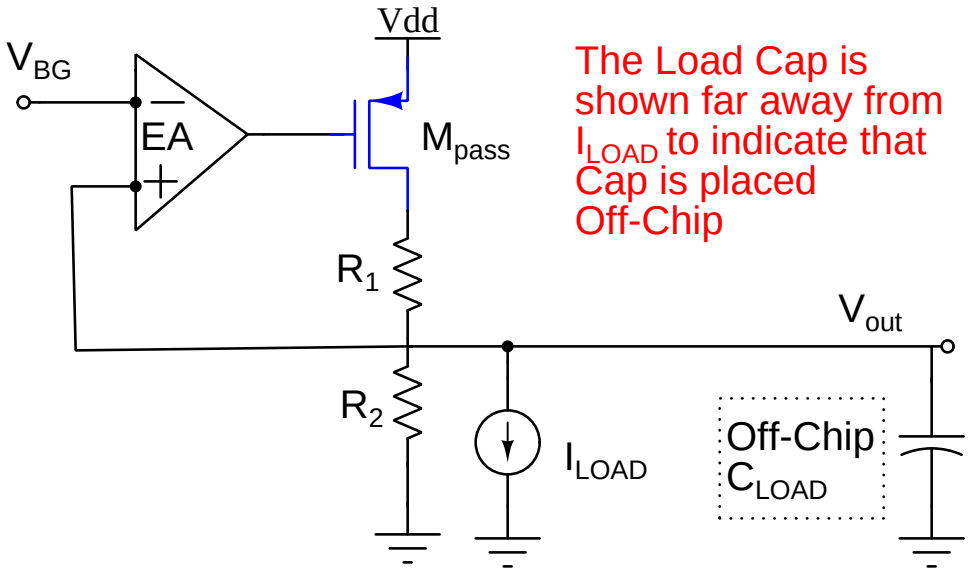

Figure 2.2: Output Capacitor Dominant Based LDO

In summary, an Output Capacitor Dominant Pole (OCDP) based LDO relies on an external output capacitor to dominate the regulator's pole, affecting its bandwidth and transient response. The adoption of 3D stacking for memory arrays might seem advantageous in terms of increased load capacitance. However, this design approach encounters challenges, notably in the following aspects: Scalability challenge: The issue stems from the lack of scalability as the number of tiers increases. This significantly upsurges in the effective load capacitance (C_{LOAD}). As C_{LOAD} expands with each generation, the bandwidth of the LDO regulator diminishes. Consequently, a continual redesign of the circuit becomes necessary, demanding additional power to enhance the bandwidth.

In essence, the bandwidth of the LDO determines how quickly it can respond to changes within its circuit. For the reasons outlined, these design approaches prove unsuitable for the evolving 3D NAND Flash memory technology. Consequently, our focus will shift toward the second type of architecture: Output Capacitor-Less (OCL) based LDO design.

2.4 Output Capacitor-less LDO (OCL-LDO)

An Output Capacitor-Less (C-Less) LDO is specifically engineered to function without an off-chip capacitor or with minimal capacitance. The notable advantages it brings include: i) reduction in area requirements, ii) enhancement of settling behavior in the LDO, and iii) facilitation of monolithic integration[16]. Within the industry, there are two primary architectural approaches widely employed [17]:

- PMOS Driver Based LDO
- NMOS Driver Based LDO

In the upcoming analysis, we will thoroughly evaluate both driver types to determine which structural configuration holds the greatest potential for our specific application. It's crucial to note that an LDO comprises two pivotal components: the error amplifier and the driver [18]. The selection of the error amplifier significantly influences the design decision, with options for either an NMOS input pair operational transconductance amplifier (OTA) or a PMOS-based OTA. This gives rise to four distinct LDO design architectures:

1. PMOS input pair based Error Amplifier with PMOS Driver (Design-1)
2. NMOS input pair based Error Amplifier with PMOS Driver (Design-2)
3. PMOS input pair based Error Amplifier with NMOS Driver (Design-3)
4. NMOS input pair based Error Amplifier with NMOS Driver (Design-4)

In the upcoming sections, we will delve into the intricacies of these structural aspects, exploring methods for selecting a suitable driver, and outlining criteria for determining the appropriate error amplifier choice.

2.4.1 Analyzing PMOS Driver Based LDO (Design 1 and Design 2)

In Figure 2.3, two variants of the PMOS Driver-based LDO are presented. The Error amplifier is implemented using a conventional 5 Pack OTA. The choice of the OTA depends on the input common range, where a PMOS input pair OTA is effective for low voltages, and an NMOS input pair OTA is suitable for higher input voltages. Assuming that V_{in} applied is within the input common mode range of both structures, the decision becomes nuanced. To evaluate these structures' performance concerning power supply variation, we will analyze Figure 2.3(a).

In Figure 2.3(a), if the supply voltage V_{DD} increases, the tail node of the PMOS input pair sees no change as it is an incremental short node in a small signal sense. The fully differential amplifier ensures that it rejects common-mode noise, and consequently, the error amplifier sees

no incremental change at the output. However, if we examine M_{pass}, its source yanks up, and the gate is constant in a small signal sense. Therefore, the PMOS sees an incremental $V_{SG,_{pass}}$, which is amplified by $g_{m,PASS}$ to change the output voltage. Hence, this configuration is susceptible to supply variations [19].

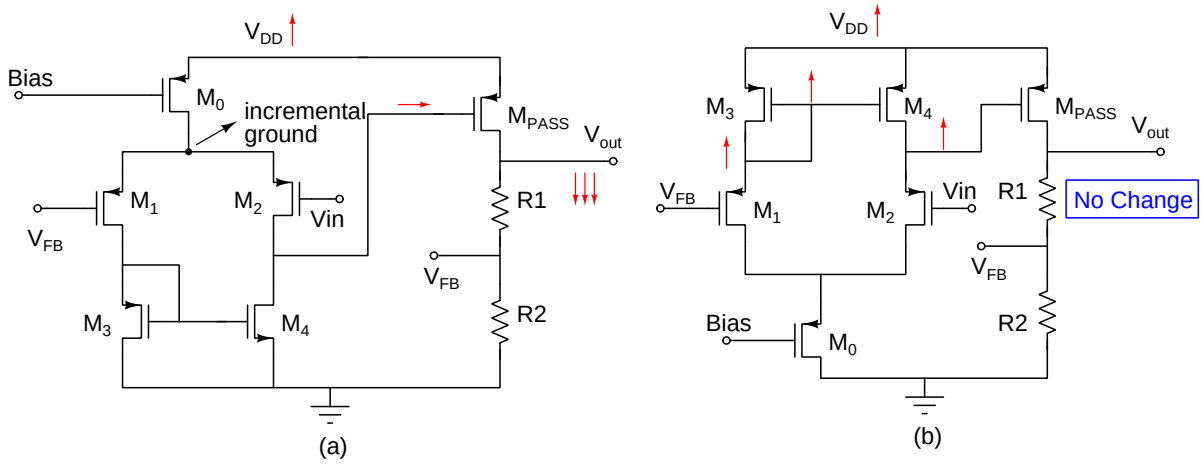

Figure 2.3: (a) PMOS Input Pair OTA with PMOS driver and (b) NMOS Input pair OTA with PMOS Driver

Contrastingly, in Figure 2.3(b), if V_{DD} increases, the gate voltage of M_3 and M_4 both rise due to the symmetric nature of the OTA. Notably, the pass gate M_{pass} experiences both source and gate voltages increasing, resulting in zero incremental $V_{SG,_{pass}}$. Therefore, this structure is more resilient against power supply variations.

In conclusion, for a PMOS Driver-based LDO, the NMOS 5-pack OTA is preferred over the PMOS-based OTA due to its superior protection against power supply variations [20].

2.4.2 Analyzing NMOS Driver Based LDO (Design 3 and Design 4)

Fig. 2.4 shows both the configurations available for an NMOS driver-based LDO. In order to analyze which input pair suits the NMOS driver, we will perform the same test again as discussed above. Here, as shown in Fig. 2.4(a), if we yank V_{DD} up, then there is no incremental change at the drain of M_0. The reason is that the same differential pair rejects the common mode signal. As a result, the gate of the NMOS driver sees no change, as shown in Fig. 2.4(a). Although the drain of the NMOS driver is changing, V_{GS} is not changing. Thus, for an NMOS driver, PMOS input pair OTA is useful for suppressing supply noise variations. However, the structure shown in Fig.2.4(b) is susceptible to power supply variations [21]. This is because as V_{DD} yanks up, OTA output also yanks up. This ensures an incremental V_{GS} of NMOS pass driver, which is undesired. As power supply variations flow to the output of LDO.

The above analysis underscores the pivotal role played by the choice of the input pair in the error amplifier design. Beyond this, it's crucial that the error amplifier's gain is sufficiently high to control the feedback node tightly. In this regard, the Cascode Topology proves advantageous as it provides a significantly larger gain compared to the 5-Pack OTA. Furthermore, the Cascode Topology eliminates dependence on supply noise, further justifying its selection as the preferred choice for an Error amplifier.

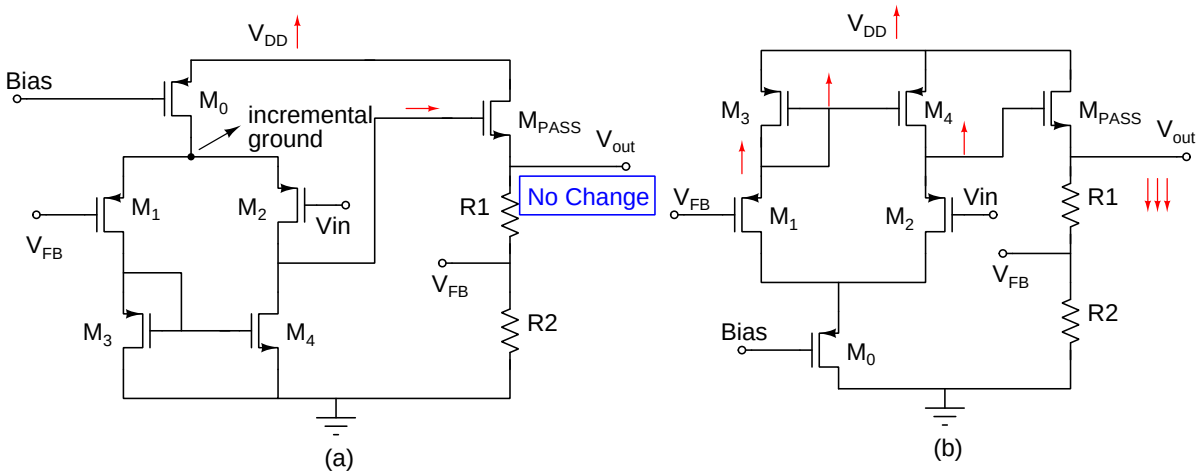

Figure 2.4: (a)PMOS Input Pair OTA with NMOS driver and (b) NMOS Input pair OTA with NMOS Driver

The next section discusses about how removing the dependency of choice of error amplifier for a robust design.

2.5 Reducing the Dependency of Error amplifier and Developing Intuition for Improved Transient Response

As presented in the above section, the choice of input pair in a conventional 5-pack OTA determines the performance of an LDO. However, using a conventional folded cascode amplifier removes the dependency of the choice of input pair. The conventional folded cascode structure doesn't add any extra pole and gives a much better gain steady state than its counterpart. For these reason, we will be using a conventional folded cascode in our design as a choice of an error amplifier [22]. To demonstrate this, we have simulated Design -1 and Design-2 with two different cascode input pair. The results shows that PSRR is now only a function of Loop Gain $A\beta$ and does not depend on the architecture.

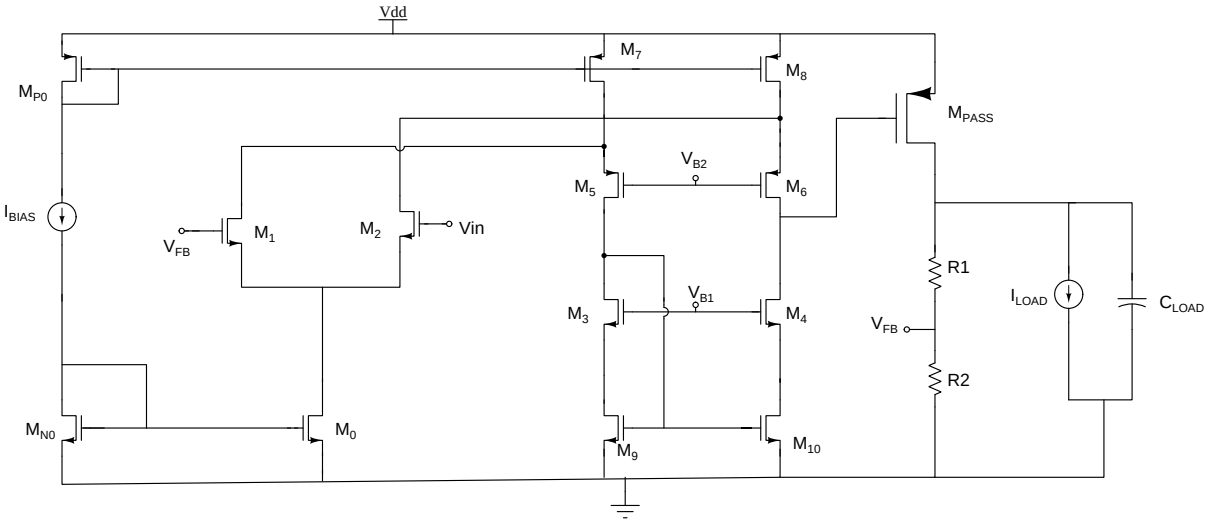

Figure 2.5: NMOS Input Pair based Error amplifier with PMOS driver

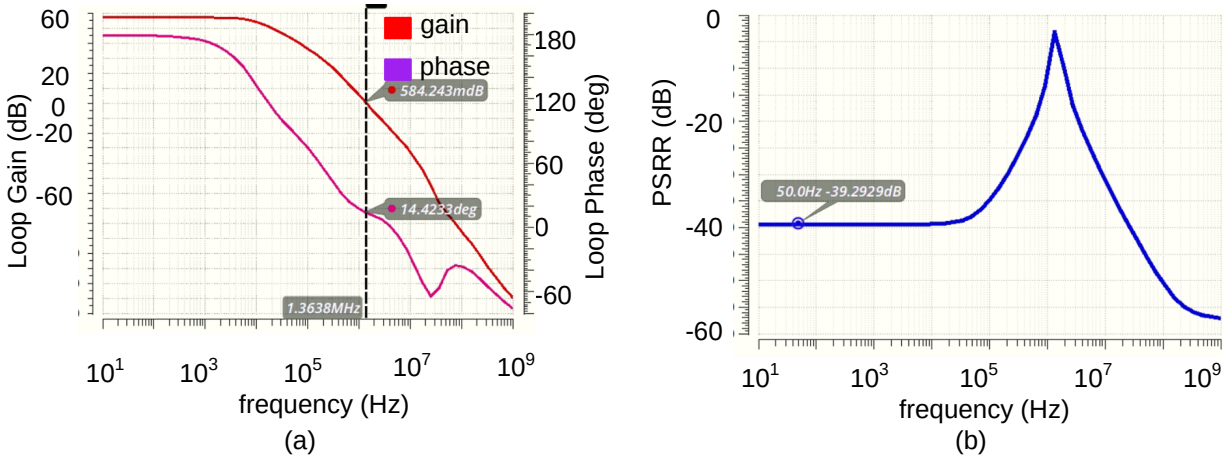

Figure 2.6: (a)NMOS Input Pair based Error amplifier with PMOS driver for low load of 10 nA (b) PSRR response at low load

Fig. 2.5 illustrates the structure with an NMOS Input Pair amplifier (cascode) [23] and PMOS Driver (Design-1). In this configuration, the Op-amp consumes a bias current of 1 μA. The PMOS driver sources a current of approximately 1 μA at no load and a current of 10 mA. Fig. 2.7(a) displays the magnitude and phase response of the system under low load conditions. The system's bandwidth at this point is close to 1.3 MHz, and the phase margin is around 14.3 degrees. The PSRR plot at low load is depicted in Fig. 2.7(a). At maximum load, the system's bandwidth increases to 8 MHz with a phase margin of 42 degrees, as shown in Fig. 2.8(a). The

corresponding PSRR plot is represented in Fig. 2.8(b). It is evident that PSRR is dependent on Loop Gain. The higher the Loop Gain, the better the PSRR.

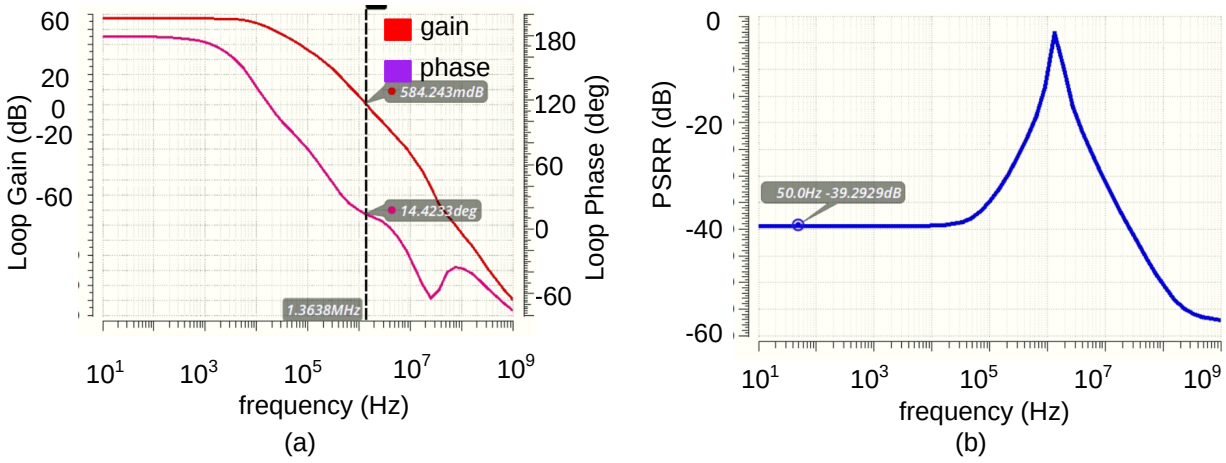

Figure 2.7: (a)NMOS Input Pair based Error amplifier with PMOS driver for low load of 10 nA (b) PSRR response at low load

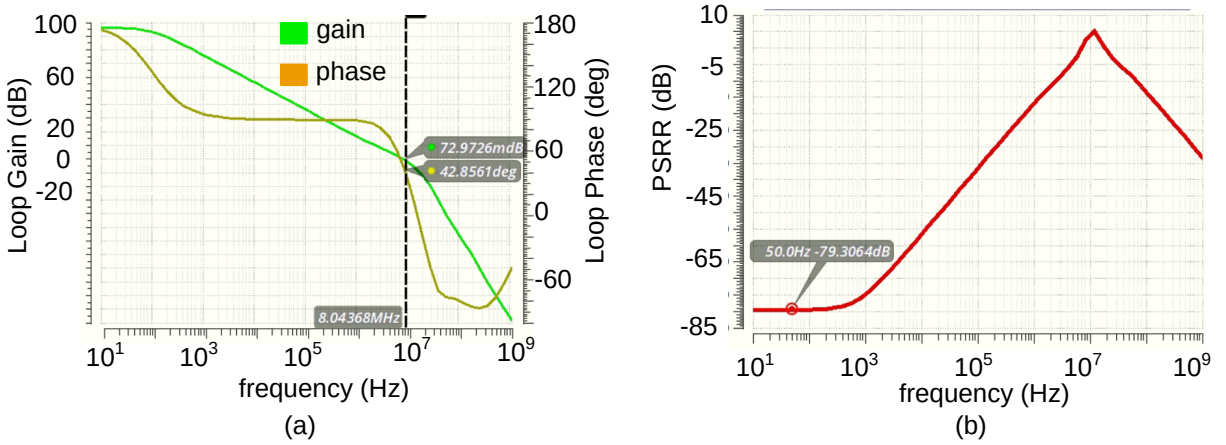

Figure 2.8: (a) NMOS Input Pair based Error amplifier with PMOS driver for a max load of 10 mA (b) PSRR response at max load

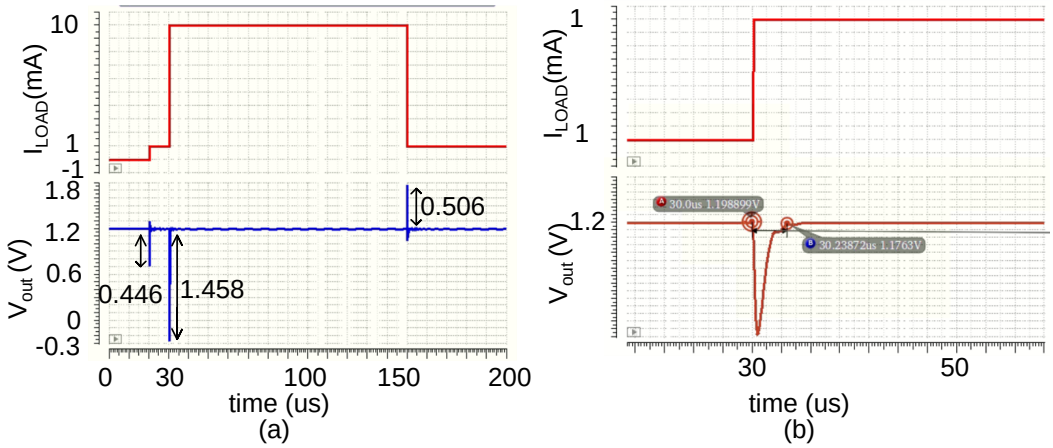

Figure 2.9: (a) Transient Response of Design-1 with 10ns rise time (b) Zoomed-in version of transient response shown in (a)

Fig. 2.9 displays the transient response of Design-1 with an I_{LOAD} ranging from 1 to 10 mA for a rise time of 10 ns. The settling time is approximately 238 ns in the absence of C_{LOAD}, as illustrated in Fig. 2.9(b).

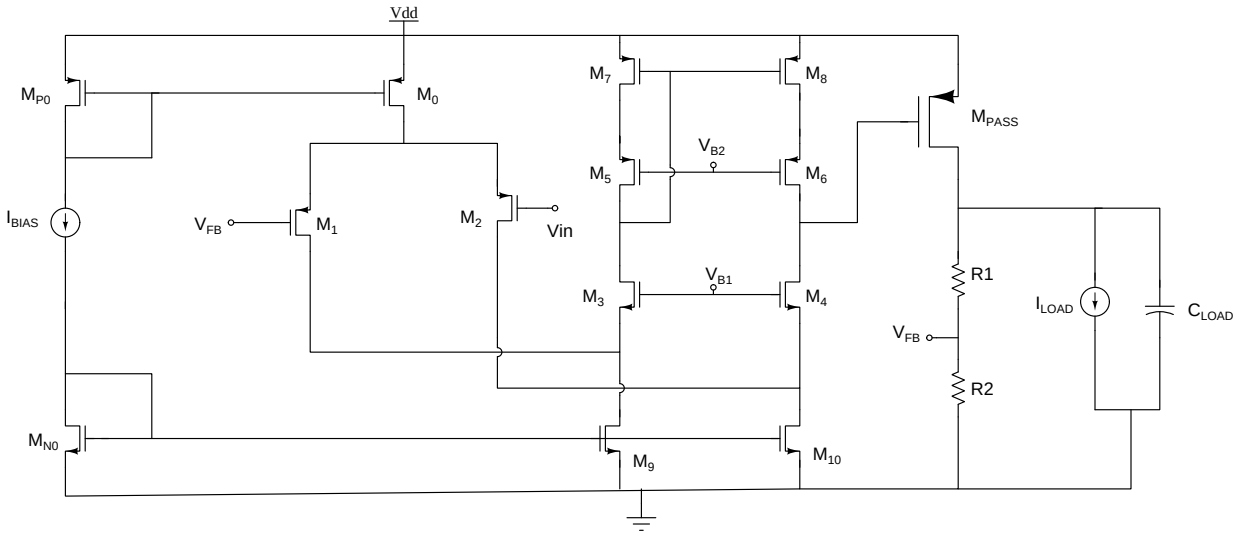

Figure 2.10: PMOS Input Pair based Error amplifier with PMOS driver

Fig. 2.10 shows the structure of with PMOS Input Pair amplifier (cascode) [23] with PMOS Driver (Design-1). Here the Op-amp consumes a Bias current of 1 μA. The PMOS driver source a current of around 1 μA at no load and a current of 10 mA. Fig. 2.11(a) shows the magnitude and phase repose of the system at low load conditions. The Bandwidth of the system is close to 1.3 MHz and the Phase Margin of the system is around 17.9 degrees. Th PSRR Plot at low

load is represented in Fig. 2.11(b). At Max. Load the Bandwidth of the system increases to 8 MHz with the Phase Margin of 80 degrees as shown in Fig. 2.12(a) The corresponding PSRR plot is represented in Fig. 2.12(b). It is again evident that PSRR is a function of Loop Gain. This again shows that more the Loop Gain the better the PSRR.

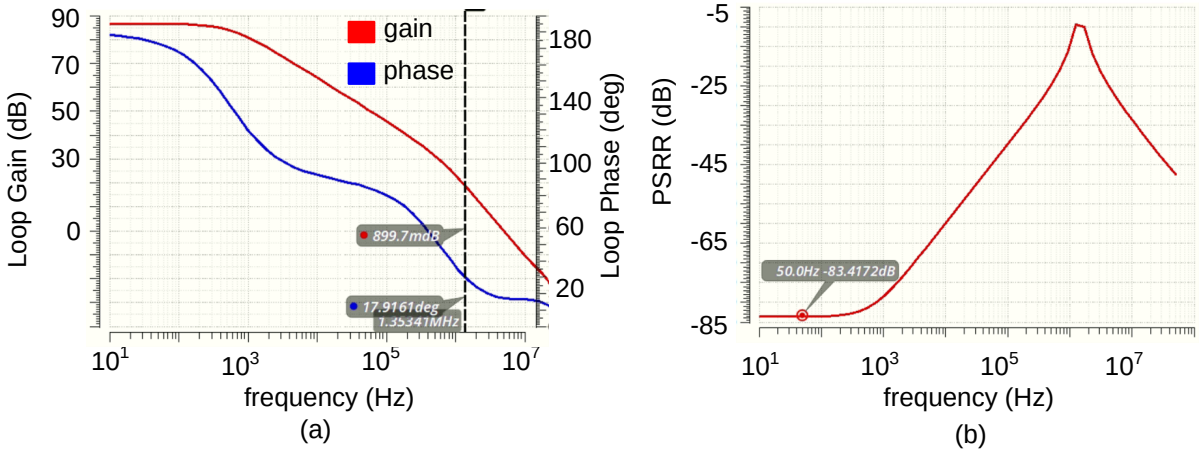

Figure 2.11: PMOS Input Pair based Error amplifier with PMOS driver for low load of 10 nA

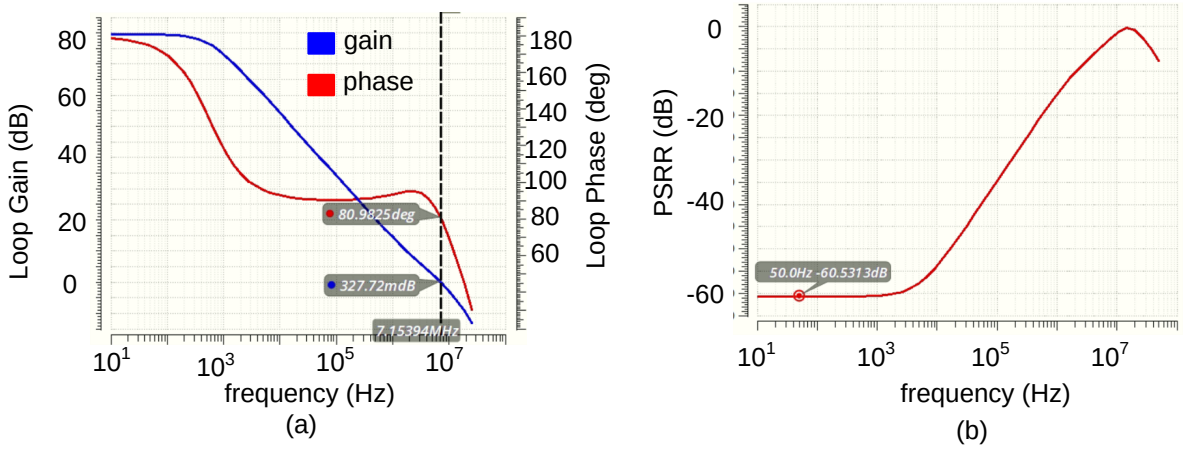

Figure 2.12: PMOS Input Pair based Error amplifier with PMOS driver for a max load of 10 mA

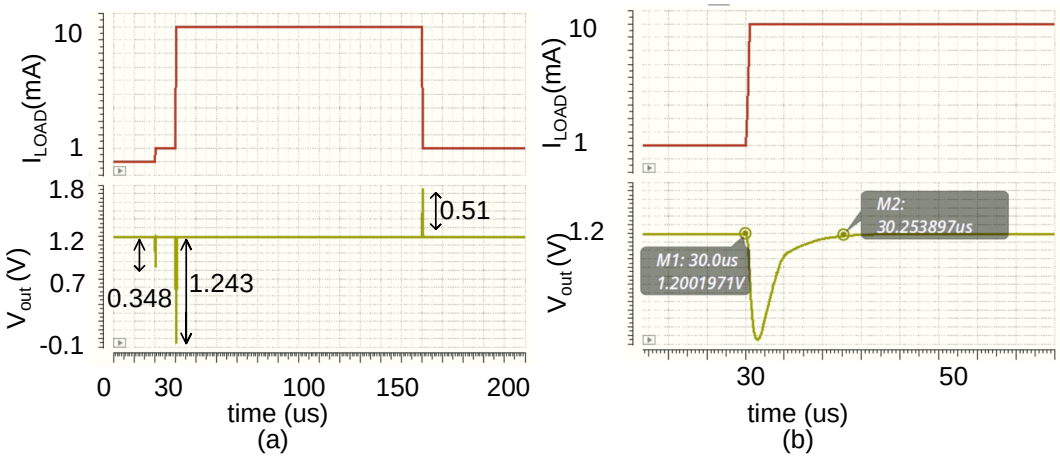

Figure 2.13: PMOS Input Pair based Error amplifier with PMOS driver

Fig. 2.13 shows the transient response of Design-1 for an I_{LOAD} varying from 1 to 10 mA for a rise time of 10 ns. The settling time is around 253 ns for no C_{LOAD} as shown in Fig. 2.9(b). Clearly, the greater the bandwidth, the better the response for the system. This is clearly the indicator for a faster settling behavior of LDO. Nevertheless, both these structures and the NMOS Driver-Based Structure face certain challenges, which will be explored in the following section. The section suggests an FVF-Based Driver as an appropriate alternative for the driver.

2.6 Motivation for new driver

In the above sections, we have discussed the fundamental structures used when designing an LDO. However, these structures suffer from certain limitations while driving a very large distributed load like that of a memory array. The limitations will be explored in this section.

In Fig. 2.14(a), a PMOS pass transistor is utilized to drive the load. However, since the PMOS pass transistor is arranged in a common-source (CS) configuration, the effective capacitance at the output of the error amplifier increases due to Miller multiplication. Consequently, both poles, namely the output pole and the inner pole (pole at the output of the error amplifier), become comparable. This has the potential to induce instability in the system. Nonetheless, the NMOS pass transistor depicted in Fig. 2.14(b) doesn't encounter this issue. Since the NMOS pass transistor is configured in common-drain (CD) mode, there is minimal Miller multiplication. Additionally, the NMOS driver provides a low output impedance $R_{out} = \frac{1}{g_{m,pass}}$, which widens the gap between the output pole and the inner pole. Consequently, the NMOS driver-based LDO proves to be a more stable option compared to its PMOS-based counterpart. However, the NMOS-based driver is not the preferred choice in applications where a low dropout is necessary.

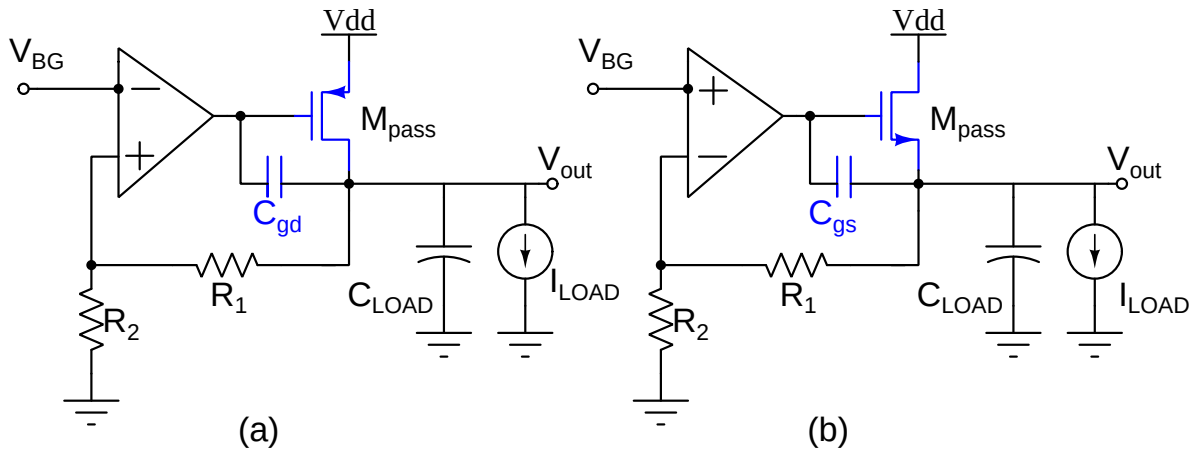

Figure 2.14: Conventional (a)PMOS and (b) NMOS driver based LDO, where V_{BG} is bandgap-voltage.

This is attributed to the higher gate voltage required to turn on the NMOS pass transistor. Typically, a charge pump is inserted between the error amplifier (EA) and NMOS pass transistor [24] [25] to supply the required high voltage to the pass transistor's gate. This, however, introduces noise due to continuous capacitor switching and also imposes additional area requirements [26]. Another approach to employing an NMOS driver-based LDO without a supplementary charge pump is by effectively using two different supplies. One, denoted as V_{high}, biases the error amplifier, and the other, denoted as V_{low}, provides potential at the drain of the NMOS driver, as illustrated in Fig. 2.15. This configuration ensures effective NMOS device activation for supplying large currents. However, it comes at the expense of utilizing two supplies, increasing routing overhead.

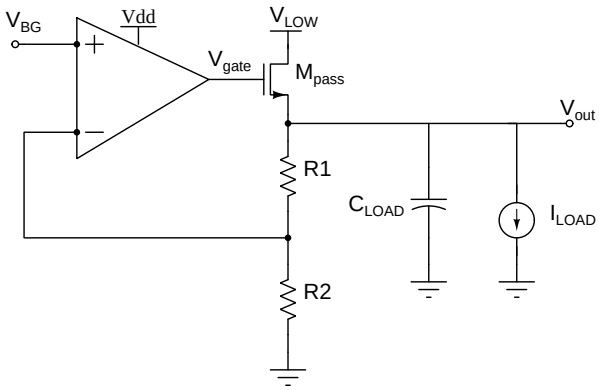

Figure 2.15: NMOS Driver with Dual Supply to ensure drivers turns on fully without external charge pump.

Furthermore, if conventional techniques are applied to applications like driving very large capacitive loads, more power must be consumed to achieve a larger bandwidth, which is undesirable. This makes the conventional structures not suitable for driving large capacitive loads. This motivates the exploration of a new structure that offers a significantly larger bandwidth without requiring additional blocks like charge pumps in the signal path. To address these issues, a Flipped Voltage Follower cell is employed in designing an LDO with a faster transient response, which will be discussed in the next chapter.

2.6.1 Flipped Voltage Follower: Obvious Choice for Driver

A Flipped Voltage Follower cell can be seen as a better substitute of common-drain stage [27]. The reason being a low impedance node is a preferred choice is because of a continuous increase in the load capacitance value. This effectively ensures that one can drive a much larger load cap and still ensures that the output pole remains of of unity gain bandwidth [28]. (Pole frequency$\omega_p = \frac{1}{RC}$) Thereby, not disturbing the LDO performance metrics such as speed, settling time, stability etc. Fig. 2.16 shows a comparison of a common drain stage and FVF cell. First obvious difference that is observed in two cases is the position of current source. In common drain stage the current source position is at the source of mosfet whereas in the FVF cell the position of current source is at the drain terminal. Since the position of current source is flipped thereby the term Flipped comes in the nomenclature of Flipped voltage follower. The second obvious difference that can be seen from the two structure is that common drain configuration is an open loop structure. However, the FVF cell is connected in a feedback fashion. The nature of feedback can be calculated by breaking the loop and performing the analysis. The transistor M_{Pass} is configured as common-source stage (CS) thus providing a phase change. The transistor M_1 is configured as common gate stage thus doesn't modify the phase. Since there is one sign change from input to output thus this feedback is configured in a negative feedback configuration.

The advantages that the structure offers because of negative feedback fashion is reduction in output impedance. The structure offers a comparatively low impedance as compared to its common drain counterpart.

$$R_{out,FVF} = \frac{1}{g_{m,1} g_{m,pass} r_{o,1}} \tag{2.4}$$

which is comparatively much smaller as compared to the common-drain (CD) stage.

$$R_{out,CD} = \frac{1}{g_{m,1}} \tag{2.5}$$

This can be intuitively calculated as in a Voltage-Voltage feedback configuration the closed loop Output Impedance reduces and is given by :

$$R_{out,CL} = \frac{R_{out,OL}}{1 + LG} \tag{2.6}$$

where open loop output impedance $R_{out,OL}$ and Loop Gain (LG) is given by

$$R_{out,OL} \approx \frac{1}{g_{m,1}} || r_{o,pass} \tag{2.7}$$

$$LG = -g_{m,pass}[r_{o,ref} || g_{m,1} r_{o,1} r_{o,pass}] \tag{2.8}$$

where $r_{o,ref}$ is the output impedance of current source I_{ref}.

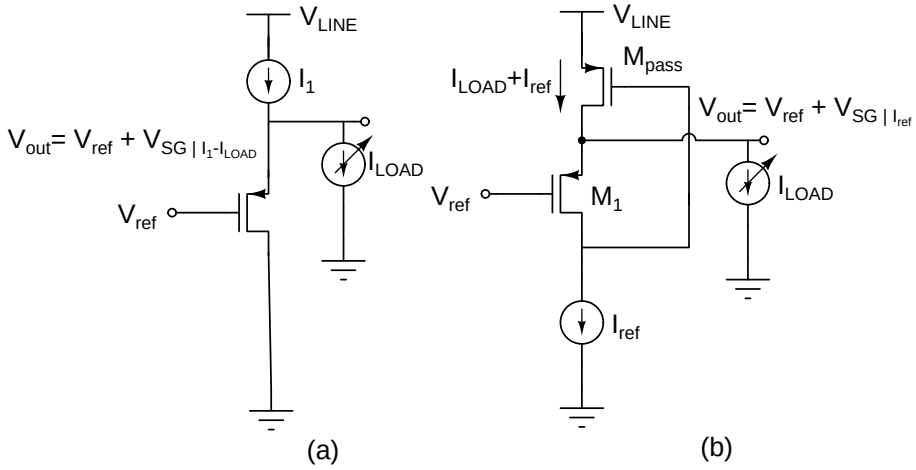

Figure 2.16: Standard Flipped Voltage Follower Cell

The preceding analysis provides a mathematical quantification of why the flipped voltage follower is a superior choice for a voltage buffer compared to its counterpart. This can be intuitively grasped from Fig. 2.16(a) and (b). In the Common drain configuration the current through M_1 is not fixed . Consequently, the output voltage is expressed as:

$$V_{out} = V_{ref} + V_{SG|_{I_1 - I_{LOAD}}} \tag{2.9}$$

On the other hand, the FVF cell's output voltage is not a function of load current, as the current through M_1 is always fixed, i.e., I_{ref}.

$$V_{out_{FVF}} = V_{ref} + V_{SG|_{I_{ref}}} \tag{2.10}$$

Given that any alteration in a low-impedance node can impact circuit performance, the MOSFET M_1 is meticulously regulated by employing the constant current I_{ref}. Consequently, the structure depicted in Fig. 2.16(b) delivers superior performance compared to the structure shown in Fig. 2.16(a).

The FVF structure appears to be a suitable choice for driving large capacitive loads due to its significantly smaller output impedance. However, designers encounter certain design challenges when employing this FVF driver. The subsequent chapter delves into the modifications made to the standard Flipped Voltage Follower cell and explores the creation of an LDO using these modifications.

Chapter 3

Programmable FVF Based LDO using V_{TH} cancellation

In the preceding chapter, we explored various LDO architectures and highlighted their limitations for applications such as large memory arrays. Subsequently, we discussed the Flipped Voltage Follower (FVF) cell as an alternative to conventional drivers.

The FVF structure, owing to its negative feedback configuration, provides significantly lower impedance. This characteristic facilitates the extension of the output pole to much higher frequencies without necessitating an increase in bias current, as compared to a common-drain output for the same capacitive loads. This inherent improvement in system stability eliminates the need for multiple compensation techniques to maintain stability.

Another advantage offered by the FVF structure is that the voltage gain from V_{ref} to V_{out} is given by:

$$\frac{v_{out}}{v_{ref}} = \frac{g_{m,1}g_{m,pass}r_{o,1}r_{o,pass}}{1 + g_{m,1}g_{m,pass}r_{o,1}r_{o,pass} + g_{m,pass}r_{o,pass}} \tag{3.1}$$

Assuming that all the transistors are biased in saturation region i.e. $g_{m,1}r_{o,1} >> 1$ and $g_{m,pass}r_{o,pass} >> 1$ gives the voltage gain from V_{ref} to $V_{out} \approx 1$.

Nonetheless, the basic FVF structure depicted in Fig. 3.1(a) encounters certain design constraints, which will be addressed in the following section along with the proposed design modifications to overcome these issues.

3.1 Limitations of standard FVF cell and need for modified FVF Cell

Although the standard FVF cell shown in Fig. 3.1(a),(b) seems to have solved the problems possessed by PMOS and NMOS driver. However, the structure is suitable for low voltage applications [29],[30]. At high voltage conditions where low dropout is not a concern, this causes an issue. To understand this we will analyse the structure shown in Fig. 3.1 (a) and Fig. 3.1(b) with light load and heavy load, respectively. For ease of analysis we will put some numbers lets say the supply $V_{line} = 1.8$ V , $V_{ref} = 0.5$ V and $V_{out} = 1.2$ V.

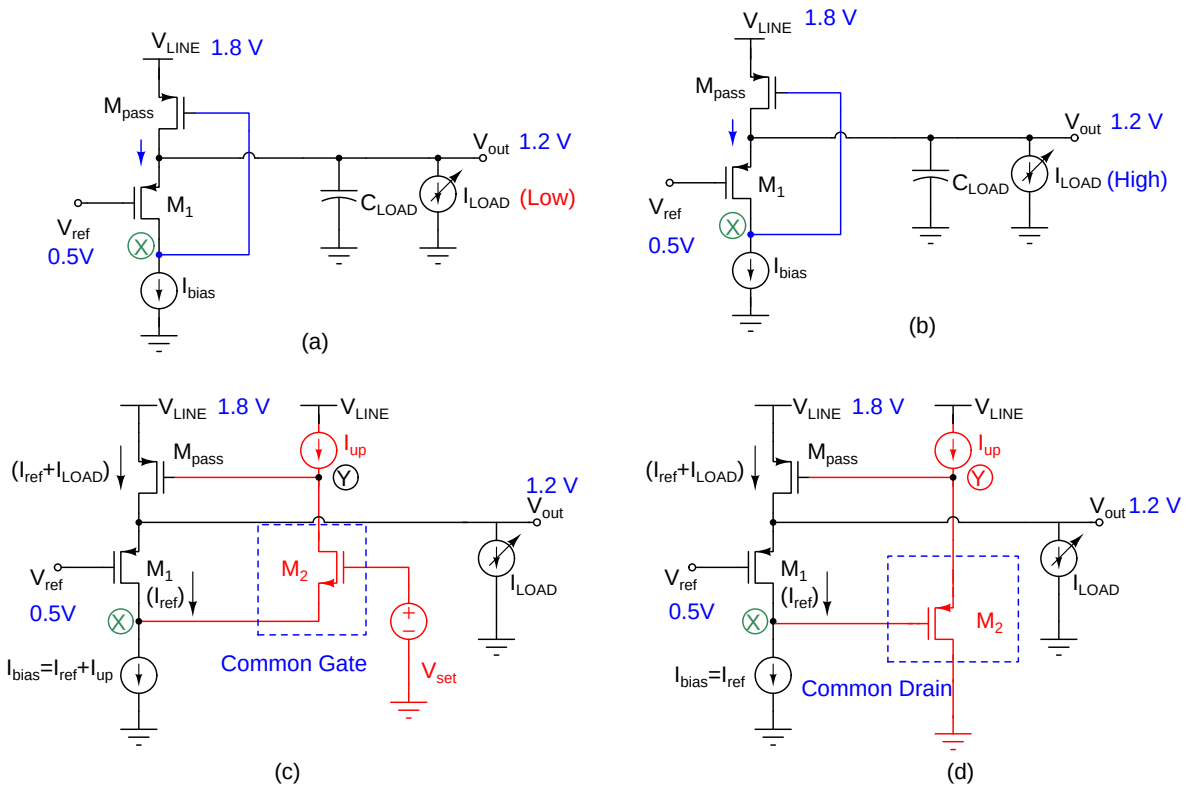

Figure 3.1: Conventional FVF Structures working at (a) Low Load and (b) High Load Modification in FVF cell by adding (c) NMOS CG stage and (d) PMOS CD stage

At light loads, current requirement is low as a result $V_{SG,pass}$ requirement would be less. So, if the pass device is oversized the terminal node X wouldn't go down and as a result the transistor M_1 can go out of saturation region. To avoid this one should reduce the size of pass device.

$$V_x < V_{ref} + V_{th|_{M_1}} \tag{3.2}$$

Now, with the reduced pass device if the load requirement increases. This would cause the node X to go down much further. This causes the current source to go out of saturation.

$$V_x = V_{line} - V_{SG|_{I,pass}} > V_{D,sat|I_{bias}} \tag{3.3}$$

$$V_{out} = V_{ref} + V_{SG}|_{I_{ref}} \tag{3.4}$$

Thus, the analysis we performed for lower output impedance offered by the structure won't work anymore. As this was based on the assumption that all the mosfets are operating in the saturation region.

3.2 Factors affecting the choice between modified FVF drivers

In the previous section, we discussed the drawbacks of conventional FVF cells. The issue exists because the M_{pass} directly affects node X depending on load current changes. This problem can be solved if we somehow remove the dependence of node voltage X from M_{pass}. To solve this, we have two different approaches, i.e. (i) add an NMOS CG as shown in Fig. 3.1 (c) [31] or (ii) add a PMOS CD stage as depicted in Fig. 3.1 (d). To determine the preferable choice between Fig. 3.1(c) and Fig. 3.1(d), we will conduct a comprehensive analysis.

Firstly, since an FVF structure operates on the principle of negative feedback, a higher Loop Gain implies tighter control over the system. Clearly, incorporating a Common Gate stage introduces a gain factor compared to a Common Drain stage. Hence, the structure shown in Fig. 3.1(c) appears to be a promising choice. Additionally, the structure in Fig. 3.1(d) reduces the effective resistance at the gate of the pass transistor, causing the two poles to come closer. Therefore, the circuit shown in Fig. 3.1(c) is the preferred choice. With this modified FVF structure, as illustrated in Fig. 3.1(c), we will delve into the design of an LDO that fulfills the following criteria:

- Ability to drive large capacitive loads.
- Absence of the need for external blocks like charge pumps.
- Provision of a scalable solution for driving distributed loads across the chip.
- Lower power consumption compared to conventional architectures.

3.3 First Cut Design on an LDO with effective V_{th} cancellation

As observed in the previous section, the input to an FVF structure is directed to a PMOS gate. The resulting output from the structure can be expressed as:

$$V_{out} = V_{BG} + V_{sg}|_{I_{ref}} \tag{3.5}$$

where V_{BG} is a constant voltage coming from a bandgap circuit. Nevertheless, a crucial requirement for any LDO is to furnish a constant output voltage regardless of Process, Voltage, and Temperature (PVT) variations. However, the term V_{SG}, it is imperative to cancel this term from the equation. One approach to achieve this is illustrated in Fig. 3.2. In this configuration, the input supplied to the FVF structure is $V_{BG} - V_{SG}$ [32]instead of V_{BG}. To achieve effective V_{SG} cancellation, it is essential to ensure that the current density through the MOSFETs M_{1a} and M_{1b} should be same[33]. This results in an output voltage equal to :

$$V_{out} = V_{BG} \tag{3.6}$$

Now, let's assess whether the circuit fulfills all the requirements for our ideal choice of LDO:

- Capability to drive large capacitive loads: Since the output cap is connected at the output node of FVF. Therefore, it can drive a large capacitive load.
- Absence of external blocks like charge pumps: The input goes to PMOS; therefore, no voltage boosting is needed for proper functionality.
- Scalable solution for driving distributed loads: Since the circuit doesn't require any additional blocks, thus this can be used to drive multiple instances of FVF driver across the chip. Thus providing a scalable solution.

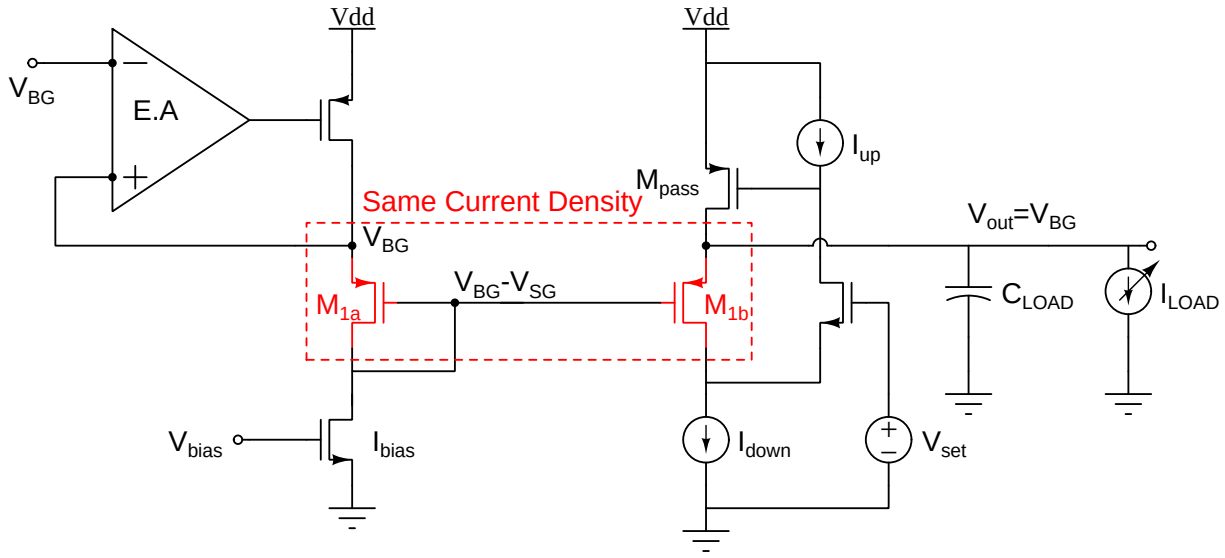

Figure 3.2: First-cut FVF Based LDO with effective V_{th} cancellation scheme[34]

However, there are 2 limitations still exist in the structure.

- A single error amplifier driving multiple FVF driver instances.

One error amplifier can be used to drive multiple FVF driver instances to reduce power consumption. However, the slew rate reduces at the output of the error amplifier as the number of FVF drivers increases. The next subsection discusses how to tackle this issue.

- No Programmable option to change the output Voltage.

The output voltage is fixed i.e. $V_{out} = V_{BG}$ as shown in Eq. 3.6. This is an major issue because the circuit relies on exact V_{TH} cancellation of mosfet. Any variations in V_{TH} because of Monte-Carlo (MC) variations would directly come at the output. In order to bring back circuit to its required voltage level one must add trim options. In the below subsections we will visit different methods to add programmable options.

3.3.1 Choice for error amplifier in driving distributed loads

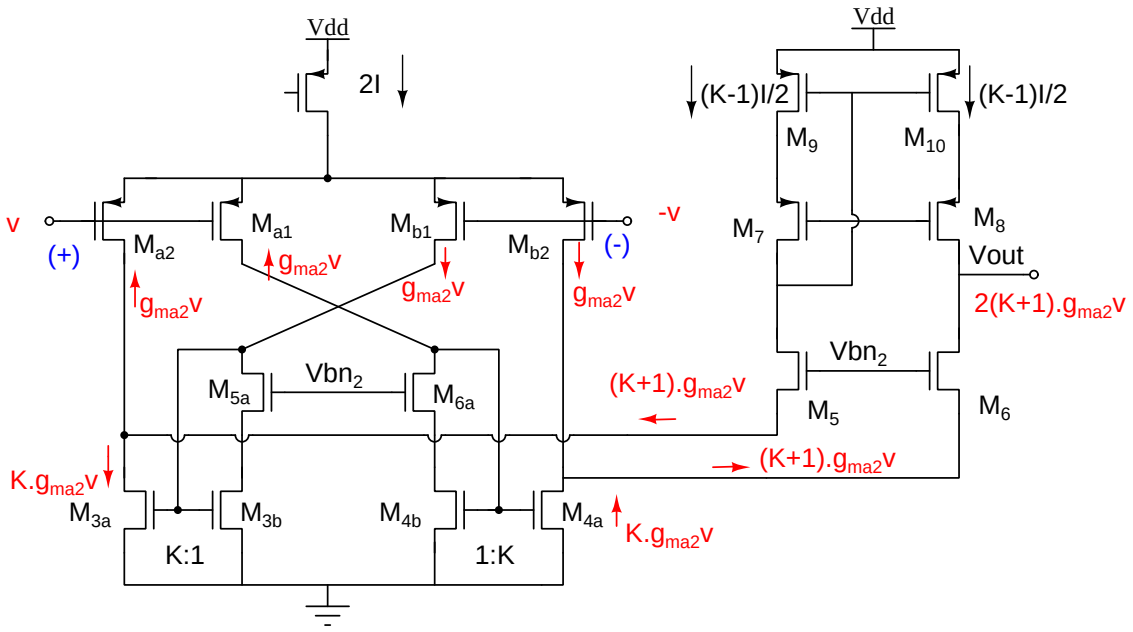

Figure 3.3: Recycled Folded Cascode Structure with PMOS Input pair for driving distributed loads

As discussed in above sections, one such requirement of an LDO is to ensure it should be able to drive distributed loads across the chip. In order to reduce the power consumption at the full-chip level, one would ensure that a single error amplifier should be able to drive N stages of the FVF Driver. This causes a burden on the error amplifier as its output capacitance has increased, thus hampering the Op-amp characteristics. This reduces the op-amps driving capability as C_L is increased. Thereby, the Slew Rate (S.R) has been reduced. One crude way method to tackle this issue is by increasing the OTA Bias current such that I/C_L ratio remains as original. This increases the overall system's power consumption and is not the optimum solution.

We used a Recycled Folded Cascode structure [35] instead of a conventional folded cascode structure to tackle this issue. Fig. 3.3 shows the structure for Recycled Folded Cascode. The PMOS input pair mosfets are broken such that widths of mosfet M_{a1} and mosfet M_{a2} is equal to width of mosfet M_1 in conventional structure. The same way mosfets M_2 of conventional structure is broken in two mosfets namely M_{b1} and M_{b2}. As a result, all these 4 Mosfets carry a current of $I/4$.

Now, in order to increase the small signal current going to the output, the connections are flipped from mosfet M_{a1} and M_{a2} such that small signal current gets added in phase. In order

to analyze the recycled folded cascode structure small signal analysis is performed as shown in Fig. 3.3 with red colors. Clearly, the short circuit current that goes to the output is :

$$I_{short-circuit} = 2(K+1)g_{m2a} \tag{3.7}$$

Since g_{m2a} has an effective g_m of half of what an input pair sees of an conventional folded cascode structure. Therefore this results in an effective transconductance of RFC higher than than that of folded cascode. The expression for both of these schemes is shown below:

$$g_{m,RFC} = (K+1)g_{m,FC} \tag{3.8}$$

$g_{m,RFC}$ denotes the effective transconductance of recycled folded cascode structure and $g_{m,FC}$ denotes the effective transcoductance of an conventional folded cascode structure. Apart from this the multiplication factor $K = 3$. The value 3 is chosen such that the current consumption remains same in Folded Cascode and Recycled Folded Cascode. Therefore, the Bandwidth of the system as Bandwidth is proportional to G_m/C. For K=3, the current in transistor M_{5a} and M_{6a} is half that of as compared to transistor M_5, M_6 respectively. The current density should be maintained properly. This ensures efficient current mirroring. Apart from the increase in $G_{m,RFC}$, the Output impedance R_{out} is also increased. To understand this intuitively, since the current is reduced in the mosfets M_{b2} and M_{a2}. Since $r_0 = \frac{1}{\lambda I_q}$ therefore, r_0 is increased in RFC as compared to FC. As a result of which the structure Recycled Folded Cascode offers a much higher Gain as compared to Folded Cascode.

The analysis above is for the small signal picture. In order to find the large signal behaviour we will apply a large signal at the positive terminal of the RFC [36]. As a result the mosfets $M_{a1}, M_{a2}, M_{4b}, M_{4a}$ are all off. This results in Mosfet M_{b2} to go in triode region as drain potential of M_{b2} was increasing. Therefore,all the bias current I flows from M_{b1} and eventually gets mirrored with a multiplication factor of K and reaches the output. As a result the Slew Rate of RFC structure is given by

$$SR_{RFC} = \frac{2KI}{C} \tag{3.9}$$

whereas the Slew Rate of FC structure is given by

$$SR_{FC} = \frac{2I}{C} \tag{3.10}$$

Fig. 3.4 shows a comparison of step response between the two structures simulated in TSMC 180 nm. Both the structures work for an input voltage of 0.9V and consume a bias current of 2 μA. The step applied is a rail-to-rail with a rise time of 1ns. Clearly, RFC offers a much-improved slew response without increasing the bias current in the Error amplifier. As a result, the choice for EA would be RFC configuration for driving distributed load, i.e., one error-amplifier driving multiple FVF drivers. Now, we will look to solve the second problem by providing programmable options to change the output voltage.

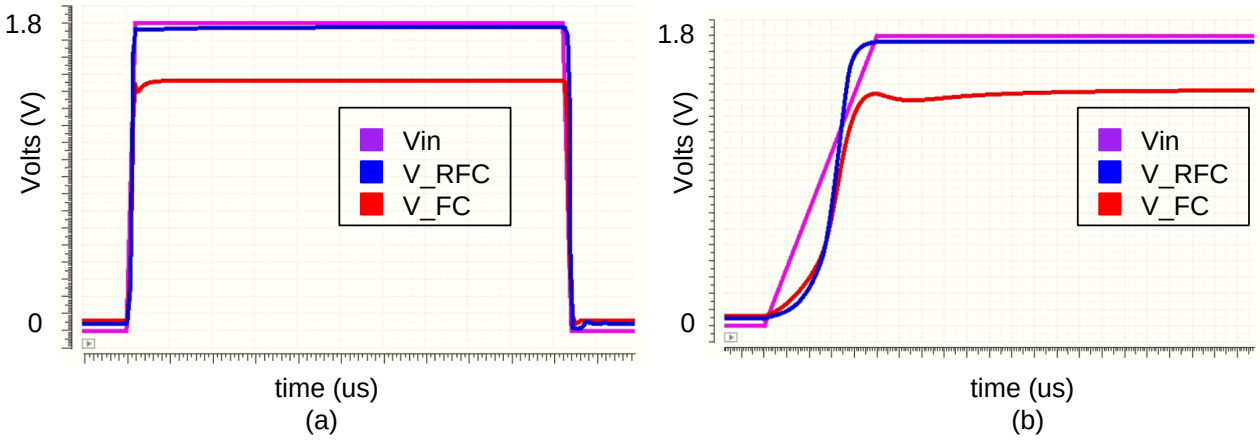

Figure 3.4: (a) Step Response of Folded Cascode with Recycled Folded cascode with a rise time o 1 ns. (b) Zoomed in version at the edge to show the difference in both the curves.

3.3.2 Method 1: Adding Programmable Option before V_{SG} Cancellation

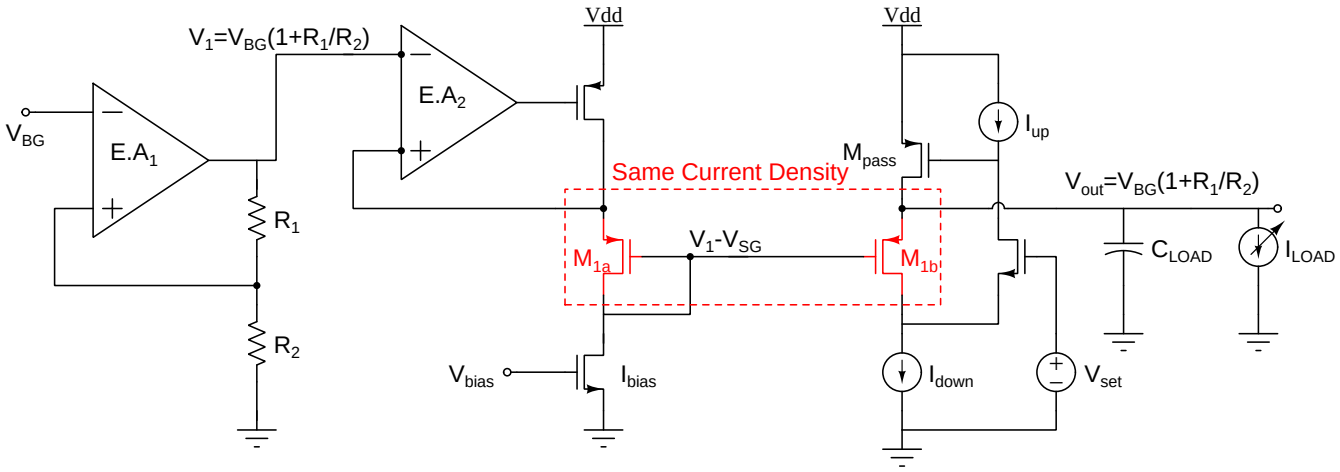

Figure 3.5: Adding Programmable Option before V_{SG} cancellation

In the first method, a programmable option is introduced before V_{SG} cancellation, as depicted in Fig. 3.5. The first error amplifier provides a programmable output given by:

$$V_1 = V_{BG}(1 + \frac{R_1}{R_2}) \tag{3.11}$$

This output is then fed into the original circuit shown in Fig. 3.2. The first amplifier is a PMOS input pair based device, given the low input voltage close to 0.9 Volts. The second amplifier is an NMOS input pair based device, as the voltage is scaled by the gain factor $(1 + R_1/R_2)$.

Clearly, the circuit shown in Fig. 3.5 gives an programmable output voltage V_{out} which is expressed below.

$$V_{out} = V_{BG}(1 + \frac{R_1}{R_2}) \tag{3.12}$$

This programmable option offers the flexibility to adjust the output voltage back to its desired value, considering aging and PVT variations. However, this scheme, while theoretically effective, suffers from design complexity. The second error amplifier EA_2 needs to operate until the rail-to-rail supply[37], complicating the design. To address this, an alternative scheme is explored in the next subsection.

3.3.3 Method 2 :Adding Programmable option after V_{SG} Cancellation

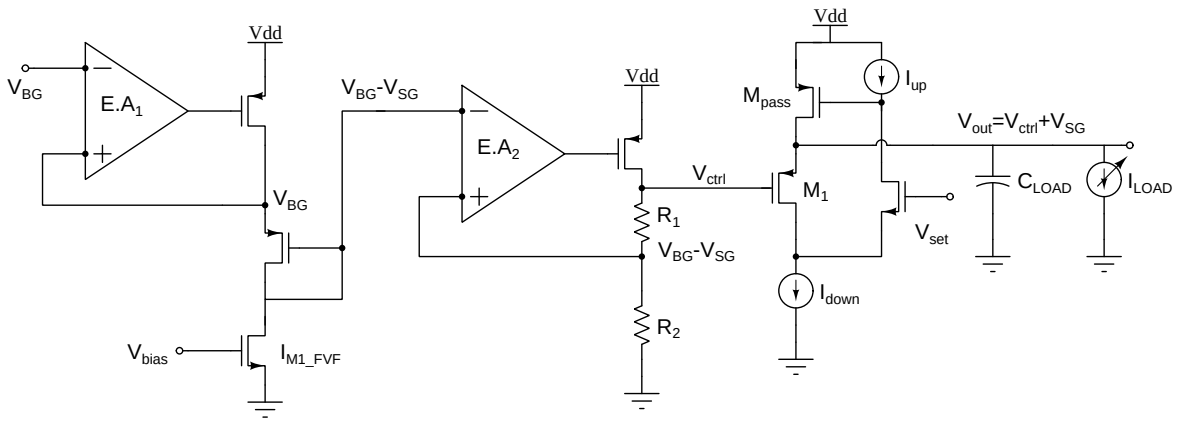

Figure 3.6: Adding Programmable Option after V_{SG} cancellation

As discussed earlier, to avoid the complexity introduced by adding a programmable option before V_{SG} cancellation, an alternative scheme is presented in Fig. 3.6. In this arrangement, the programmable option is applied after V_{SG} cancellation. The first amplifier is a PMOS input pair Operational Transconductance Amplifier (OTA), generating an output voltage $V_{BG} - V_{SG}$. This output is then fed to a programmable output stage. Given the low input, the second OTA is also a PMOS input-based OTA, providing a gain of $(1 + \frac{R_1}{R_2})$that can be adjusted to achieve the desired output voltage level.

However, this approach has a drawback: effective V_{SG} cancellation is not achieved. The output voltage in this scheme is expressed as:

$$V_{out} = (V_{BG} - V_{SG})(1 + \frac{R_1}{R_2}) - V_{SG} \tag{3.13}$$

Clearly, in Eq. the V_{SG} cancellation is not done effectively and a factor of process and temperature dependent V_{SG} would come at the output. This clearly makes the response much

poorer than previous method. In this equation, V_{SG} cancellation is not effectively executed, and a factor of the process and temperature-dependent V_{SG} contributes to the output. This compromises the response compared to the previous method.

In the subsequent subsection, a new scheme will be introduced to address this issue, aiming for effective V_{SG} cancellation without imposing additional complexity on the design of any of the error amplifiers.

3.4 An Programmable and Efficient Vth cancellation based LDO with added Trim Bits

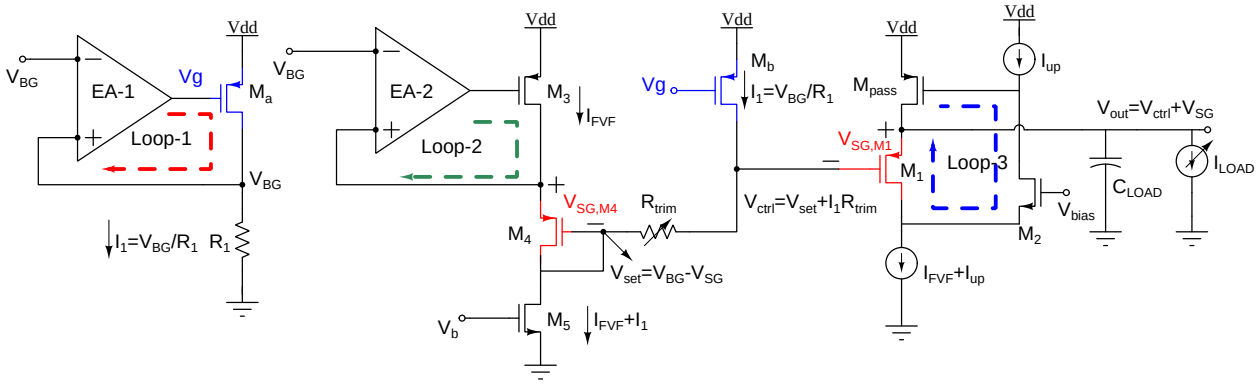

Figure 3.7: First-cut FVF Based LDO with effective V_{th} cancellation scheme

The circuit shown in Fig. 3.7 introduces an efficient method to generate a programmable and clean V_{SG} cancellation-based LDO regulator. The first operational amplifier is used to generate a constant current equal to I_1 :

$$I_1 = \frac{V_{BG}}{R_1} \tag{3.14}$$

The second operational amplifier generates a voltage $V_{BG} - V_{SG}$. Instead of using amplification, the term $I_1 * R_{trim}$ s added to provide programmable output. The output voltage is expressed as:

$$V_{out} = V_{BG} + I_1 * R_{trim} \tag{3.15}$$

This can be further written as :

$$V_{out} = V_{BG} + V_{BG}\frac{R_{trim}}{R_1} \tag{3.16}$$

Importantly, the output voltage is not a function of Process, Voltage, and Temperature (PVT). Even though resistance values change across PVT, their ratio remains constant.

However, this scheme comes with the drawback of increased power consumption due to the need for an additional operational transconductance amplifier (OTA). Additionally, two extra branches, each consuming I_1 amount of current, are added.

Beyond the extra power consumption, the system is a single-loop system. In Fig. 3.7, there are three different loops working individually. If any change in V_{out} occurs, only Loop 3 would react to correct this action.

To overcome these limitations, the next step involves extending this structure to a dual-loop system, where two different loops work together to enhance the system response speed. The next chapter will delve into this topic along with a design methodology to make the entire system more efficient.

Chapter 4

Efficient Programmable LDO with Dual-Loop Structure with improved transient response

In the preceding chapters, we delved into the challenges faced by Low Dropout Regulators (LDOs) in handling extensive distributed loads and examined the essential criteria for an ideal LDO. A concise summary is provided below.

Typically, an SoC seeks multiple LDOs to provide regulated supply to its different peripherals distributed across the chip. The primary requirement of such an LDO is to mimic the behaviour of an ideal voltage source ($R_{out} \approx 0$) and provide ripple-free output. Conventional LDOs were designed by placing large off-chip capacitors (C_{ext}) at the output node, which ensured stability as well as provided excess charge during load current switching [38]. However, these kind of designs suffer from two limitations. (1) It is not possible to achieve monolithic integration. (2) As the dominant pole is set by the output node pole, any increase in C_{ext} would affect the performance metrics of LDO like unity-gain bandwidth (UGB), settling time (t_s) etc. These challenges at hand has led to an increased recognition of output capacitor-less (OCL) based LDOs as a viable solution for resolving these issues.

Two of such variants of OCL-LDO are PMOS and NMOS-based pass transistor respectively. However, both of these designs have their own limitations. For instance, the output resistance offered by PMOS-based driver is large, which is not desired ($R_{out} \approx r_{ds}$). Although the output impedance offered by the NMOS-based driver is small ($R_{out} \approx \frac{1}{g_m}$), they require much higher gate voltages to turn on the NMOS pass transistor. Thus requiring an additional charge pump [24]. It eventually increases the noise due to continuous switching of capacitors and increases the area requirements[26]. Apart from this, each structure requires an additional transient detection block that adaptively changes the bias current to reduce the overshoot/undershoot during load switching. Moreover, multiple copies of such LDOs are needed to drive distributed loads, which can significantly increase both power consumption and area requirements.

To tackle these challenges, a digitally programmable multi-loop-based LDO using distributed Flipped Voltage Follower (FVF) is presented. It (i) offers very low R_{out}, (ii) does not require

any additional blocks such as a charge pump (iii) adds scalability features to drive distributed loads without increasing the power budget, and (iv) ensures inherent stability of the system.

4.1 Proposed LDO structure for driving large capacitive load

An FVF structure as we have already discussed, offers a much smaller output impedance compared to its C.D. counterpart. This reduction in the output resistance implies one can drive a much larger capacitance (C_{load}) at the output and still ensure the system's stability. Thus, the structure can be used as a substitute for NMOS driver. In addition to extremely low R_{out}, it doesn't require any additional charge pump as the input V_{ref} goes to PMOS transistor.

Fig. 4.1 shows the structure for the proposed LDO to provide ripple-free supply and is suitable for high-frequency applications. However, the structure consists of two loops as shown in Fig. 4.1. Loop-1 is the fast loop due to the inherently low output impedance of the FVF structure. Whereas the outer loop (Loop 2) is the slow loop which is used to provide DC accuracy by connecting the feedback to V_{BG} by using the virtual short property of op-amp. The resistor ladder consisting of R_1 and R_2 provides programmable output and is represented as

$$V_{out} = V_{BG}(1 + \frac{R_1}{R_2}) \tag{4.1}$$

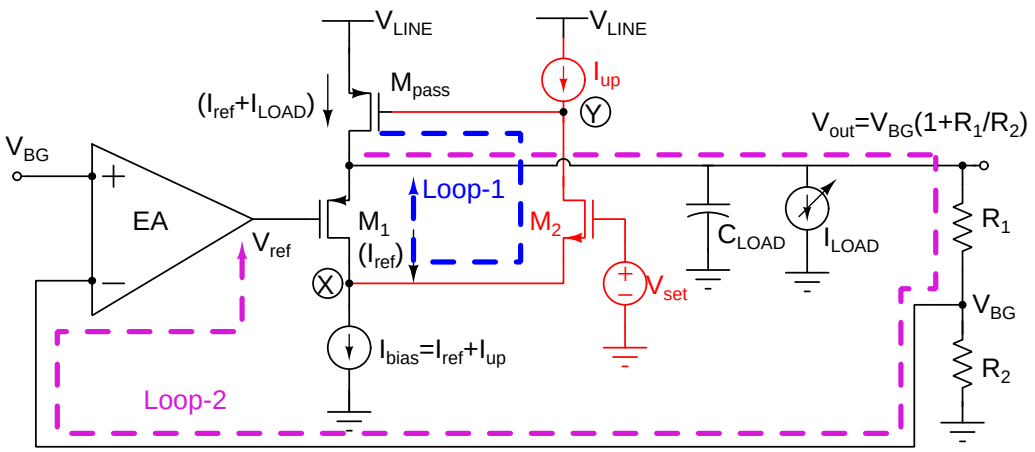

Figure 4.1: Interacting multi-loop based LDO with EA implemented using Recycled Folded Cascode (RFC)[35] with K=3 (Miller compensation not shown for better visibility)

Since the system shown in Fig. 4.1 now consists of two interacting loops as a result extra care needs to be taken to ensure stability of the whole system. As a general rule for thumb, whenever designing an interacting a multi loop system the fast loop is designed to be much higher bandwidth than the slow loop bandwidth. It is typically done to ensure that that the

phase lag due to fast loop can be neglected while calculation the phase delay of the slow loop. Therefore, effectively making the system in a way non interacting. Now in order to ensure the same pole zero analysis of both the loops are discussed in subsequent section such that the system remains stable.

4.1.1 Pole-Zero Analysis of Multi-Loop based LDO

The section presents the pole zero analysis of each loop independently. Although as mentioned above even though the loops are interacting, we can make them kind of non interacting. It can be achieved by ensuring that the fast loop bandwidth is much higher than the slow loop bandwidth.

4.1.1.1 Fast Loop Analysis

The analysis of the FVF Loop is presented first as this sets an upper bound on the bandwidth of slow loop. To perform the analysis of the FVF loop a dc voltage source V_{ref} is applied and the corresponding pole-zeros are observed by breaking the FVF loop. The open loop gain for the fast loop is expressed below

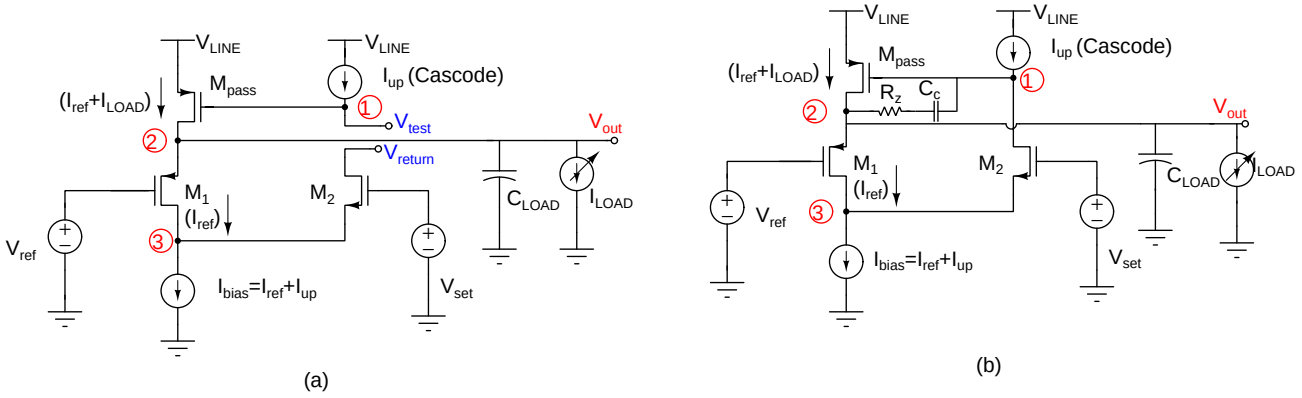

Figure 4.2: Pole Zero Analysis of the Fast Loop by doing the (a) Loop Test Analysis (b) Fast Loop Compensation by using Miller Compensation

$$A_{OL,FL} \approx -[\frac{g_{m,pass}}{g_{m_1}}].[g_{m_1}(r_{o_2}||r_{o,I_{bias}})].g_{m_2}(r_{o,I_{up}}||g_{m_2}r_{o,2}r_{o,I_{bias}}) \tag{4.2}$$

To maximize the $A_{OL,fast-loop}$ $r_{o,up}$ should be designed using cascode structure where $r_{o,bias}$ should be designed using simple current mirror. Since in the above Eq. 4.2 the only dynamic term is $r_{o,pass}$ rest all the terms are fixed. As a result at maximum loads $r_{o,pass}$ becomes very

small as a result the $A_{OL,fast-loop}$ reduces. This can be understood from basic Equation shon below.

$$r_{o,pass} = \frac{1}{\lambda I_{LOAD}} \tag{4.3}$$

The dominant pole is at node Y and its location is given by

$$\omega_{p,1} = \frac{1}{[r_{o,up}||g_{m,2}r_{o,2}r_{o,down}]C_Y} \tag{4.4}$$

The second pole is at the output node and is expressed as:

$$\omega_{p,2} = \frac{1}{[\frac{1}{g_{m,1}}||r_{o,pass}]C_{out}} \tag{4.5}$$

Node X also appears in the signal path which also contributes a pole whose location is given by:

$$\omega_{p,3} \approx \frac{1}{[\frac{1}{g_{m,1}}||\frac{1}{g_{m,2}}||r_{o,down}]C_x} \tag{4.6}$$

As C_x is many order of magnitudes smaller than C_{out}, therefore $\omega_{p,3}$ lies far away from $\omega_{p,2}$. A right half plane zero also appears because of the parallel path coming because of $C_{gd,pass}$ whose location is given by:

$$\omega_{z,1} = \frac{g_{m,pass}}{C_{gd,pass}} \tag{4.7}$$

At Light Load $\omega_{p,1}$ and $\omega_{p,2}$ comes close to each other as at light load $r_{o,pass}$ increases. This effect is further enhanced as the Loop Gain is increased at light load as compared to heavy load. Therefore, a compensation technique is required to stabilize the system particularly at light load. So to stabilize the FVF loop, Miller compensation technique is used by placing a miller cap C_c and R_z as shown in Fig. 4.2(b)

4.1.1.2 Slow Loop Analysis

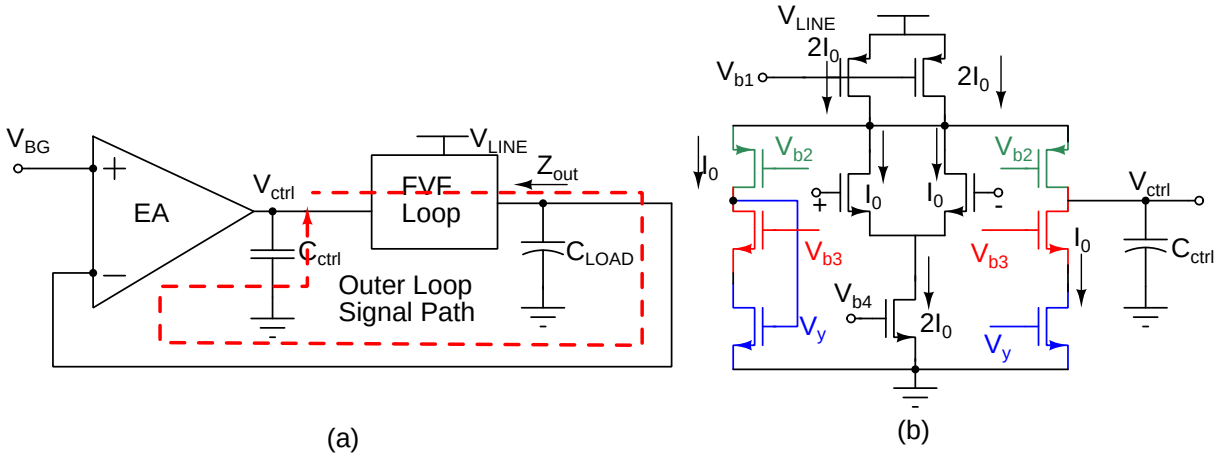

Figure 4.3: (a) Signal path of Outer Loop (b) Folded Cascode amplifier with NMOS input pair (biasing circuit excluded)

The Outer Loop (Loop-2) is the slow loop whose signal path is depicted as shown in Fig. 4.3. The V_{ctrl} node determines the dominant pole. As depicted in Fig. 4.3, the error amplifier shown here is a simple Folded Cascode structure biased in sub-threshold region. This ensures that the bandwidth of the system remains small and the amplifier doesn't burn too much power. An additional capacitor C_{ctrl} is also added at the V_{ctrl} node to ensure that the V_{ctrl} remains the dominant pole.
The second node in the signal path of the outer loop is the V_{out} node. However, when FVF loop is used as a driver as in our case then the V_{out} node consists of complex conjugate poles. This can be calculated by plotting the impedance of the FVF driver loop as shown in Eq. (4.8) [27].

$$Z_{out,FVF}(s) \cong \frac{(1+s(r_{o,1}\|r_{o,bias})(C_{gs,pass}+C_{gd,1}))}{g_{m,1}r_{o,1}g_{m,pass}\left(1+\left(\frac{C_{gs,pass}}{g_{m,pass}}+\frac{C_{Load}}{g_{m,1}g_{m,pass}(r_{o,1}\|r_{o,bias})}\right)s+\left(\frac{C_{gs,pass}C_{Load}}{g_{m,1}g_{m,pass}}\right)s^2\right)} \tag{4.8}$$

Eq. (4.8) results in a complex pole under the conditions when $g_{m,pass} >> g_{m,1}$ and $C_{Load} >> C_{gs,pass}$. The location of the complex pole is given by:

$$\omega_{p_{1,2}} = \sqrt{\frac{g_{m,1}g_{m,pass}}{C_{Load}C_{gs,pass}}} \tag{4.9}$$

This peaking can cause a significant decrease in phase response and can push the system to become unstable. Hence, the FVF driver should be designed such that peaking occurs at a high frequency, and the magnitude of peaking should be limited [39].

4.1.1.3 Simulation Results of Multi-loop System

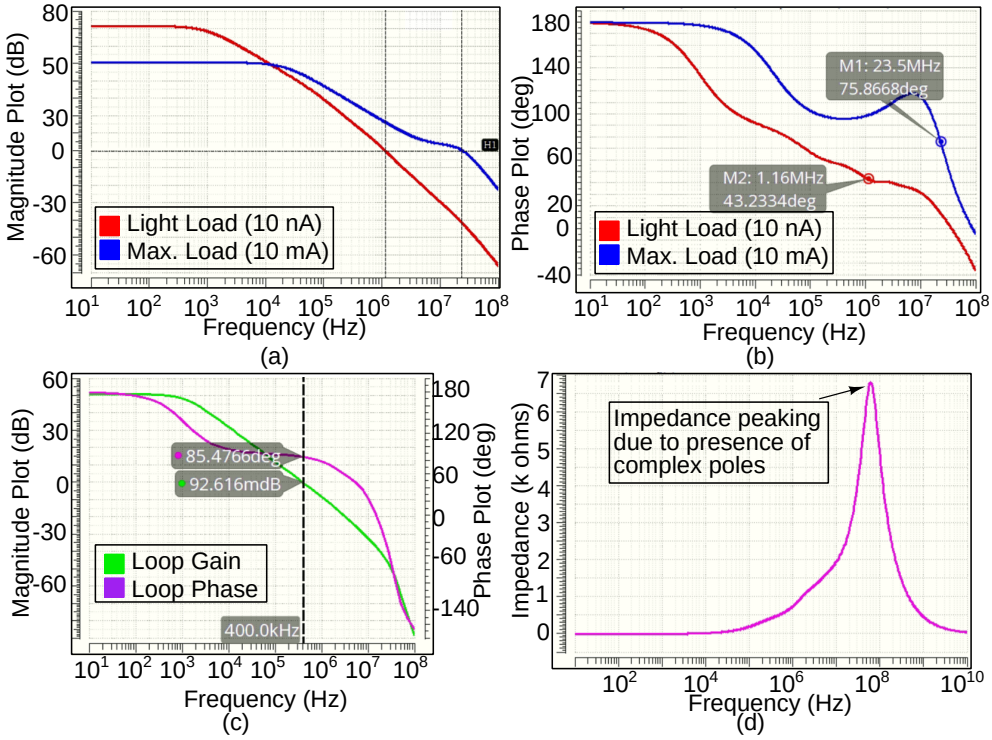

Figure 4.4: (a) Magnitude and (b) Phase plot for the FVF Loop at No Load (shown in red) and maximum load (shown in blue).(c) Magnitude and Phase plot for the slow loop(outer loop) (d) Impedance peaking in the FVF structure due to complex poles must be designed such that it occurs at a higher frequency than fast loop U.G.B at maximum load

Fig. 4.4(a) and (b) shows the magnitude and phase response of the Fast Loop for light and heavy load respectively. As discussed above, the low frequency d.c gain for light load is more than that of maximum load. The FVF loop is stable in both the conditions i.e. min and max loads. At maximum load the system is stable with a phase margin of 75°and with the unity gain bandwidth of 23.5 MHz. Similarly at light load condition the system is stable with a phase margin of 43 °and with the unity gain bandwidth of 1.16 MHz. Miller Capacitance C_c of 1 pF and R_z of 32 $K\Omega$ is used to ensure stability across all corners.

To ensure that this fast loop effectively becomes non interacting with the outer loop. The bandwidth of the of the outer loop should be less than the bandwidth of fast loop. So, the upper bound on the unity gain bandwidth of the outer loop should be less than 1.16 MHz. An extra cap C_{ctrl} of 1 pF is added at the V_{ctrl} node to make the dominant pole moves towards the origin thereby reducing the bandwidth of outer loop.

Fig 4.4(c) shows the magnitude and phase response of the outer loop. The outer loop is stable

with a phase margin of 83 °and with a unity gain bandwidth of 400 KHz which is less than 1.16 MHz. Fig. 4.4(d) shows the impedance peaking behavior of the FVF driver. Although the peaking occurs due to complex poles but it occurs at a very high frequency. By the time we see these peaking in the magnitude and phase plots our gain has already rolled off below 0 dB axis and hence the system remains inherently stable. Since the structure has two negative feedback loop to bring back the V_{out} to the desired voltage. This topology can be further extended to exploit parallelism by placing N parallel FVF drivers to a single V_{ctrl} generating block.

4.2 Power Grid Structure using Distributed FVF Driver

As discussed above, due to multiple loops, the structure can be extended to exploit parallelism by connecting N parallel drivers to a single V_{ctrl} generating block. This can also be understood intuitively as each FVF loop reacts abruptly due to any changes in V_{out} and tries to bring back V_{out} to its desired voltage. Therefore, replicas of only the FVF driver must be instantiated only where each FVF serves as a local loop to its driver. To further enhance the performance metric, a power grid structure is also proposed where each FVF output is connected to the power grid as shown in Fig. 4.5. The structure significantly improves the transient performance of the proposed LDO with the addition of any additional transient detection schemes. The next section discusses about the benefits of the proposed scheme.

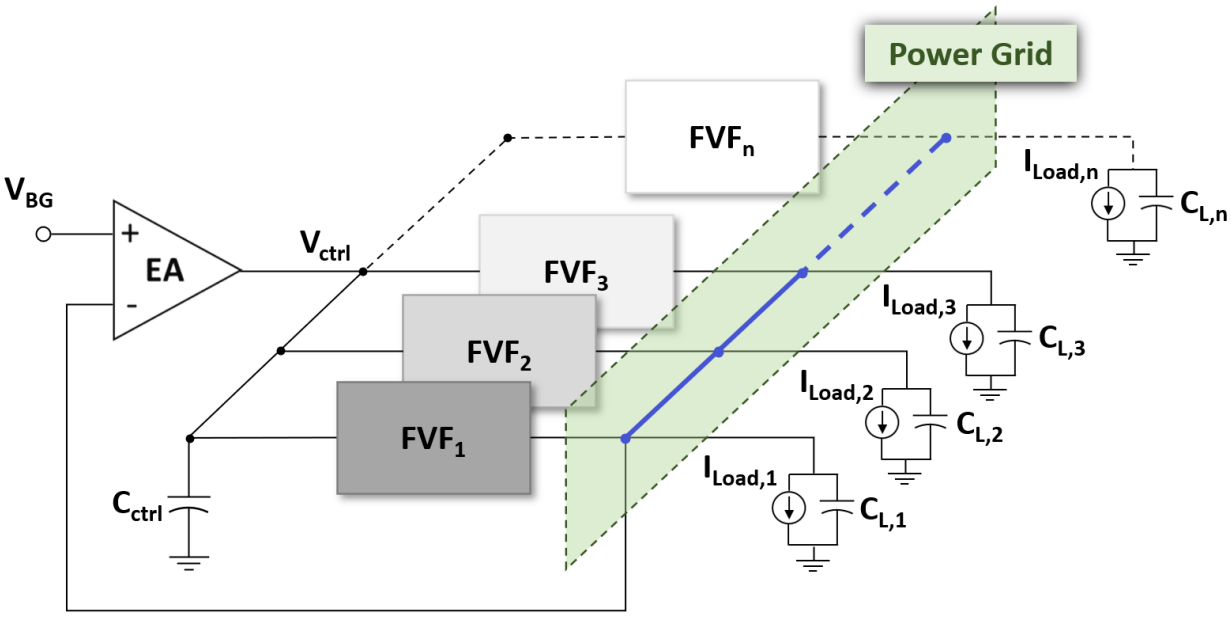

Figure 4.5: Block Diagram representing N distributed drivers connected a single power grid

4.3 Advantages of the Proposed Scheme

4.3.1 Reducing the Effective Resistance

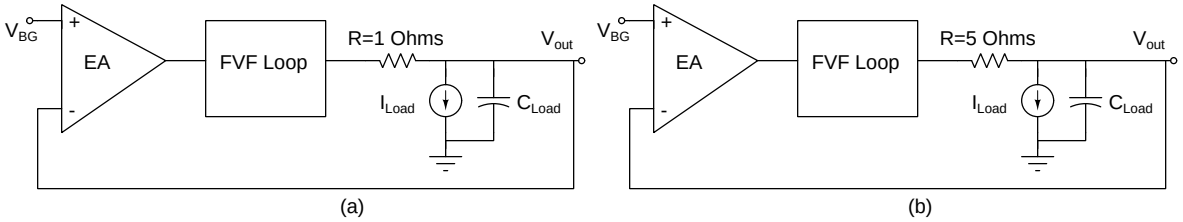

Figure 4.6: Significant IR drop when the load is placed at a faraway point due to significant routing resistance

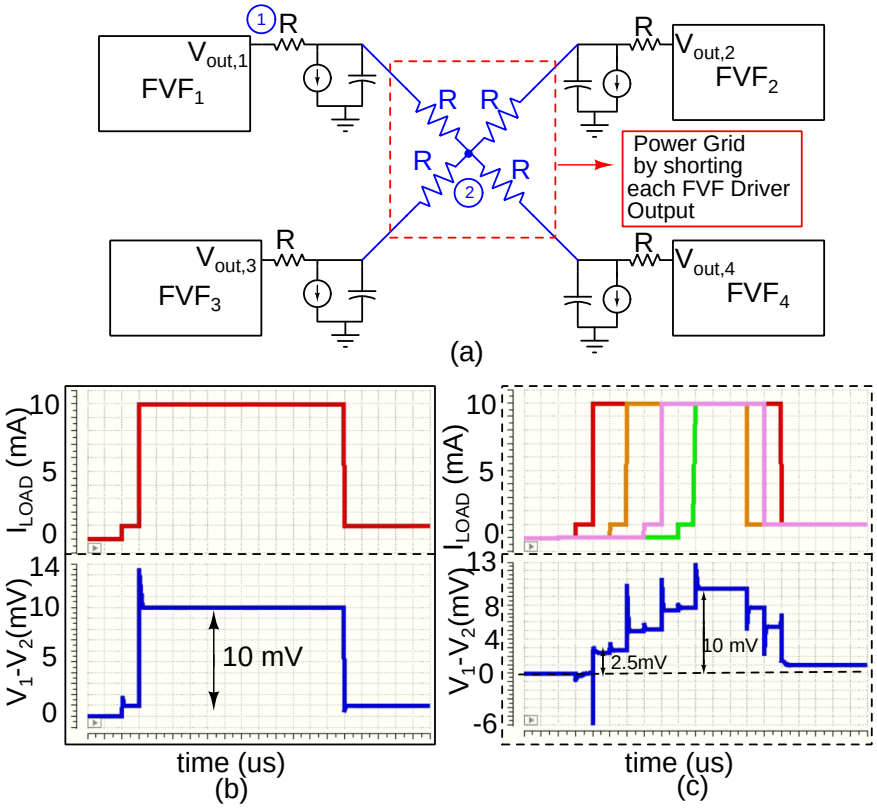

Figure 4.7: (a) Distributed FVF driver connected to a power grid to reduce the effective resistance resulting in reducing (b) At I_{LOAD} of 10 mA voltage difference between node 1 and node 2 is 10 mV for $R = 1\ \Omega$ whereas (c) The net resistance reduces to 0.25 Ω for distributed load and the corresponding voltage difference of 2.5 mV

The first major advantage of the proposed scheme is the reduction in effective resistance seen from the load. This can be intuitively understood from Fig. 4.6 (a) and (b). Fig. 4.6(a) shows the case when the load is placed close to the FVF driver thereby by modelling a resistance of 1 Ω. So for a maximum load of 10 mA one observe a drop of 10 mV on the routing resistance. The same effect is magnified in Fig. 4.6(b) by considering the case when the FVF driver and load are much widely separated by modeling a routing resistance of 5 Ω. For this case we would see a drop of 50 mV across the routing resistance. Therefore, reducing the routing resistance should be the way around to solve this issue. Since the resistance reduces in parallel combination therefore the proposed power grid structure reduces the effect of routing resistance. Fig. 4.7(a) shows how the routing resistance can be reduced by connecting parallel FVF drivers. To model the routing resistance, a 1Ω resistor is placed between node 1 and 2 as shown in Fig. 4.7(a). Fig. 4.7(b) shows the simulation results of standalone FVF with a routing resistance of 1Ω. As expected, a voltage drop of 10 mV is observed because of the routing resistance at 10 mA of load current. However, for the proposed structure shown in Fig. 4.7(c) with $N = 4$ drivers, we see a reduction in resistance from R to $\frac{R}{4}$. Therefore, the drop across the routing resistance reduces from 10 mV to 2.5 mV. This technique can be extended to N such drivers. Thereby reducing the effective resistance from R to $\frac{R}{N}$ and effectively reducing the IR drop.

4.3.2 Reducing the Undershoot/Overshoot Voltage

The proposed structure helps in reducing the undershoot/overshoot voltage for same step change in Load current without any additional transient detection circuits. Fig. 4.8(a) shows the transient response for the standalone FVF driver shown in Fig. 4.1. The corresponding results of undershoot/overshoot are tabulated in Table. 4.1. Fig. 4.8(b) shows the layout of the proposed scheme with $N = 4$ drivers. Fig. 4.8(c) and (d) shows the schematic results of the proposed LDO for different profiles of I_{LOAD}. The I_{LOAD} is varying in a staggered manner in Fig. 4.8(c) whereas I_{LOAD} is varying in a periodic manner in Fig. 4.8(d). The corresponding transient responses are captured in Table 4.2 and Table 4.3. Fig. 4.8(e) and Fig. 4.8(f) shows the post layout results for the proposed distributed driver for different profiles of I_{LOAD}. The results shows an improvement in transient response by reduction in overshoot/undershoot voltage by more than 40%.

Table 4.1: Transient Behaviour of Standalone FVF (Post Layout Results)

I_{LOAD} variation	Rise/Fall Time	Undershoot/Overshoot
10 nA $->$ 1mA	1 ns	200 mV
1 mA $->$ 10 mA	1 ns	430 mV
10 mA $->$ 1mA	1 ns	180 mV

Table 4.2: Transient Behaviour for Multi Driver FVF with I_{LOAD} variation in staggered response (Schematic Results)

I_{LOAD} variation	Rise/Fall Time	Undershoot/Overshoot
10 nA $->$ 1mA	1 ns	77 mV
1 mA $->$ 10 mA	1 ns	170 mV
10 mA $->$ 1mA	1 ns	100 mV

Table 4.3: Transient Behaviour for Proposed LDO with load currents switching at different intervals (Schematic Results)

I_{LOAD} variation	Rise/Fall Time	Undershoot/Overshoot
10 nA $->$ 1mA	1 ns	80 mV
1 mA $->$ 10 mA	1 ns	170 mV
10 mA $->$ 1mA	1 ns	100 mV

Table 4.4: Transient Behaviour for Multi Driver FVF with I_{LOAD} variation in staggered response (Post Layout Results)

I_{LOAD} variation	Rise/Fall Time	Undershoot/Overshoot
10 nA $->$ 1mA	1 ns	90 mV
1 mA $->$ 10 mA	1 ns	200 mV
10 mA $->$ 1mA	1 ns	110 mV

Table 4.5: Transient Behaviour for Proposed LDO with load currents switching at different intervals (Post Layout Results)

I_{LOAD} variation	Rise/Fall Time	Undershoot/Overshoot
10 nA $->$ 1mA	1 ns	90 mV
1 mA $->$ 10 mA	1 ns	200 mV
10 mA $->$ 1mA	1 ns	170 mV

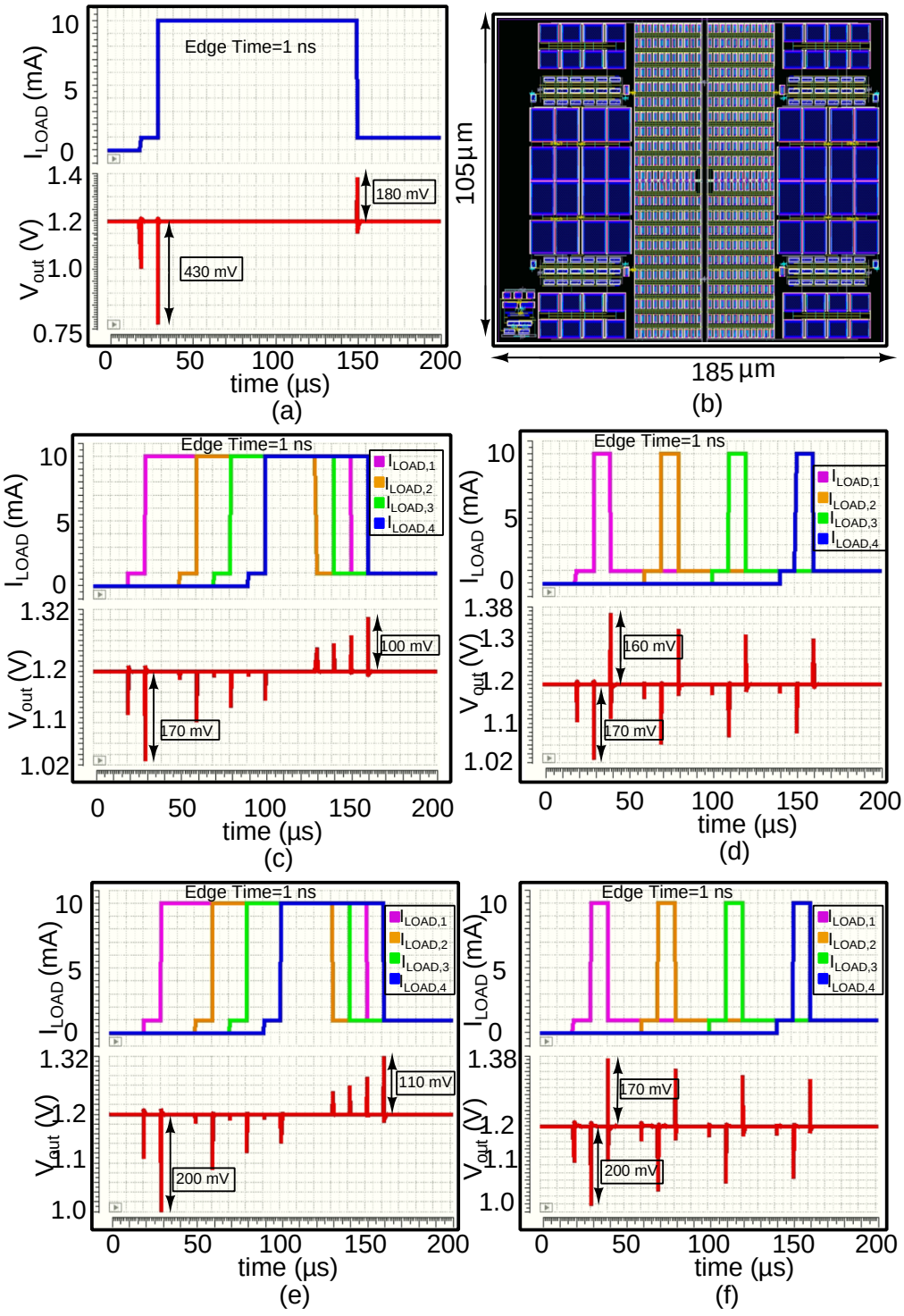

Figure 4.8: (a) Transient response for the standalone FVF structure shown in Fig. 4.1. (b) Layout of the proposed scheme with 4 FVF drivers. Post layout results for the proposed LDO with I_{LOAD} varying in a (c) staggered fashion and (d) periodically varying for the Circuit shown in Fig. 4.5.

4.3.3 Higher Noise Immunity

Apart from the advantages mentioned above, the scheme also provides much better noise immunity. Fig. 4.8 (c) and Fig. 4.8 (d) shows that the overshoot and undershoot keep reducing as N increases. It is evident as the consecutive value of droop/overshoot voltage keeps reducing every time one more load is turned on. It indicates that the noise on one of the drivers is distributed across N drivers. As a result, we see this reduction in consecutive undershoot/overshoot. Thus, the proposed structures employing N distributed drivers ensure much better power integrity than the conventional structures. The next subsection examines how the choice for N is made.

4.3.4 Factors determining the Choice of N

Till now, we have been using N arbitrarily in our discussion. However, the power budget helps determine the choice for N by ensuring that the system remains stable. For a fixed total current I_0 the current through each FVF cell is $\frac{I_0}{N}$. Therefore as N keeps increasing, the current through each FVF driver starts reducing, which effectively reduces the U.G.B of the structure. The more concerning thing is that at low currents, the poles start coming close to each other, resulting in instability of FVF driver cell. This helps in deciding the value for N.

Table 4.6: Performance Comparison with Recent works

Parameter	[38]	[24]	[40]	[41]	[42]	This Work
Technology (nm)	90	65	65	65	65	180
Vin/Vout	0.75/0.5	2.4-2.6/1	1.2/1	1.2/1	1.2/1	1.4/1.2
Load Cap (pF)	7	39	50	100	-	150
ΔV_{out} (mV)	114	195	200	250	143	200
I_Q (A)	8	195	13.2	28/3	58.2	15*4
ΔI_L (mA)	100	30	50	9	60	9
Edge Time (ns)	100	0.2	100	100	1	1
FoM (mV)	4.5	1.265	26.4	41.66	0.693	6.67

$$FoM = K\frac{\Delta V_{out} I_Q}{\Delta I_L} \text{ [38]}$$

Chapter 5

Conclusions

5.1 Research Contributions

In conclusion, this thesis has undertaken a comprehensive exploration into the challenges posed by the burgeoning growth of 3D NAND Flash Arrays. The industry's demand for increased memory storage in the face of this technological surge presented critical hurdles, notably in the realm of load capacitance within conventional structures.

The initial chapters of this work meticulously dissected the limitations of existing designs, laying the groundwork for a transformative solution. Our investigation revealed that conventional structures faced significant hurdles, especially when subjected to elevated load capacitance inherent in the evolving landscape of 3D NAND Flash Arrays.

Building on this understanding, the thesis articulated the ideal requirements for a Low-Dropout Regulator (LDO) and detailed the meticulous efforts undertaken to achieve these specifications. The introduction of a novel Flipped Voltage Follower (FVF) driver-based LDO marked a paradigm shift in the pursuit of effective power delivery systems.

The journey traversed various modifications to existing circuits, each carefully examined for its merits and drawbacks. A dual-loop architecture, leveraging FVF as a driver stage, stood out as a pivotal advancement, showcasing its efficacy in mitigating the impact of heightened load capacitance.

To ensure the stability of the proposed multi-loop system across varying Process, Voltage, and Temperature (PVT) conditions, a novel methodology was introduced. This methodology serves as a testament to the dedication to creating a design that is not only effective but also reliable in real-world operating conditions.

The pinnacle of our innovation lies in the presentation of a groundbreaking approach to drive large distributed loads — a multi-loop FVF driver topology. By extending this topology to incorporate N distributed FVF drivers connected to a common power grid structure, our method presents significant advantages over traditional LDO designs. Simulation results unequivocally

demonstrate a substantial reduction in overshoot/undershoot, surpassing standalone structures without the need for additional reduction schemes.

In essence, this thesis not only identifies and addresses the challenges associated with 3D NAND Flash Arrays but also propels the field forward by offering a practical and innovative solution. The culmination of this research signifies a noteworthy contribution to the domain of LDO design, promising enhanced stability, efficiency, and performance in the dynamic landscape of advanced semiconductor technologies.

As we navigate the evolving landscape of data storage technologies, the findings presented in this thesis pave the way for a new era of power delivery systems, poised to meet the escalating demands of the AI-driven data centers of tomorrow.

Related Publications

Relevant Publications

1. Ashish Papreja, Rakesh KK, Aravind Polkampally and Syed Azeemuddin, "A High-Performance Digitally Programmable FVF-Based LDO for efficient power management in driving distributed loads using a shared Power Grid" 2023 66th IEEE International Midwest Symposium on Circuits and Systems, Arizona, USA

Other Publications

1. Ashish Papreja, Sresthavadhani Mantha and A. Srivastava, "Design Methodology of Low Phase Noise mmWave Oscillator with Partial Cancellation of Static Capacitance of High-Q On-chip MEMS Resonator" 2022 35th International Conference on VLSI Design and 2022 21st International Conference on Embedded Systems (VLSID), India, 2022

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