Ultra-Low Power Analog Circuit Design for Resistance-to-Digital Converter and Voltage/Current References: Achieving High Precision and Energy Efficiency

Thesis submitted in partial fulfillment
of the requirements for the degree of

*Master of Science in **Electronics and Communication Engineering** by Research*

by

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CERTIFICATE

It is certified that the work contained in this thesis, titled ***" Ultra-Low Power Analog Circuit Design for Resistance-to-Digital Converter and Voltage/Current References: Achieving High Precision and Energy Efficiency"*** by Arnab Dey, has been carried out under my supervision and is not submitted elsewhere for a degree.

Date

Advisor: Dr. Zia Abbas

To My beloved Father and Mother

Acknowledgments

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My initial interest in Analog Circuit design was largely developed due to online resources available like Nptel lectures, which are highly intuitive and easily comprehensible. The available resources encompass lectures delivered by prominent individuals in the field, including Dr. Shanthi Pavan from IIT-Madras, Dr. Nagendra Krishnapura from IIT-Madras, Dr. Behzad Razavi from the University of California, Los Angeles, Dr. Ali Hajimiri from CalTech, Prof. K Radhakrishna Rao from IIT-Madras, Dr. Qadeer Ahmad Khan from IIT-Madras, and Dr. Saurabh Saxena from IIT-Madras. I would like to express my immense gratitude to Dr. Inhee Lee from the University of Pittsburgh for providing constant guidance and support throughout my first project which enabled me to learn and dive deep into the depth of Analog Circuits. Dr. Lee inspired me through his diverse knowledge and passion for research. I thank Texas Instruments for giving me the opportunity to get a hands-on experience on real fabrication issues and I got to know all the steps of Analog Circuit Design from defining the problem to implementation, design verification, fabrication, and testing.

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Abstract

In the dynamic landscape of the semiconductor field, the application and significance of ultra-low power circuits have become paramount, particularly in the domains of the Internet of Things (IoT) and biomedical applications. The relentless pursuit of higher speeds in traditional semiconductor designs is giving way to a new paradigm where energy efficiency takes precedence. In IoT applications, where devices are often constrained by the absence of continuous power sources, ultra-low power circuits enable prolonged operation through energy harvesting or miniaturized batteries. This not only extends the device lifespan but also aligns with the energy-conscious demands of IoT ecosystems. In the realm of biomedical applications, the importance of ultra-low power circuits is underscored by the need for minimally invasive, long-term implantable devices. These circuits facilitate precise sensing, control, and communication within the human body, ensuring both longevity and safety. As the semiconductor industry navigates this transformative shift, the development and integration of ultra-low power circuits emerge as a crucial frontier, shaping the future of semiconductor technology with profound implications for IoT and biomedical advancements.

In ultra-low power IoT applications, as well as biomedical implants, need low power consumption, low supply voltage, and high accuracy. Keeping all these constraints in mind, we worked on designing an ultra-low power Resistance-to-Digital Converter (RDC) with improved Figure-of-Merit (FoM) and low-temperature sensitivity for miniature low-powered sensing system. The proposed RDC system consumes only 162nW, with FoM as low as 0.845pJ/conversion cycle. The RDC can measure wide range of resistances measuring from 50kΩ to 1MΩ. Due to this, the RDC can be configured to use as different sensors like pressure sensors, temperature sensors, touch sensors, etc.

For almost all IoT and biomedical systems, biasing circuits are essential, as these are in general always-on circuits. It makes sense to design voltage and current references in the ultra-low power domain. Consequently, we focused on designing a 2.3nW, sub-Bandgap voltage reference. It generates a reference voltage of 336mV without incorporating any resistors and operates for a high-temperature range of -40°C to 150°C and a supply range of 0.7V-4V. In the above temperature and supply ranges, the proposed circuit's power consumption stays fairly linear, eliminating the exponential power consumption issue at such high temperatures. Designed in 65nm CMOS process, it achieves an impressive line sensitivity of 0.0066%/V for a supply range of 0.7V to 4V and a PSRR of 89dB at DC and 1V supply. As we all know, the voltage reference always preferred to be process independent, and the proposed circuit shows a $\pm 3\sigma$-inaccuracy of 4.295% without additional trimming circuits. It used gate-leakage-based

resistance to save significant silicon area of high-value resistance. However, we need to design voltage and current references separately, and low-level current references require high-value resistances, and other CMOS current references suffer from high process variation.

Consequently, we focused on designing ultra-low power trim free voltage/current reference without using resistance and amplifiers. The whole system works for as low as 37nW. The proposed voltage/current reference outputs a voltage and current of 820mV and 3.23nA, respectively. Without trimming, the process variation of the proposed voltage/current reference is $1.34\%(\sigma/\mu)$ / $1.75\%(\sigma/\mu)$. Designed in 90nm CMOS process, it achieved proper trim-free, low-power operation without using resistors, Which reduces area significantly. These attributes make it a desirable choice for various ultra-low power wearables and IoT applications.

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Chapter 1

Introduction

Over the course of the last seven decades, we have witnessed a remarkable evolution in computing systems, a journey from individuals interacting with computers to the seamless integration of computers into our daily lives. In the early days of the internet, the collection of vast amounts of data relied heavily on human efforts, prompting the need for a new era in computing where systems could autonomously interact with their surroundings. This new era came to be known as the Internet of Things (IoT).

The IoT empowers us to connect everyday objects to networks, unlocking new and previously unattainable services and opportunities. As virtually anything can now be connected to the internet, the IoT is poised to emerge as the largest electronics market in the world. The accompanying figure provides clear evidence of a continuous upward trend in global active IoT connections over the years, with forecasts indicating further growth.

The applications of IoT, including those in the fields of biomedicine, wearables, surveillance, and environmental monitoring, require systems that can operate on energy derived from miniature batteries or energy harvesters, ensuring self-sustainability. Circuits powered by energy harvesters must be capable of functioning at lower supply voltages and lower power consumption. Conversely, circuits relying on miniaturized batteries need to be optimized for low power consumption across a wide range of supply voltages. Researchers worldwide have been challenged to adapt various IoT subsystems, including sensing networks, biasing networks, and radio frequency transmission circuitry, to meet these novel constraints. This manuscript introduces a range of circuit-level techniques and system-level optimizations to address the diverse needs of emerging applications in the IoT design space.

1.1 Motivation of Low Power Analog Design for IoT and Biomedical Applications

The quest for Low Power Analog Circuit Design holds a pivotal role in the ever-evolving landscape of technology, with particular significance in two cutting-edge domains: the Internet of Things (IoT) and Biomedical Applications. This thesis embarks on a journey to explore the profound implications

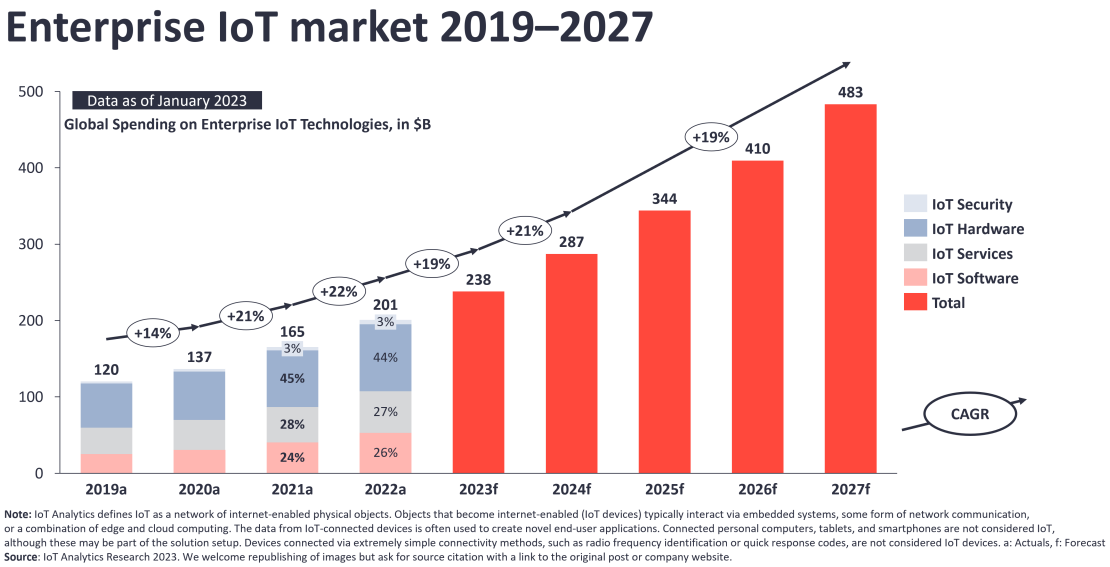

Figure 1.1: Global spending on Enterprise IoT Technologies [1]

and motivations behind this endeavor, unveiling the compelling reasons that drive the design of energy-efficient analog circuits tailored for these applications.

The emergence of the Internet of Things has revolutionized the way we interact with our environment, promising a future where everyday objects, from smart appliances to industrial sensors, are interconnected and endowed with the ability to communicate and respond to our needs autonomously. This transformative paradigm shift hinges on the power of interconnected devices that can function for extended periods on a single battery charge or even harness energy from their surroundings. Low Power Analog Circuit Design stands as the linchpin, enabling these IoT devices to operate efficiently, thereby reducing the burden of frequent battery replacements and fostering a sustainable, interconnected world. The significance of IoT becomes evident when considering Fig. 1.1, illustrating the substantial growth in IoT demands over the recent years and projecting further exponential expansion in the near future.

In parallel, the realm of Biomedical Applications is witnessing a revolution of its own as technology plays an increasingly central role in healthcare and medical research. Wearable health monitors, implantable medical devices, and portable diagnostic tools are becoming indispensable in our quest for improved health and well-being. These applications necessitate analog circuits that operate with remarkable efficiency and ultra-low power consumption, enabling the continuous monitoring of vital signs, drug delivery, and precise diagnostics while minimizing the physical and physiological impact on patients.

This thesis sets out to uncover the intricate design considerations, innovative techniques, and holistic system-level optimizations that underpin Low Power Analog Circuit Design for IoT and Biomedical Applications. It explores the unique challenges posed by these domains, ranging from the need for

extended battery life and energy harvesting in IoT devices to the stringent power constraints and biocompatibility requirements in biomedical contexts.

Through a comprehensive examination of the design principles, the significance of this thesis becomes apparent. It addresses the pressing demands of our increasingly connected world and the ever-advancing field of healthcare technology, where efficient, low-power analog circuits have the potential to not only enhance the functionality of devices but also improve the quality of life for individuals. This journey seeks to unlock the true potential of IoT and Biomedical Applications, offering solutions that are not only technologically advanced but also environmentally sustainable and human-centric.

1.2 Applications of IoT

The Internet of Things (IoT) has emerged as a transformative force, reshaping the way we interact with technology and our surroundings. In this era of connectivity, IoT applications have permeated various aspects of our lives, from healthcare to agriculture, industrial monitoring, and urban development. One common thread that runs through these diverse applications is the demand for ultra-low power analog circuit design.

1. Wearable Health Monitors

- Designing low-power analog circuits for wearable health monitors involves creating sensors and signal conditioning circuits that continuously and accurately track vital signs such as heart rate, ECG (electrocardiogram), and blood pressure.
- Achieving ultra-low power consumption is crucial to extend the device's battery life and minimize the need for frequent charging.
- Investigating efficient data transmission methods ensures real-time monitoring while conserving energy.

2. Implantable Medical Devices

- Developing ultra-low-power analog circuits for implantable medical devices encompasses the design of circuits that can operate within the strict power constraints of the human body.
- Biocompatibility is a significant consideration, ensuring that the device does not harm the patient and operates reliably over extended periods.
- Efficient power management is essential to extend the lifespan of the implant and reduce the need for surgical replacements.

3. Environmental Sensing

- Creating low-power analog sensors for environmental monitoring involves designing sensors to measure parameters like air quality, temperature, humidity, and pollution levels.

- Minimizing power consumption is essential for long-term deployments of environmental sensors, especially in remote or challenging locations.
- Reducing power usage during data transmission helps maximize the operational life of these sensors.

4. Smart Agriculture

- Designing analog circuits for smart agriculture includes creating sensors for monitoring soil moisture, weather conditions, and crop health.
- Power optimization is critical for sensors deployed across large agricultural areas, where frequent battery replacement may not be practical.
- Efficient energy usage in remote agricultural settings can be achieved through energy harvesting or extended battery life.

5. Energy Harvesting

- Investigating low-power analog circuitry for energy harvesting explores the design of circuits that can efficiently collect and store energy from sources like solar panels, vibrations, or temperature differentials.
- Ensuring power-efficient energy transfer and storage is essential to maximize the utility of harvested energy, especially in low-power IoT applications.

6. Asset Tracking

- Developing energy-efficient analog circuits for asset tracking involves creating devices that monitor the location, condition, and status of valuable assets such as goods in transit or equipment.
- Extending the operational life of tracking devices by minimizing power consumption is a key goal.
- Balancing real-time tracking requirements with energy efficiency is crucial to maximizing battery life.

7. Smart Building Systems

- Designing low-power analog circuits for smart buildings includes sensors for occupancy detection, lighting control, and HVAC (heating, ventilation, and air conditioning) systems.
- Power optimization is essential for devices that need to operate for extended periods in commercial or residential settings.
- Using efficient communication protocols reduces the energy required for building automation.

8. Industrial IoT (IIoT)

- Creating ultra-low-power analog circuitry for IIoT involves designing sensors and monitoring devices for industrial applications.
- Reducing maintenance requirements and the need for frequent battery replacements is essential for devices operating in industrial environments.
- Ensuring reliable operation with minimal power consumption is critical for IIoT devices.

9. Smart Cities

- Developing analog circuits for urban infrastructure monitoring includes creating sensors for smart streetlights, waste management, and parking systems.
- Power optimization ensures that these devices can operate continuously, providing real-time data for urban management.
- Efficient energy usage contributes to the sustainability of smart city deployments.

10. Home Automation

- Designing low-power analog circuits for home automation devices involves creating sensors and controllers for applications such as smart locks, thermostats, and security cameras.
- Maximizing energy efficiency helps extend battery life or reduce the need for frequent recharging in battery-powered devices.
- Efficient communication and data processing are essential for real-time and reliable home automation.

11. Agricultural IoT

- Developing energy-efficient analog circuitry for precision agriculture includes sensors for monitoring soil conditions, irrigation control, and crop health.
- Efficient power management is crucial for agricultural IoT devices, especially in remote and large-scale farming operations.
- Energy-efficient solutions can reduce the environmental impact of agricultural practices.

12. Wildlife and Environmental Conservation

- Creating low-power analog circuits for wildlife and environmental conservation involves designing tracking devices for wildlife monitoring and sensors for environmental data collection.
- Minimizing power consumption is essential to avoid disturbing wildlife and to enable long-term, unattended environmental monitoring.

- Energy-efficient solutions are critical for preserving natural ecosystems and studying wildlife behavior.

These applications provide a rich and varied landscape for exploring ultra-low power analog circuit design within the context of IoT for an MS thesis. Each application offers distinct challenges and opportunities for innovative and sustainable solutions.

1.3 Motivation and Application of Low Power Resistance-to-Digital Converter (RDC) Design for IoT and Biomedical applications

1. Extended Device Operation

The combined motivation of using Resistance to Digital Converters (RDC) and ultra-low power voltage and current reference designs is to significantly extend the operational life of electronic devices. By minimizing power consumption in both RDC and reference circuits, devices can operate for prolonged periods without frequent energy replenishment, reducing the need for maintenance and enhancing user convenience.

2. Energy Efficiency

The integration of RDC and ultra-low power references contributes to overall energy efficiency in electronic systems. By optimizing power usage in both analog-to-digital conversion and voltage/current referencing, devices become more sustainable, aligning with global efforts to reduce energy consumption and promote environmentally friendly practices.

3. Precision and Stability

Both RDC and ultra-low power references play a crucial role in maintaining precision and stability in electronic systems. The accurate conversion of analog signals by RDCs and the stable generation of reference voltages/currents are essential for reliable and accurate measurements in various applications.

4. Miniaturization and Portability

The motivation extends to creating compact and portable devices by utilizing both RDC and ultra-low power reference designs. This is particularly important for applications in wearables, IoT devices, and portable electronics, where space and weight constraints are significant considerations.

5. Versatility and Ubiquity

The motivation lies in creating versatile designs that can adapt to a wide range of applications. The combination of RDC and ultra-low power references provides flexibility and compatibility with diverse electronic systems, making them suitable for various industries and use cases.

Applications In IoT

1. IoT Sensors and Devices

Utilize RDC and ultra-low power references in IoT sensors for energy-efficient and accurate data acquisition. This is crucial for devices deployed in remote locations or with limited access to power sources, ensuring prolonged operation without frequent battery changes.

2. Wearable Electronics

Integrate RDC and ultra-low power reference designs in wearables such as health monitors and fitness trackers. This combination enables precise biometric measurements while maintaining an extended battery life, enhancing the usability of wearable devices.

3. Wireless Sensor Networks

Implement RDC and ultra-low power references in wireless sensor networks to optimize power management. This ensures that devices can communicate efficiently over extended periods without exhausting energy reserves, a key requirement for IoT applications.

4. Energy Harvesting Systems

Apply RDC and ultra-low power references in energy harvesting systems to efficiently convert and utilize harvested energy. This supports the sustainability of autonomous IoT devices, enhancing their ability to operate in remote or off-grid locations.

5. Smart Building Systems

Integrate RDC and ultra-low power references into IoT devices for smart building applications. This includes occupancy sensors and environmental monitors, contributing to energy-efficient building management by reducing overall power consumption.

6. Industrial IoT (IIoT)

Deploy RDC and ultra-low power references in IIoT sensors for industrial applications. This combination supports predictive maintenance strategies, reduces downtime, and optimizes overall operational efficiency in industrial settings.

In Biomedical Applications

1. Wearable Health Monitors

Implement RDC and ultra-low power references in wearable health monitoring devices. This combination enables continuous and accurate monitoring of biopotentials and other health parameters while preserving battery life for prolonged use.

2. Implantable Medical Devices (IMDs)

Integrate RDC and ultra-low power references into implantable medical devices such as pacemakers and neurostimulators. This ensures long-lasting operation within the human body with minimal power consumption, reducing the need for frequent device replacements.

3. Point-of-Care Diagnostics

Utilize RDC and ultra-low power references in portable diagnostic devices for real-time measurements. This application is essential for providing rapid and accurate diagnostics in remote or resource-limited settings, improving healthcare accessibility.

4. Biopotential Measurement

Apply RDC and ultra-low power references in devices for continuous and non-invasive monitoring of biopotentials like ECG and EEG. This combination ensures accurate data collection, supporting healthcare professionals in making informed decisions.

5. Precision Medicine Devices

Integrate RDC and ultra-low power references into devices for precision medicine applications. This includes devices for monitoring specific biomarkers or administering personalized treatments, where accuracy and energy efficiency are paramount.

6. Rehabilitation and Assistive Devices

Implement RDC and ultra-low power references in devices for rehabilitation and assistive purposes. This combination enables the development of energy-efficient devices that aid in rehabilitation processes or assist individuals with specific medical conditions.

The combined application of RDC and ultra-low power voltage and current reference designs offers a comprehensive solution for diverse industries, emphasizing energy efficiency, precision, and longevity in electronic systems.

1.4 Thesis Organization

In this manuscript, we presented an ultra-low power Resistance-to-Digital Converter (RDC). As a system, the RDC can be configured differently and can be used in different low-power sensors like temperature sensors, pressure sensors, touch sensors, humidity sensors, radiation dosimeters, etc. Almost every Analog to Digital Converters like RDC, Capacitance-to-Digital Converters (CDC), RC to Digital Converter uses various Voltage references as an input to comparators, Operational Transconductance Amplifiers (OTA), and Voltage buffers. Whereas temperature-compensated current references are used to bias almost all the sub-blocks inside the system. In general, These blocks always remain on so as to avoid the start-up delay and long settling time. So, it's essential to design these blocks with ultra-low power consumption.

In Chapter 2, we presented a 162nW ultra-low power Resistance-to-Digital converter that works for a high input resistance range of 50k-1MΩ. This makes the RDC reconfigurable to work as different types of sensors like Temperature sensors, Pressure sensors, Humidity sensors, Radiation dosimeters, etc. The whole system works at 162nW, and it's designed in such a way that over the whole resistance range, the power consumption remains constant. The comparator is also designed in nW power, so generally, it's affected by a large delay. In the proposed architecture, the comparator delay is cancelled digitally by using an up-down counter. It achieves an impressive Figure of Merit (FoM) of 0.845 pJ/conversion cycle. Also, it obtains a temperature sensitivity of 26.9ppm/$\circ$C from -40 to 100$\circ$C. Compared with the state-of-the-art RDCs, this work improves the FoM and temperature sensitivity by 42.91% and 11.52%, respectively.

In Chapter 3, we covered the understanding and the functionality of the always-on blocks. From a system-level point of view, the importance and stringent conditions required for designing are discussed in this section. Different methods of temperature compensation for both Current and Voltage References, as well as methods to make the references supply-sensitive, are discussed in this section.

In Chapter 4, we discussed a novel nW range gate-leakage-based Sub-Bandgap Voltage Reference (sub-BGR) for low-power and high-temperature range IoT applications. As bandgap references are

one of the most reliable architectures that show a lesser process, supply, and temperature dependency, it is constructive to design BJT-based references. It generates a reference voltage of 336mV without incorporating any resistors and works for a wide temperature range of -40°C to 150°C. It also works for low and wide voltage levels starting from 0.7V to 4V. In the above temperature and supply ranges, the proposed circuit's power consumption only goes up by 30x and 1.025x times, respectively. Designed in a 65nm CMOS process, the proposed architecture achieves an accuracy of 94ppm/∘C. It achieves a line sensitivity of 0.0066%/V for a supply range of 0.7V to 4V and a PSRR of 89dB at DC and 1V supply.

In Chapter 5, presents a trim-free, low-power, and high-precision voltage/current reference for IoT and biomedical applications. The voltage reference is generated by the proper addition of CTAT and PTAT voltages, whereas, the current reference is generated using a MOSFET in the active region, which acts like a resistor and helps in lowering power consumption without increasing the form factor. Implemented in the 90nm CMOS process, the proposed voltage/current reference outputs a voltage and current of 820mV and 3.23nA, respectively. Without trimming, the process variation of the proposed voltage/current reference is $1.34\%(\sigma/\mu)$ / $1.75\%(\sigma/\mu)$ and the temperature coefficient of the voltage/current reference is 62ppm/^{o}C / 332ppm/^{o}C over the temperature range of -40^{o}C to 100^{o}C. The line sensitivity of the voltage/current reference is 0.296%/V / 0.414%/V for a wide supply range of 1V - 3.5V. The area occupied by the total circuit is 0.0112mm^2, while the total power consumption of the design is 37nW at the typical corner of 27^{o}C and 1V supply.

In Chapter 6, we summarised all of our work and discussed the future scope of improvements over similar circuits and system-level designs.

Chapter 2

A 162nW, 0.845pJ/step Resistance-to-Digital Converter for Miniature Battery-Powered Sensing Systems

2.1 Introduction

The Internet-of-Things (IoT) application space is rapidly growing and has emerged as a newer form of computing in recent times. The trend of scaling both power & area for these new computing systems led to the development of miniaturized ultra-low-power resistive sensors to measure physical signals such as pressure, temperature, force, concentration, etc. In addition to lower power/energy per conversion cycle and lower form factor, these sensors are desired to have good linearity, wide input range, and also immune to supply and temperature variations.

With the proliferation of battery-powered and energy-harvesting devices in various fields, the demand for ultra-low power analog-to-digital converters (ADCs) has become increasingly critical. These devices require efficient conversion of analog signals into digital representations while minimizing power consumption. Traditional ADC architectures often struggle to meet these stringent power requirements, necessitating the exploration of alternative approaches. In this context, the ultra-low power resistance-to-digital converter (RDC) emerges as a promising solution

Unlike traditional ADCs, which utilize capacitor-based circuits, RDCs rely on the conversion of resistance variations to digital codes. This novel approach opens up possibilities for enhanced performance, improved power efficiency, and reduced circuit complexity. Various circuit topologies, signal processing techniques, and calibration methods will be explored to optimize the performance of resistance-based ADCs. Special attention will be given to mitigating potential sources of error, such as nonlinearity, and temperature effects, which can degrade the accuracy and reliability of the conversion process. This study focuses on ultra-low power RDCs with high resistance range, so that it supports reconfigurability of ultra-low power RDCs in practical scenarios. The compatibility of RDCs with various sensing elements, such as resistive sensors, pressure sensor, and temperature sensors, will be investigated to assess their versatility and effectiveness in different applications. Through a systematic exploration of the underlying principles, design considerations, and practical implementations, this re-

search aims to enable the development of ultra-low power, high-performance RDCs that can meet the evolving demands of modern applications.

Next, the fundamental operating principles and key components of ultra-low power resistance-to-digital converters will be presented. The unique characteristics of resistance-based conversion techniques, such as their inherent low-power nature and potential for high-speed operation, will be discussed. Moreover, strategies for minimizing power consumption in RDCs, such as optimized circuit architectures, low-leakage techniques, and advanced delay cancellation techniques, will be explored.

By exploring the principles, design considerations, and practical implementations of ultra-low power RDCs, this research strives to facilitate the development of energy-efficient ADCs that can meet the stringent power requirements of emerging battery-powered and energy-harvesting applications.

2.2 Literature Survey

Conventionally, resistance is transduced to an analog voltage, and high precision ADCs (like DSM) [7] were used to convert it to digital code. Although these sensors achieve good resolution, their power consumption and energy per conversion cycle (FoM) are much higher for most IoT applications. Duty cycling is a widely adopted technique [8, 9] to reduce the average power consumption of the circuits. Although this technique reduces the average power and energy conversion per cycle, higher instantaneous power in the order of micro-watt poses the following challenges a) Higher source resistance of a miniaturized battery contributes to higher voltage drop [10] b) Power generated by an energy harvesting unit (photo voltaic cells, RF energy harvesting, etc.) cannot support the high instantaneous current [11].

A power-efficient approach is to transduce resistance to time/frequency and translate it to a digital code [2, 3, 4, 5, 12, 13]. Although [8, 5] and [12] report lower power, these architectures suffer from other limitations like higher form factor, non-linearity, and lower input range. For example, [5] uses an off-chip capacitance (in nF) to increase conversion time and reduce power consumption, but it compromises area and cost. Time/frequency-based resistance-to-digital converters (RDC) are inherently expected to have a higher input range to have reconfigurability to accommodate different resistive sensors. However, [5] reports a lower input range, and [2] reports a high range using a high external resistance (R_S) at the expense of low sensitivity at high sensor resistances, area, and cost. Although [4] reports operation for large resistances, but doesn't report FoM for any such values. Architecture in [2],[3], and [4] suffers from increased non-linearity, resolution limitation due to limited noise shaping, and high power consumption due to the voltage-controlled oscillator.

2.2.1 Voltage/Current mode sensor interface circuit

Fig. 2.1 shows the general architecture of the voltage/current mode sensor interface circuits. Digital circuits take advantage of technology scaling and reduce power consumption, delay, silicon area, cost,

etc. However, as supply voltage reduces with scaling, the dynamic range of such voltage/current mode sensor gets limited. Moreover, such types of architectures need sophisticated noise cancellation techniques and use complex structures, which results in high power consumption and directly contradicts our requirement for ultra-low power operation.

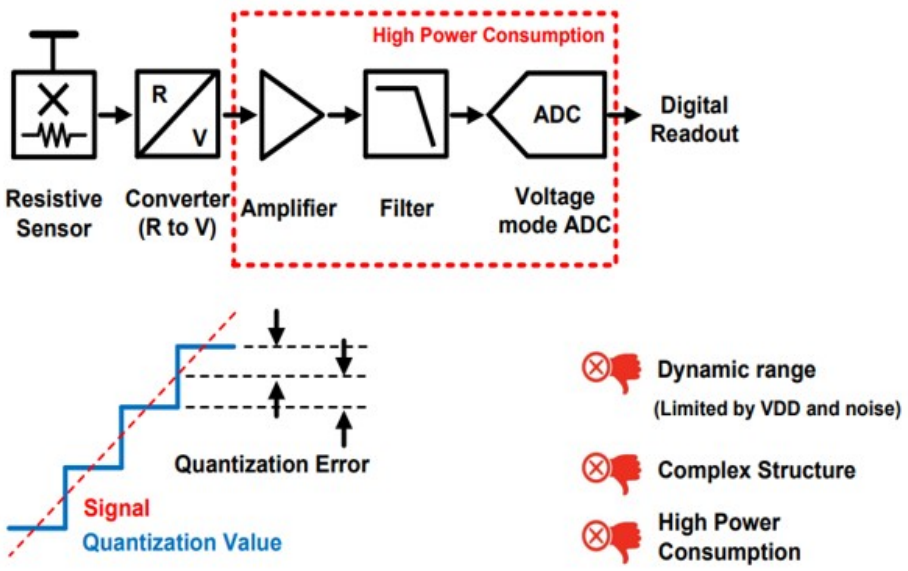

Figure 2.1: Voltage/Current mode sensor interface circuit [2]

2.2.2 Time/Frequency mode sensor interface circuit

Fig. 2.2 shows the general architecture of time/frequency mode sensor interface circuits and its general advantages over voltage/current mode architectures for low-speed, high-resolution applications. In order to achieve high resolution and dynamic range, just the enable time can be increased, which also reduces the residue over time. It achieves high SNR by time averaging of noise. Due to comparatively simpler architecture, it can be designed for ultra-low power regimes. For all the above-mentioned reasons, we chose the time/frequency mode architecture over voltage/current mode sensors.

Now between time and frequency mode architectures, frequency mode architectures generally use a VCO or ring oscillator whose frequency gets decided by the sensor resistance. These architectures, as shown in Fig. 2.3, and Fig. 2.4 consume in the order of tens and hundreds of μW range. Typically in these low-power systems, energy is provided by miniaturized batteries or energy harvesters. Higher source resistance of miniaturized batteries results in a greater voltage drop. Also, energy harvesters like photo voltaic cells and RF energy harvesters cannot support such high currents. To get a further reduction in power consumption, time-based architecture is explored in this study.

Some time-based low-power architectures, such as [5] take power in nW, but as shown in Fig. 2.5, uses 6.1nF external off-chip capacitor to generate a higher time pulse, i.e., to achieve more dynamic

range. Moreover, it incorporates an external off-chip voltage reference circuit, which ends up increasing the cost significantly.

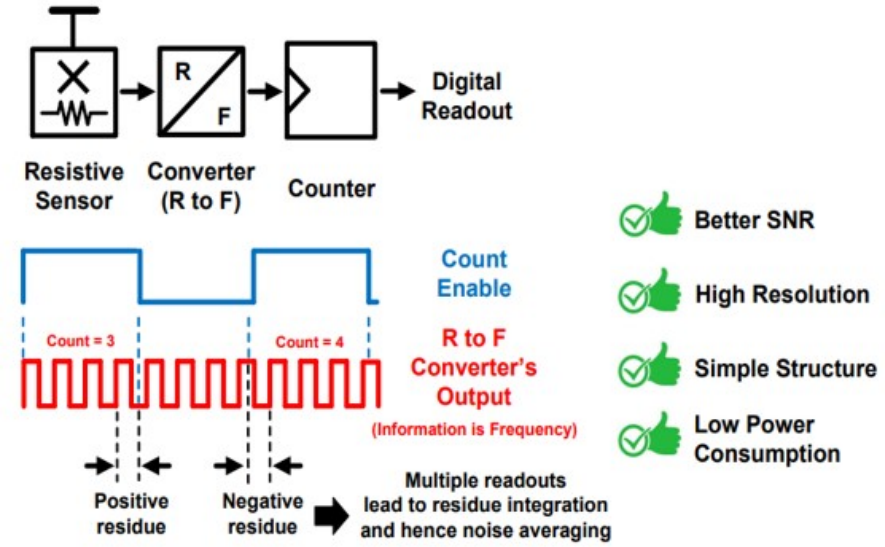

Figure 2.2: Time/Frequency mode sensor interface circuit [2]

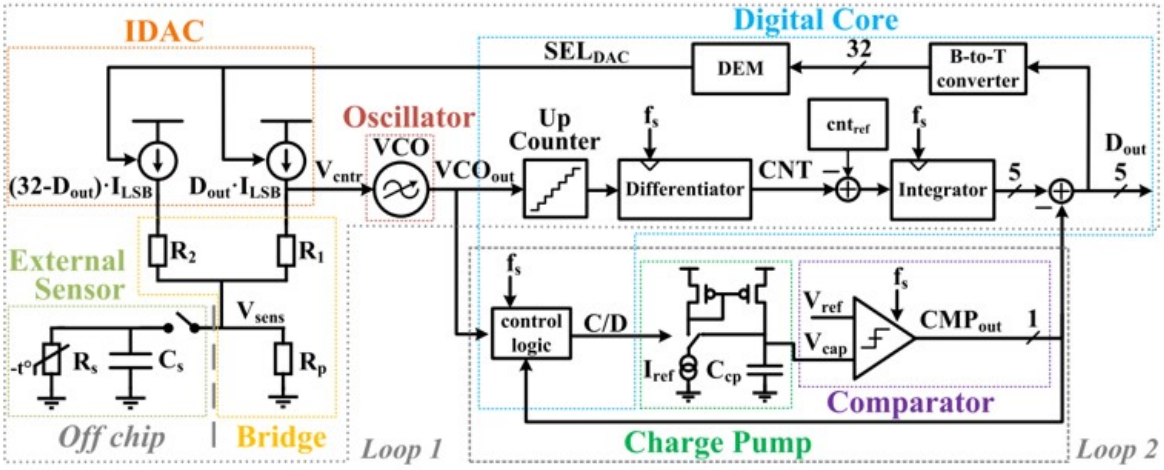

Figure 2.3: VCO based frequency mode sensor interface circuit [3]

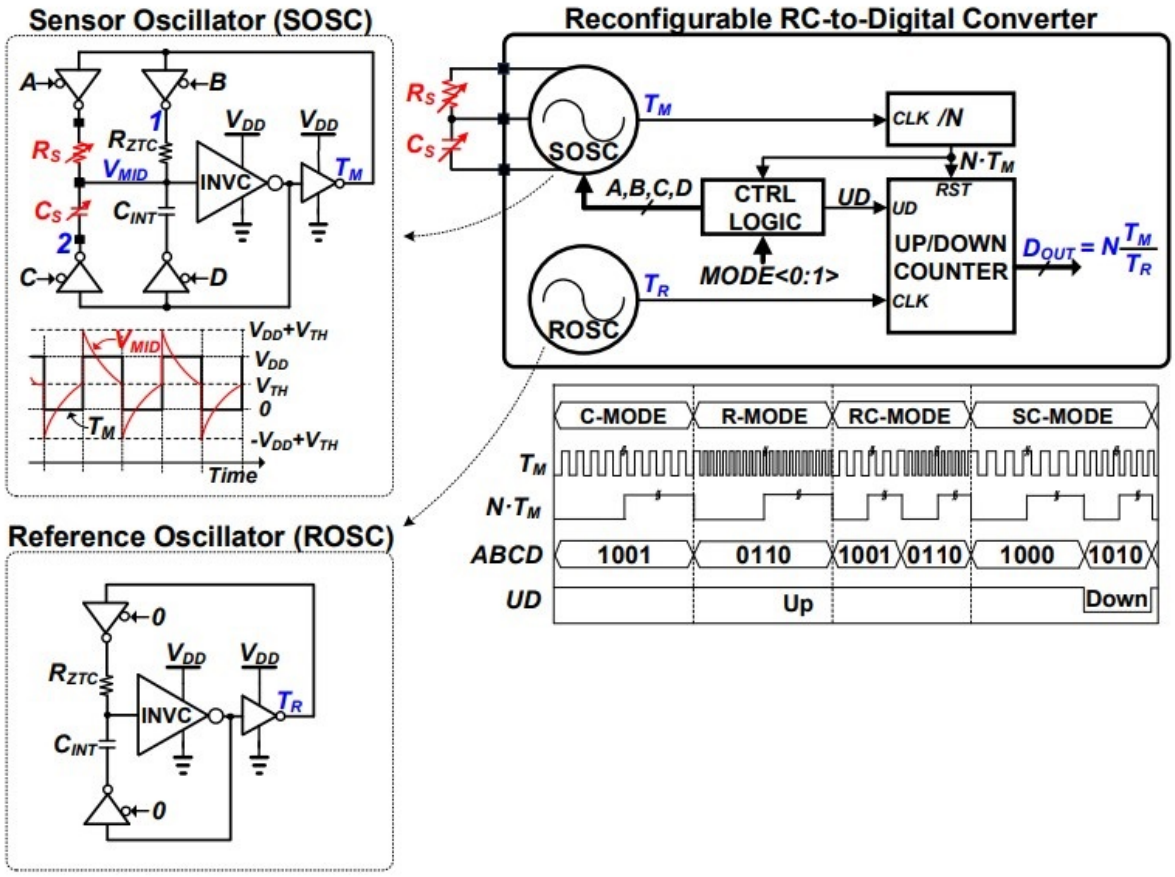

Figure 2.4: Frequency mode sensor interface circuit [4]

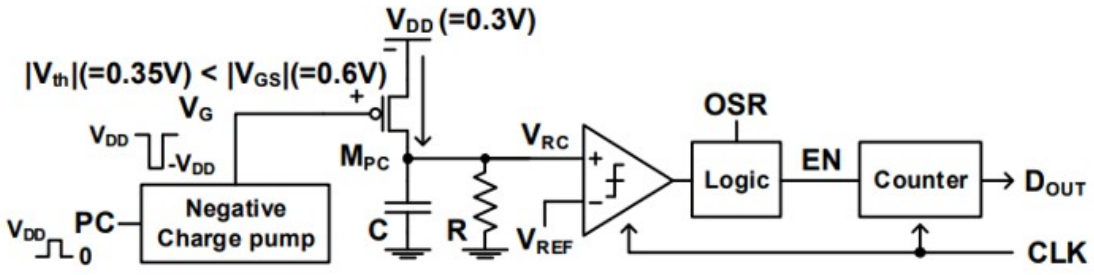

Figure 2.5: Time mode sensor interface circuit [5]

In this architecture, as shown in Fig. 2.6 resistance is converted to a time pulse, and it creates two pulses of different widths depending on the sensor resistance. To eliminate the delay associated with the comparator due to ultra-low power design architecture, an up-down is implemented to subtract these two pulses digitally. The detailed operation and design of the proposed RDC are discussed in the subsequent sections.

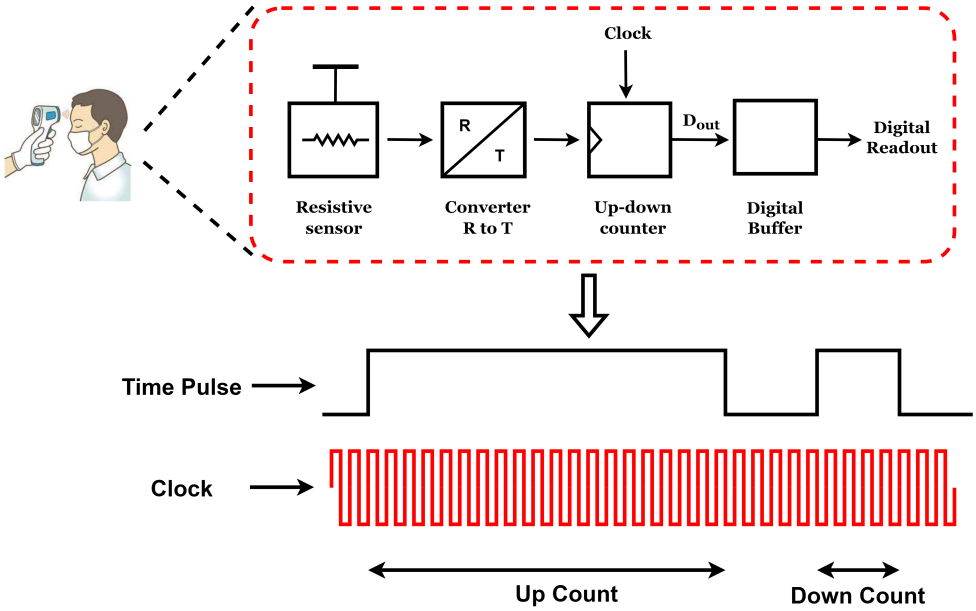

Figure 2.6: Design of time mode sensor interfacing circuit

2.3 System-level architecture of the Proposed RDC

Fig. 2.7 shows the block diagram and the basic building blocks of the proposed time-based RDC. Here the resistive sensor (R) is inside the beta multiplier circuit. The beta multiplier generates current I, depending on the value of the sensor resistance, and $1/5^{th}$ of this current, i.e., I_{cap}(=I/5), is mirrored to charge the capacitor C_1.

The beta multiplier current (I) can be expressed by,

$$I = \frac{V_{gs_1} - V_{gs_2}}{R} = \frac{V_{res}}{R} \tag{2.1}$$

Where R represents the sensor input resistance. If t specifies pulse width up to when capacitor C_1 charges, i.e., the first pulse at the comparator output. Then capacitor voltage (V_{cap}) can be expressed in the following way,

$$V_{cap} = \frac{I_{cap}}{C_1} \int dt = \frac{I}{5C_1} \times t = \frac{V_{res}}{5RC_1} \times t \tag{2.2}$$

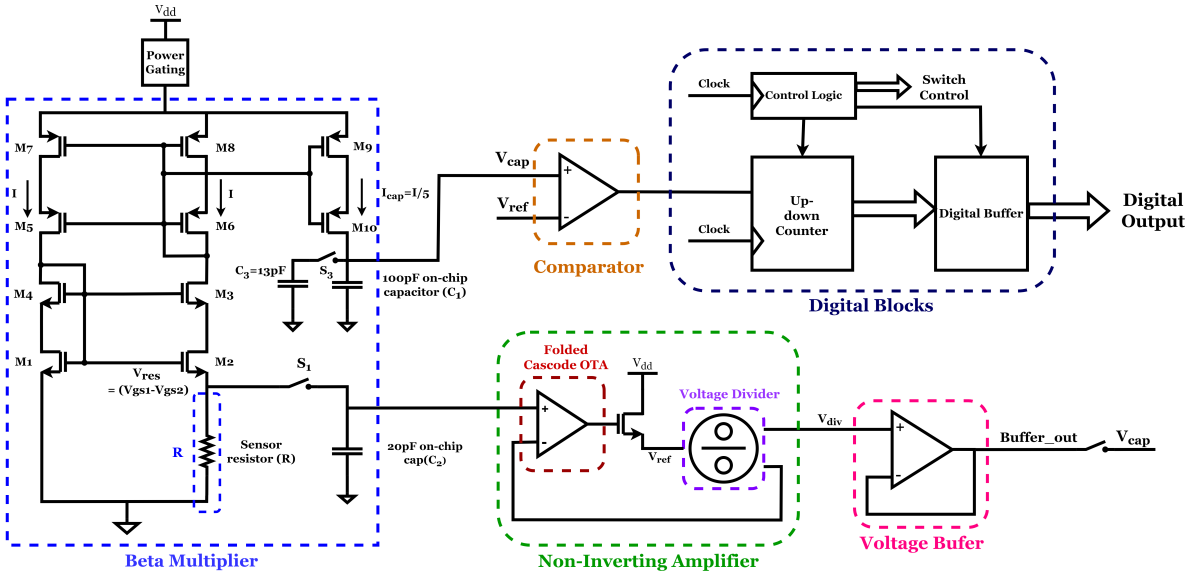

Figure 2.7: Block Diagram of the proposed RDC

Beta multiplier consumes high power for small sensor resistances, but the circuit will be operational for a shorter time. Thus, power gating is implemented to obtain lower average power.

To eliminate the temperature dependency and non-linearity of V_{cap}, the same voltage (V_{res}) that is being used to charge the capacitor is amplified (V_{ref}) and being compared with V_{cap} at the comparator input. The non-inverting amplifier is implemented to achieve a gain Av(=50), uses a 3-stage folded Cascode OTA, and 50 diode-connected NMOS transistors connected in series as a voltage divider. For offset cancellation, auto-offset calibration [14] is incorporated in the folded cascode OTA.

The non-inverting amplifier output i.e. the reference voltage (V_{ref}) can be expressed as

$$V_{ref} = A_v \cdot V_{res} \tag{2.3}$$

As we equate V_{cap} and V_{ref} at the comparator input, we get the expression for the pulse width generated for a given sensor resistance.

$$t = A_v \cdot 5RC = 250 \cdot RC \tag{2.4}$$

Thus, pulse width only depends on the resistance (R) and 100pF on-chip capacitor (C_1). Since the proposed RDC eliminates any variation of the voltage reference circuit and due to this simple expression, the RDC measurement is independent of temperature and any other circuit parameters, which greatly improves the accuracy. For example, [5] reports a higher linearity error of 0.32% due to oversampling ratio and use of additional voltage reference. Also, the proposed RDC reports lesser temperature sensitivity than the recent works like [3, 4]. The voltage across R (V_{res}) works as the input to the non-inverting amplifier to generate the reference voltage. A 20pF on-chip capacitor (C_2) stores V_{res} to have a steady reference voltage always present for the circuit operations.

2.3.1 Non-Inverting Amplifier

The proposed RDC uses a non-inverting amplifier of gain A_v(=50) (from Fig. 2.7), generates the reference voltage (V_{ref}) by amplifying V_{res}. It consists of Folded cascode OTA (Operational Transconductance Amplifier) (Fig. 2.8), a common drain amplifier as a buffer, and a voltage divider using nmos diode-connected mosfets (Fig. 2.9). For offset cancellation, auto-offset calibration [14] is incorporated in the Folded cascode OTA. The buffer is used to supply the current required in the nmos voltage divider. As otherwise, due to the loading effect, the 2^{nd} stage gain of the Folded cascode OTA gets affected. The same voltage that is being used to charge the capacitor C_1, is amplified and used as a reference voltage at the comparator input. This eliminates all the effects of PVT variations and the usage of additional voltage reference circuitry.

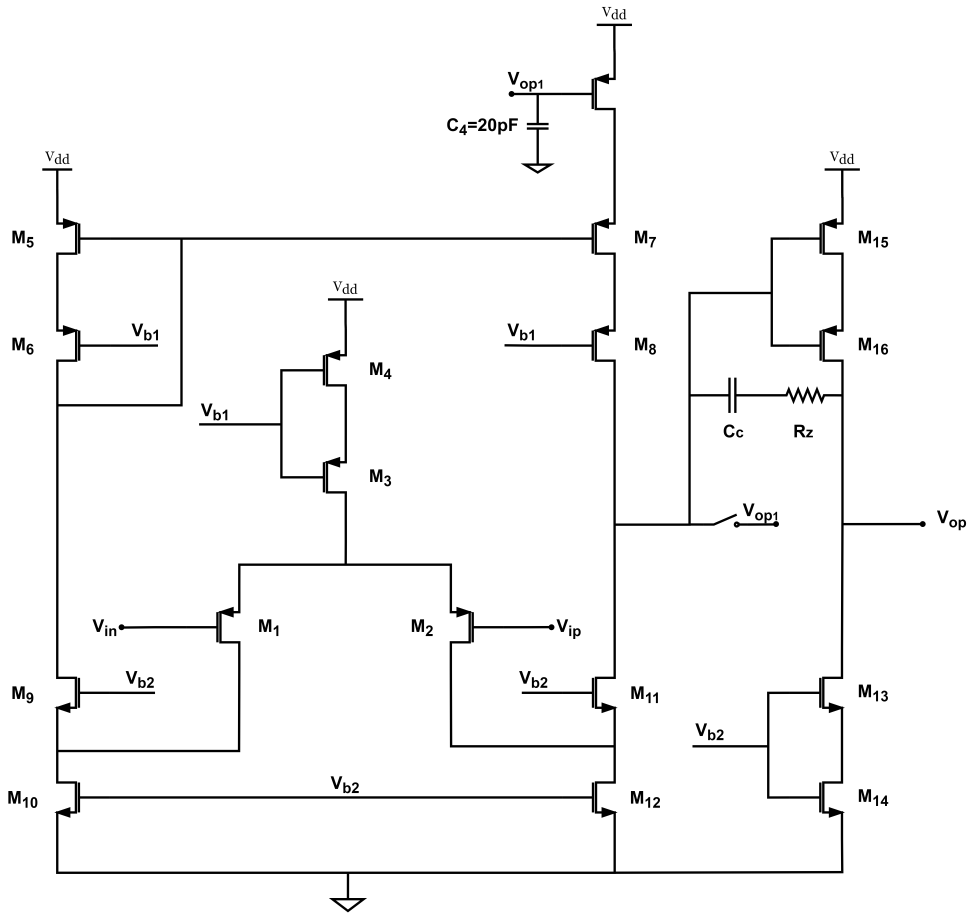

Figure 2.8: Folded Cascode OTA

2.3.2 NMOS Voltage Divider

The division ratio should be constant, i.e., it should be invariant to PVT variations. The voltage divider should also draw negligible current so that the common drain buffer stays in the proper operating region. Resistance dividers can be used as a voltage divider, however, we require large resistance to scale the current consumption of the divider, which means a higher silicon area. We can use MOS diode connected in series as dividers, which consumes negligible current consumption and gives a constant ratio independent of process, supply, and temperature variations. A voltage divider using nmos diode-connected mosfets is shown in Fig. 2.9.

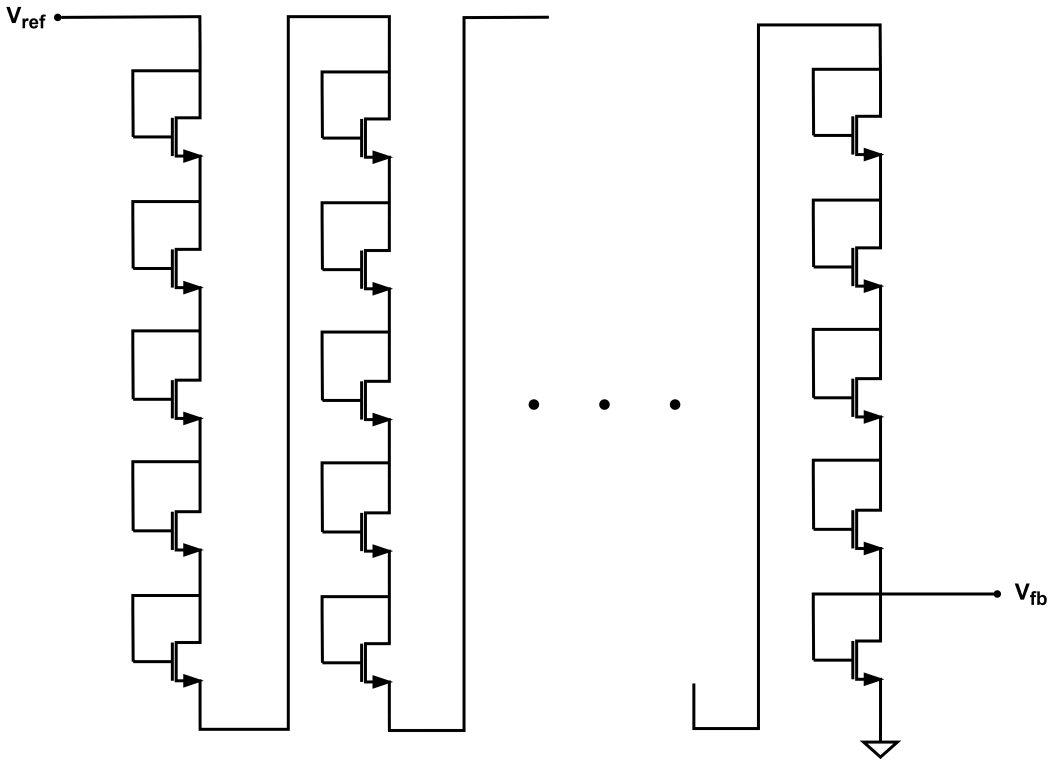

Figure 2.9: NMOS Voltage Divider

2.3.3 Delay and offset cancellation of the Always-on Comparator

In the proposed time-based RDC, an NMOS input 2-stage always-on comparator is used to generate a pulse, and the pulse width depends on the sensor resistance value. As the comparator is designed for ultra-low-power operation, it suffers from a large delay which varies significantly with PVT variations. Instead of a simple up counter, a CDS-style up-down counter is proposed to eliminate the offset and delay of the comparator.

During the first pulse generation, as soon as the comparator switches states, the beta multiplier is turned off to conserve power, and capacitor C_1 will maintain the stored voltage. After some finite time

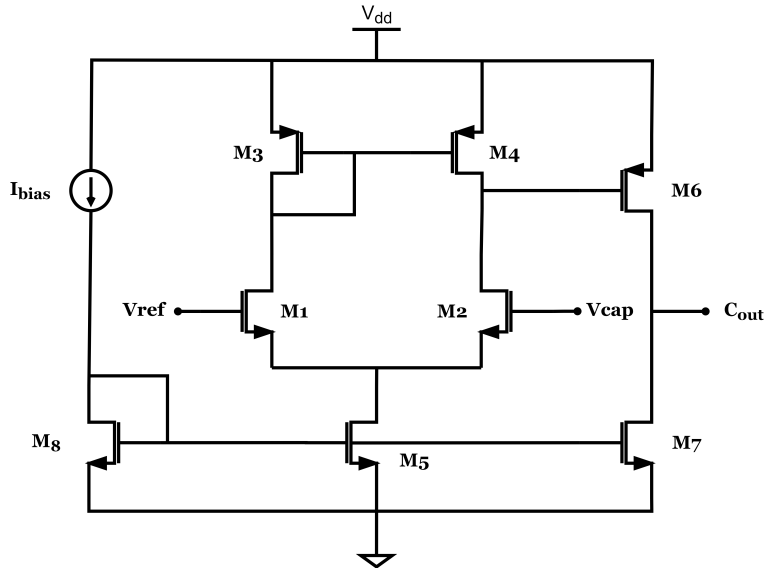

Figure 2.10: Circuit schematic of Always-on Comparator

(∼5ms, considering PVT variations), an initially discharged capacitor C_3 (=13pF) is connected to the capacitor C_1 to get it discharged instantaneously, according to the capacitance ratio. Again, the mirrored current (I/5) from the beta multiplier charges C_1 up to V_{ref} and generates a shorter pulse. This smaller pulse is similarly affected by the comparator delay and offset in the same way as the first pulse. As the proposed circuit subtracts the two pulses using an up-down counter, both the delay and offset of the comparator will be canceled, which enables the use of an ultra-low-power comparator that works at as low as 3nW. This technique eliminates the use of clocked comparator like in [3], [5] and [15], where a pre-amplifier is also needed to minimize the impact of kickback noise. Thus enabling the use of simple, ultra-low-power, always-on comparator architecture.

Defining the operations in 1^{st} and 2^{nd} pulses in C_{out} (Fig. 2.11) as phase1 and phase2. Also, V_d and V_{off} represent the delay and the offset of the always-on comparator. In phase1, the capacitor voltage can be described as

$$V_{cap} = \frac{V_{res}}{5RC_1} \times t_1 \tag{2.5}$$

At the comparator input V_{cap} will be compared with V_{ref}(=$A_v \cdot V_{res}$). Taking the offset and delay of the comparator into account, the 1^{st} pulse width t_1 can be found as follows,

$$\begin{aligned} V_{cap} &= V_{ref} + V_{off} + V_d \\ \frac{V_{res}}{5RC_1} \times t_1 &= A_v \cdot V_{res} + V_{off} + V_d \\ t_1 &= 5RC_1(A_v + \frac{V_{off}}{V_{res}} + \frac{V_d}{V_{res}}) \end{aligned} \tag{2.6}$$

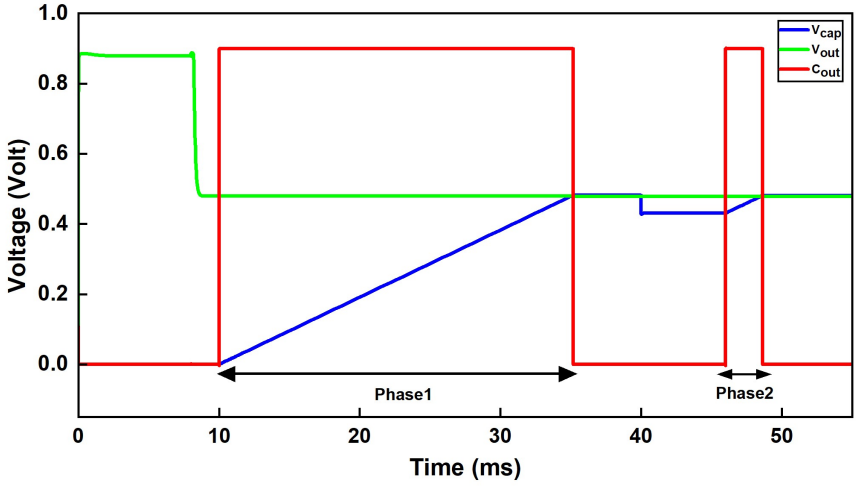

Figure 2.11: Basic RDC Operation

In phase2 with the help of capacitor C_3 and voltage buffer, C_1 is initially charged to $0.9 \cdot V_{cap}$ and the 2^{nd} pulse width t_2 can be expressed as follows,

$$\begin{aligned} 0.9 \cdot V_{ref} + V_{cap} &= V_{ref} + V_{off} + V_d \\ \frac{V_{res}}{5RC_1} \times t_2 &= 0.1 \cdot A_v \cdot V_{res} + V_{off} + V_d \\ t_2 &= 5RC_1(0.1 \cdot A_v + \frac{V_{off}}{V_{res}} + \frac{V_d}{V_{res}}) \end{aligned} \tag{2.7}$$

The up-down counter subtracts these two pulses, and the effective final pulse width Δt proportional to the sensor resistance is obtained as,

$$\Delta t = t_1 - t_2 = 225 \times RC_1 \tag{2.8}$$

e simple expression of Δt implies that it is free from all the non-linearities of the circuit components. Also, it can be affirmed that the delay and offset of the comparator are canceled. It enables the use of an ultra-low power comparator in the proposed RDC.

2.3.4 Voltage Buffer with high load driving capability

For comparator offset and delay cancellation, capacitor voltage C_1 is being discharged instantaneously to $0.9*V_{ref}$ by connecting an initially discharged capacitor C_2. An ultra-low-power 2-stage NMOS differential pair voltage buffer with high load drive capability such as C_1=100pF is used to discharge any error voltage (ΔV) due to comparator delay and PVT variations. As the buffer is only operational (i.e., connected to C_1) for a short duration of 5ms, to ensure its stability during its active stage

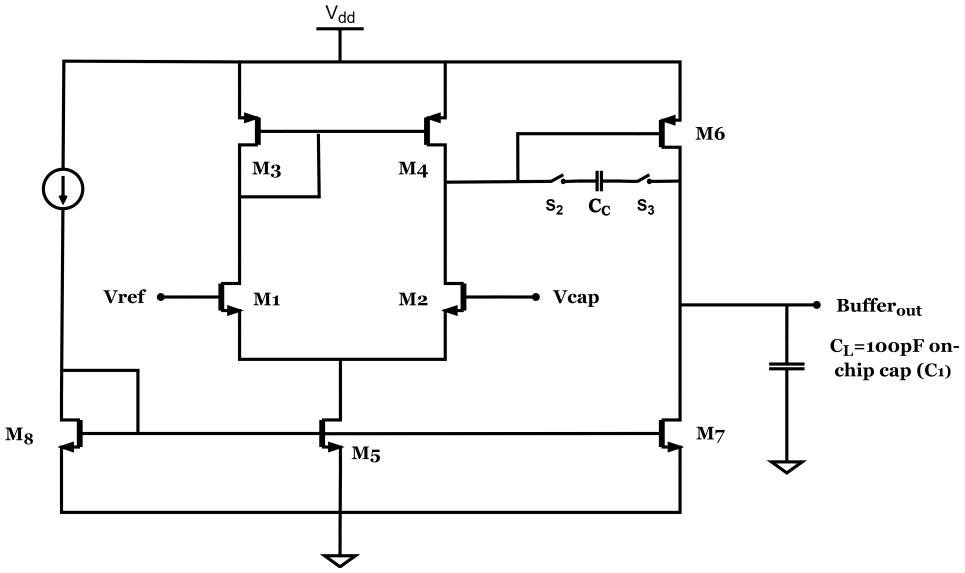

Figure 2.12: Circuit schematic of Voltage Buffer

the miller capacitor gets disconnected and pole due to C_1 ($P_2 = -\frac{g_{m6}}{C_1}$) becomes dominant. Otherwise, the miller cap remains connected and the pole due to the 1^{st} stage ($P_1 = -\frac{g_{m1}}{A_{V_2} C_c}$) becomes dominant. In this approach, the buffer can always maintain an acceptable phase margin (64.2° in active and 72.3° in sleep).

2.3.5 Proposed long Asynchronous chain Up-Down Counter

The 16-bit up-down counter is mainly responsible for converting the resistance-dependent time pulse width to the digital equivalent, it also cancels the delay and offset of the comparator. To achieve high resolution in the proposed ultra-low-power RDC, the counter needs to operate at as low frequency as possible. For this reason, we all along tried to have a higher time pulse width for a given sensor resistance. The Correlated Double Sampling (CDS) Up-Down Counter given in [16] is modified to use in the long asynchronous chain. In [16], dynamic logic is implemented for T flip-flop, but due to noise impact, it's not suitable for long-chain asynchronous operation, static logic D flip-flop is used for this purpose. An external clock of 1MHz frequency is used in the up-down counter to count for the respective time pulse.

Two-time pulses are generated and subtracted for the delay and offset cancellation of the comparator. For the 1^{st} time pulse, the counter will upcount and hold the digital output, and when the short 2^{nd} pulse appears, the counter will downcount from the hold state and finally generate the subtracted output as the final digital equivalent of the given sensor resistance (R_s).

2.4 Control Logic

As discussed in the earlier sections, the proposed RDC needs a few control signals for its proper operation, e.g.,

- Power gating the beta multiplier.
- Storing the voltage across R to a capacitor C_2.
- Discharging the capacitor (C_1) for the delay and offset cancellation of the comparator by connecting voltage buffer and capacitor C_3.
- To maintain the stability of the buffer throughout the whole operation.
- Generating the start-up pulses for the main beta multiplier and current bias circuit (Separate beta multiplier to bias all the analog circuitry).
- Two BWI (Bit-Wise-Inverter) pulses are required for the Up-Down counter.
- To generate an internal reset signal to reset all the essential blocks before the multiple RDC operations.
- Generate a 'Done' signal to indicate when digital conversion gets completed.

To make the system self-sufficient, the control signals are generated on-chip as well. A 16-bit Up counter that works for the same clock pulse and combinational logic is designed to obtain all the required control signals.

2.5 Digital Buffer

As the RDC operation gets completed, and the 'Done' signal goes low to high, the final Digital equivalent from the up-down counter will be stored in a Digital Buffer. This output will be held until again the Done signal goes from low to high. The purpose of adding the digital buffer is to reduce the capacitance of the frequent switching nodes.

2.6 System Level Simulations

The proposed design is implemented in a 180nm CMOS process. Fig 2.11 shows the system-level simulation results from the analog blocks, describing the working of the proposed RDC. Initial 10ms are required to start up the beta multiplier and cancel the offset of the folded cascode OTA. In $phase_1$ capacitor C_1 starts charging, and as it exceeds V_{ref}, we will have the 1^{st} pulse, and as described in earlier sections, in $phase_2$, a 2^{nd} short pulse is generated and gets subtracted digitally from the 1^{st} pulse

in order to cancel the delay and offset of the comparator. The proposed methodology allows for the avoidance of the usage of high power clocked comparators along with a pre-amplifier.

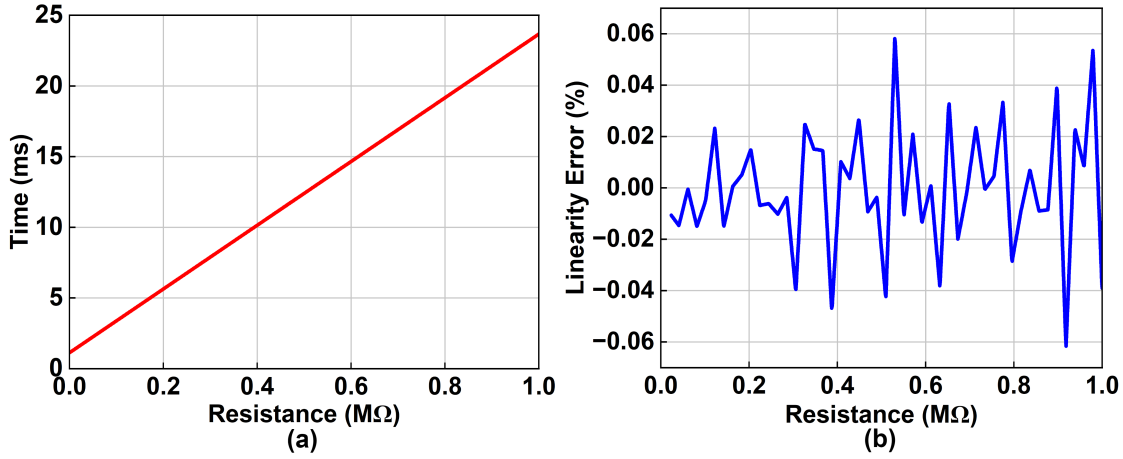

Figure 2.13: (a) Input-output characteristics. (b) % Non-linearity error

Fig. 2.13(a) shows the subtracted pulse width vs sensor input resistance (R), as R varies from 0 to 1MΩ (50kΩ internally connected). Fig. 2.13(b) depicts the percentage non-linearity error vs R, it shows that the proposed ultra-low-power RDC limits the maximum non-linearity error to 0.06% at room temperature. Further, to avoid switch non-idealities, highly linear bootstrapped switches from [17] and [18] are used precisely in the design.

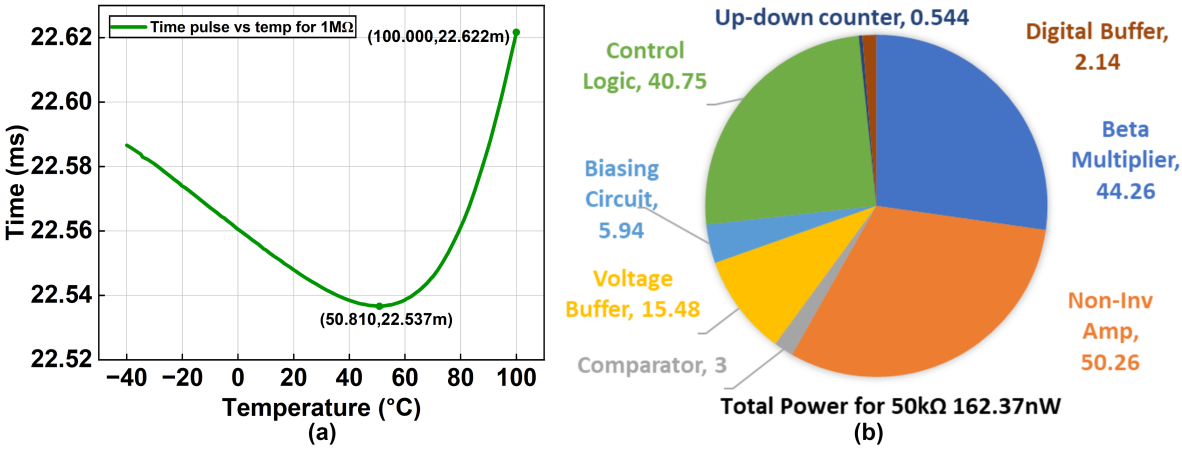

Figure 2.14: (a) Temperature sensitivity of RDC. (b) Power consumption at 50kΩ

The proposed RDC works in the ultra-low power range, and on average it consumes as low as 162.37nW and works from 900mV supply. The power consumption is almost constant w.r.t to sensor resistance. For lower input resistance, the current through the beta multiplier is higher, but the circuits operate in a shorter time. Thus, the average power consumption remains almost constant by power gat-

ing (138.24nW for 1MΩ and 162.37nW for 50kΩ). Fig.2.14(b) illustrates the power breakdown of the RDC for 50kΩ resistance. Critical parameters like Effective number of bits (ENOB) and figure-of-merit (FoM) are defined in [5], as follows

$$ENOB = \frac{20 \times \log_{10}\left(\frac{Inputrange/2\sqrt{2}}{Resolution}\right) - 1.76}{6.02} \tag{2.9}$$

$$FoM = \frac{Power \times Measurement\,time}{2^{ENOB}} \tag{2.10}$$

The proposed RDC achieves ENOB of 13.23 bits for 50kΩ in 50ms conversion time. This leads to an FoM of 0.845pJ/CS.

A few trimming circuitry is included in the RDC, e.g. in the beta multiplier for current bias, analog voltage buffer, and for the 100pF on-chip capacitor (C_1). This capacitor trimming also helps in accuracy by reducing other mismatch effects of the internal circuits of the RDC. The proposed RDC works in the ultra-low-power range. It consumes as low as 162nW and works from 900mV supply. The power consumption is almost constant w.r.t to sensor resistance. As for lower resistances, although the current through the beta multiplier would be high, but the circuit would be operational for a lower time, and due to power gating, the average power consumption will remain low.

Table 2.1: Performance summary and comparison with the state of the art

Parameter	**This work**†	JSSCC20 [3]	ISSCC17 [12]	TCAS219 [5]	VLSI18 [4]	MICRO18 [19]	EESS20 [2]	ISSCC19 [15]	ISSCC18 [8]
Technology (based)	**Pulse width**	Time (PLL)	Time (FDC)	Pulse width	SB-PM RCDC	Time (SAR)	Time (count)	Amplitude (CTSDM)	Amplitude (SAR)
Sensor type	**Internal resistor**	External resistor	Internal VCO	External resistor	Oscillator based	Internal 12-b SAR-res	Oscillator based	Internal p-resistor	External resistive bridge
Technology (nm)	**180**	180	180	65	180	180	350	180	180
Area (mm^2)	**0.64**	0.064	0.22	0.0025	0.175	0.35	0.435	0.12	1.6
Supply voltage (V)	**0.9**	—	—	0.3	1	1.8	1.75	1.8	1.2
Power (µW)	**0.162**	171	0.57	0.543	140	93.2	86.1	79	0.78
Conversion Time (ms)	**50**	0.2	8	8.64	2.93	0.92	10	10	1
ENOB (bits)	**13.23-8.91**$^{\triangleright}$	14.5	8.3	10.6	16.6	11.3	18	18.3	7.88
Temp. range (°C)	**-40–100**	-40–125	-20–100	—	—	—	—	-55–125	—
Temp. Sensitivity (ppm/°C)	**26.9**	30	N/A	N/A	64.2	N/A	N/A	N/A	N/A
Input range	**50k–1MΩ**	—	—	1k–100kΩ	15k–10MΩ*	0-2MΩ	2k–50kΩ	—	—
Off-chip component	**—**	Sensing cap	—	6.1nF, V_{ref}	—	—	Counter	—	—
FoM$_W$ (pJ/CS)	**0.845-14.36**	1.48	14.21	3.03	4.04	33	3.29	2.43	10.6
FoM$_S$ (dB)$^{\diamond}$	**159.66-133.65**	160.7	132.3	—	—	—	—	170	132.2

*FoM is reported only for 40pF cap, **2-Point trimming, $^{\triangleright}$Using non-linearity error

$^{\diamond}\mathrm{FOM_S} = \mathrm{SNR} + 10\log\left(\frac{1}{2\cdot \text{Power}\cdot t_{\text{conv}}}\right)$, †Simulation results

2.7 Comparison to the State of the Art

Table 2.1 shows the performance comparison of the proposed RDC with the state of the arts. The proposed RDC has the least power consumption of 162nW among all the RDCs. Along with the high input range, it achieves an excellent temperature sensitivity of 26.9ppm/°C for the high-temperature range of -40 to 100°C (Fig.2.14(a)). The proposed RDC consists of all on-chip components and takes around the area of 0.64mm^2. It has fairly comparable FoM$_W$ and FoM$_S$ with the state of the arts considering the resistance range. In RDCs with lower input ranges like [5] and [2] and with higher input ranges such as [19] report FoM$_W$ as 3.03pJ/CS, 3.29pJ/CS and 33pJ/CS respectively, which is significantly higher than the reported FoM$_W$ of 0.845-14.36pJ/CS.

2.8 Summary

This paper presents a novel time-based ultra-low-power RDC, that achieves high energy efficiency with the least power consumption and high resolution. In the proposed design, the delay and offset of the always-on comparator are cancelled digitally. Designed in a 180nm CMOS process, the proposed RDC consumes as low as 162nW with a measurement time of 50ms at a supply voltage of 900mV. The proposed architecture works for the large resistance range of 50k-1MΩ, with a wide temperature range of -40 to 100°C, achieves an ENOB of 13.23 bits at 50kΩ, leading to a FoM$_W$ of 0.845pJ/CS.

Chapter 3

Always-on Blocks and the Functionality of Voltage and Current References

3.1 Introduction

The domain of Internet of Things (IoT) applications is rapidly evolving, with numerous applications generating considerable interest, as highlighted in the preceding chapter. As previously mentioned, IoT nodes typically operate within the constraints of micro-fabricated batteries with limited energy storage capacities, often as low as, owing to their compact size. This imposes a critical constraint on power consumption, directly influencing the system's overall lifespan. To mitigate energy limitations, systems resort to aggressive duty-cycling to reduce average power consumption. However, the efficacy of duty-cycling relies heavily on significantly reducing the power consumption of the always-on blocks. This thesis delves into the design of two pivotal always-on analog blocks: voltage reference, current reference, and analog temperature sensor. To comprehend how to design these blocks effectively, it is essential to gain insights into their functionalities, which will be expounded upon in the subsequent sections of this chapter.

3.2 Voltage Reference

A voltage reference serves as a crucial component that produces a voltage resilient to variations in process, supply, and temperature (PVT). Such a voltage reference is imperative in analog systems like ADCs/DACs, voltage regulators, and flash memories. Despite the essential need for a stable voltage reference in semiconductor technology, no electrical quantity is entirely independent of PVT variations. The generation of a voltage reference involves combining two quantities with opposite temperature dependencies or subtracting two quantities with similar temperature dependencies. The analysis of these operations is simplified when linear dependencies are considered. Quantities that increase or decrease concerning temperature are termed Proportional-to-absolute-temperature (PTAT) and Complementary-to-absolute-temperature (CTAT), respectively.

$$V_{ref} = \begin{cases} M_1 V_{PTAT} + M_2 V_{CTAT} \\ M_1 V_{PTAT1} - M_2 V_{PTAT2} \\ M_1 V_{CTAT1} - M_2 V_{CTAT2} \end{cases} \tag{3.1}$$

3.3 Methods of Generating PTAT Voltage

1. Basic Principle

- PTAT voltage is designed to vary proportionally with absolute temperature. The fundamental idea is to use a component or circuit that changes its characteristics with temperature in a proportional manner.

2. Diode-Based Approach

- Silicon diodes exhibit a voltage-temperature relationship that is roughly proportional to absolute temperature. Utilizing diodes in series or parallel can create a PTAT voltage.
- The voltage across a diode is given by the Shockley diode equation, which has a temperature-dependent term.

2. Bipolar Transistor-Based Approach

- Bipolar transistors can be configured to exhibit a PTAT voltage characteristic.
- A common method involves using a pair of transistors with different emitter areas, as the thermal voltage term varies with the area.

3. Current Mirrors

- PTAT voltage can be generated by employing current mirrors with transistors having different emitter areas. The resulting output voltage is proportional to the absolute temperature

3.4 Methods of Generating CTAT Voltage

1. Basic Principle

- CTAT voltage is designed to vary inversely with absolute temperature. This is achieved by using components or circuits with characteristics that change in a complementary manner to PTAT.

2. Bipolar Transistor-Based Approach

- Bipolar transistors can be configured to exhibit a CTAT voltage characteristic. A common method involves using a pair of transistors with similar emitter areas but different collector currents.

3. Resistor Networks

- Resistor networks with different temperature coefficients can be used to generate a CTAT voltage.
- The change in resistance with temperature compensates for the PTAT voltage.

4. Bandgap Voltage References

- Advanced voltage reference circuits, such as the bandgap reference, can generate CTAT voltages.
- Bandgap references combine PTAT and CTAT components to produce a stable voltage across a range of temperatures.

3.4.1 PTAT voltage and current generation

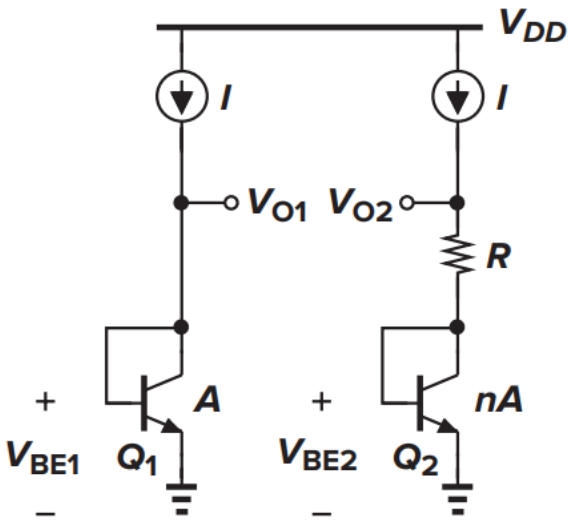

Figure 3.1: (a) Basic BJT based PTAT generator [6]

It was recognized in 1964 that if two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature. For example, as shown in Fig. 3.1, if two identical transistors (I_{S1} = I_{S2}) are biased at collector currents of nI_0 and I_0 and their base currents are negligible, then

$$\begin{aligned} V_{EB1} - V_{EB2} &= V_T \ln\left(\frac{I}{I_{S1}}\right) - V_T \ln\left(\frac{I}{I_{S2}}\right) \\ &= V_T \ln(n) \end{aligned} \tag{3.2}$$

The above two figures show the conventional implementation of the PTAT voltage generator. Where Fig 3.2(a) uses an Operational Transconductance Amplifier (OTA) and current mirrors to generate the

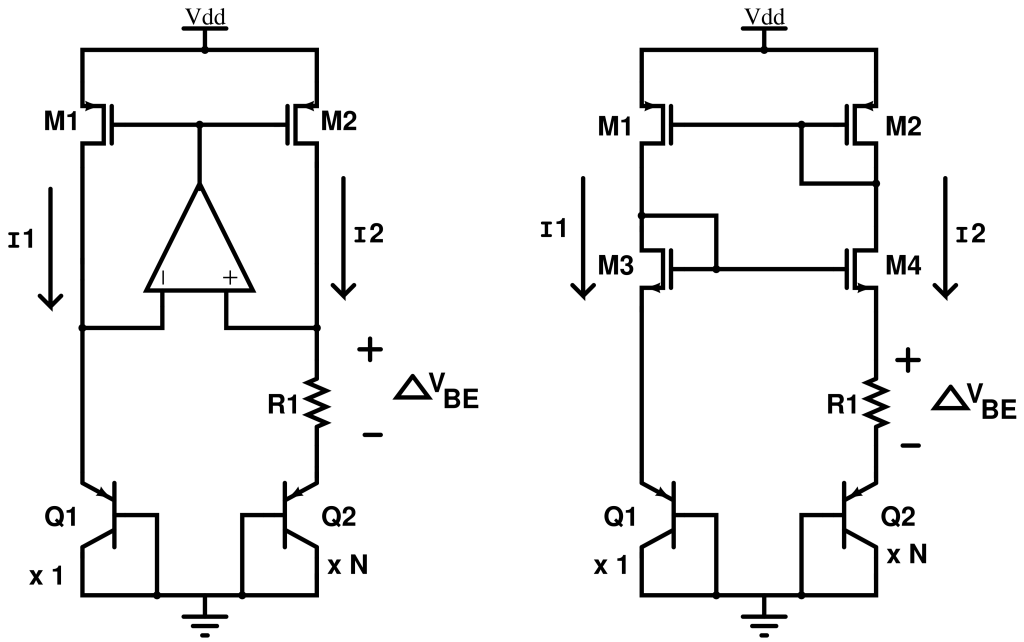

Figure 3.2: (a) Basic BJT-based PTAT generator with OTA and (b) Current mirrors

current bias for the BJTs to generate the PTAT voltage ΔV_{EB}. The slope of the PTAT voltage mainly depends on the ratio N, the multipliers of the BJTs, and the temperature coefficient of the resistance (R_1).

PTAT (Proportional to Absolute Temperature) currents find utility across various applications and can be generated through a topology depicted in Fig. 3.3 (a). An alternative approach involves combining the supply-independent biasing scheme with a bipolar core and OTA, as shown in Fig. 3.3 (b). Assuming the pairs M1-M2 and M3-M4 are identical, and for simplicity, setting $I_{D1} = I_{D2}$, the circuit ensures $V_X = V_Y$. Consequently, $I_{D1} = I_{D2} = (VT \ln n)/R_1$, resulting in the same behavior for I_{D5}. However, practical implementation faces challenges due to transistor mismatches and, notably, temperature coefficient variations in R1. The actual behavior of ID5 may deviate from the ideal equation. For applications with low-voltage operation, the topology depicted in Fig. 3.3 (b) is typically preferred.

Fig. 3.4 shows another approach to generate PTAT voltage. Where the PNP is replaced by NMOS devices. This method is particularly helpful, considering ultra-low power applications. As, here the mosfet will operate in the subthreshold region and currents I_1 and I_2 flowing through M1 and M2, respectively, the expression for V_{PTAT} can be given by

$$V_{PTAT} = V_{GS1} - V_{GS2} = (V_{th1} - V_{th2}) + \eta V_T ln\left(\frac{I_1}{I_{01}}\right) - \eta V_T ln\left(\frac{I_2}{I_{02}}\right) \tag{3.3}$$

where η is the sub-threshold slope factor and $I_0 = \mu_n C_{ox}(W/L)(\eta - 1){V_T}^2$. The threshold voltage of the mosfets M1 and M2 will be cancelled, considering similar mosfets are used, and the body effect of M2 is ignored.

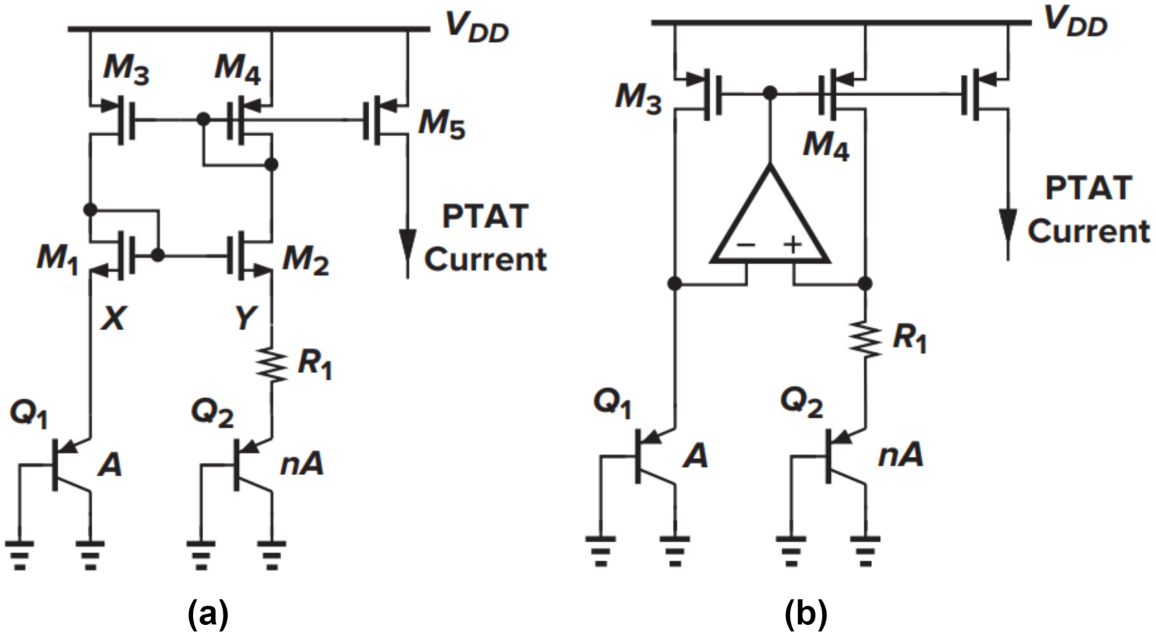

Figure 3.3: (a) PTAT current generation using current mirrors and (b) OTAs

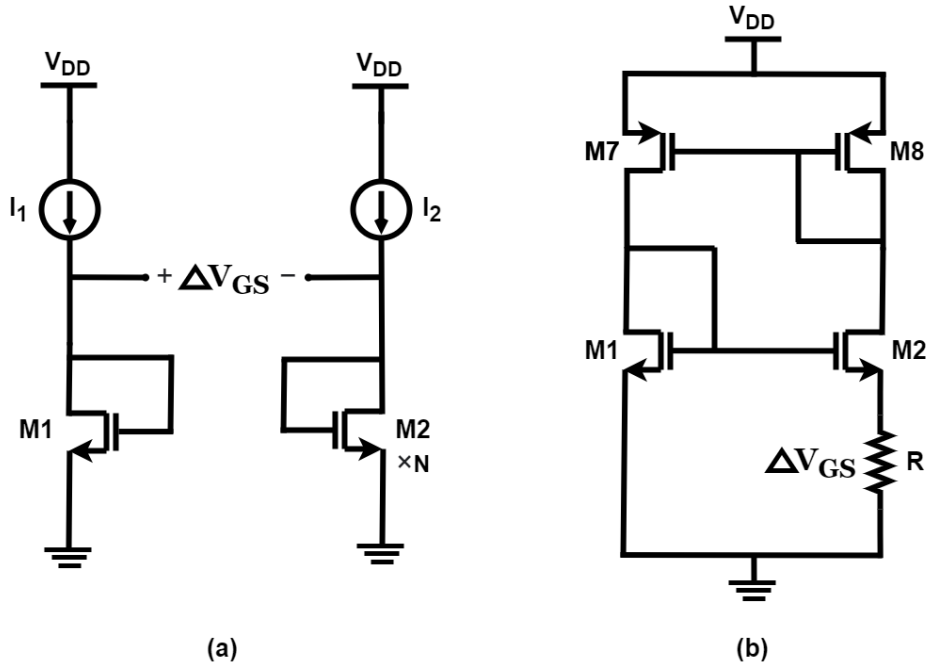

Figure 3.4: (a) Principle of Mosfet-based PTAT voltage generation and (b) Practical implementation

However, as we can see from Fig. 3.4 (b), due to the body effect of M2, the threshold voltage won't be cancelled exactly, and also, the η varies with respect to the process variation. Various techniques are used to deal with these issues, and this approach is widely used in ultra-low power operations. The

threshold voltage can be expressed as follows:

$$V_{TH2} = V_{TH0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right) \tag{3.4}$$

where ϕ_F is the fermi potential and γ is the body factor coefficient.

In the coming chapters, we will use the above-discussed architectures and proposed novel methodologies to improve the specifications in the ultra-low power domain.

3.4.2 CTAT voltage generation

In a manner akin to PTAT generation, CTAT voltages are derived using MOS diodes and PNP illustrated in Fig. 3.5(a) and Fig. 3.5(b), respectively. Instead of calculating the difference between gate-source voltages or two base-emitter, we utilize the voltage V_{GS} or V_{EB}, both of which exhibit CTAT behavior, as elucidated.

$$V_{GS} = V_{th} + \eta V_T ln \left(\frac{I}{\mu_n C_{ox} (\eta - 1) {V_T}^2} \right) \tag{3.5}$$

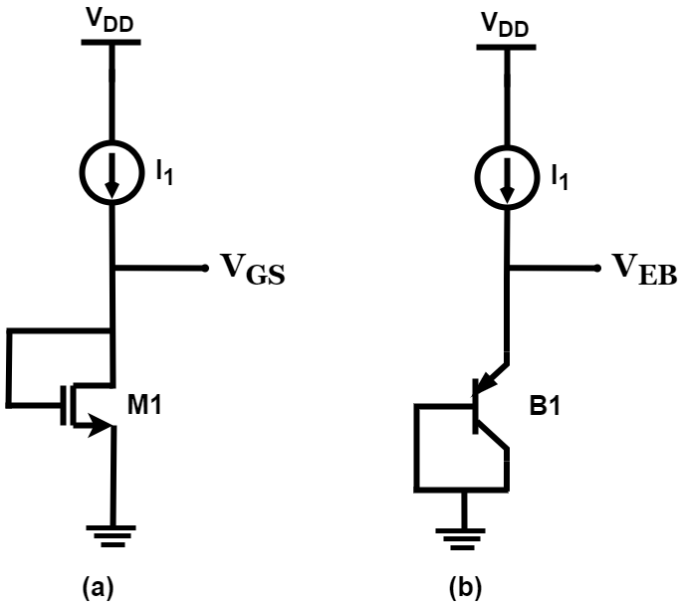

Figure 3.5: Principle of Mosfet and BJT-based CTAT voltage generation

The threshold voltage (V_{th}) exhibits a Complementary to Absolute Temperature (CTAT) behavior, expressed as $V_{th0} - k_1 T$, where V_{th0} is the nominal threshold voltage, and k_1 represents the slope of the threshold voltage. The term μ_n is directly proportional to $T^{(} - 3/2)$, causing the term $\eta V_T ln(I/(\mu_n C_{ox}(\eta - 1){V_T}^2))$ to be proportional to $ln(T^{-1/2})$, assuming I remain constant with temperature. Despite being a weak function of temperature, the predominant CTAT nature of V_{th} extends to V_{GS}. It can be inferred that even a Proportional to Absolute Temperature (PTAT) current cannot alter

the CTAT nature of the term V_{GS}, thereby maintaining its CTAT characteristic. The expression for the derivative of V_{EB} can be articulated as follows.

$$V_{EB} = V_{G0} + \frac{kT}{q} ln \left(\frac{IE}{T^{\gamma}} \right) \tag{3.6}$$

The band gap of silicon extrapolated to absolute zero is denoted as V_{G0}, where E is a constant dependent on fundamental quantities and processing variables but not on temperature. Additionally, Γ is defined as 2.5. When the current (I) remains constant with respect to temperature, the slope of VEB is -2mV/°C. This characteristic signifies that VEB functions as a Complementary to Absolute Temperature (CTAT) voltage.

In general, the slope of CTAT voltage generated using the above methods is higher than the PTAT slope. So, we used amplification of the PTAT voltage, which will cancel the CTAT slope and temperature-compensated reference voltage gets generated.

Chapter 4

A 2.3nW Sub-Bandgap Voltage Reference with Line Sensitivity of 0.0066%/V from -40°C to 150°C for Low-Power IoT Systems

4.1 Introduction

The essence of ultra-low power analog circuit design lies in achieving efficient energy utilization while maintaining the desired performance specifications. One fundamental principle of ultra-low power analog circuit design is the reduction of power supply voltages. By operating at lower supply voltages, the power dissipation can be significantly reduced. Voltage reference circuits play a crucial role in various electronic systems and applications by providing stable and accurate voltage references. These references are essential for ensuring the proper operation and reliability of analog and mixed-signal circuits. While traditional voltage reference circuits have been designed to operate at or above the bandgap voltage, there is a growing demand for ultra-low power, high-temperature range sub-bandgap voltage references.

Ultra-low power, high-temperature range sub-bandgap voltage references are circuits that generate stable and accurate voltage references below the bandgap voltage while operating at extreme temperatures. These circuits find significant applications in harsh environments, such as aerospace, automotive, and industrial applications, where high temperatures and stringent power constraints are common.

The design and implementation of ultra-low power, high-temperature range sub-bandgap voltage reference circuits pose several challenges. First, the circuit must operate reliably and accurately at low supply voltages, ensuring minimal power consumption while providing precise voltage references. Second, it must exhibit excellent temperature stability over a wide range of temperatures, allowing it to function reliably in extreme environments. Third, the circuit should be robust against process variations, noise, and other environmental factors to maintain accuracy and stability under adverse conditions.

This thesis aims to address these challenges and develop novel ultra-low power, high-temperature range sub-bandgap voltage reference circuits that offer improved performance and robustness. The research will focus on exploring different circuit architectures, device selection, and design techniques to achieve accurate, trimming-free and stable voltage references below the bandgap voltage while op-

erating at high temperatures. Special attention will be given to addressing the impact of temperature fluctuations, process variations, and noise on the performance of the proposed circuits.

The advancement and rapid development of the Internet of Things (IoT) have created many applications, such as intelligent wearables, wireless sensors, medical devices, smart home accessories, remote sensing systems, etc. Due to lower form factor targets, these devices are powered by either miniaturized batteries or by energy scavenging units like photovoltaic cells and RF energy harvesting. In both cases, power consumption becomes the bottleneck, and aggressively reducing power consumption is the key to enabling this technology. Duty cycling is a widely adopted technique to reduce average power consumption. However, voltage references being always-on circuits cannot benefit from duty cycling and require novel architectures to scale the power consumption. In addition to low power consumption, these references are desired to operate in a wide temperature range with good accuracy and line sensitivity without using an extensive trimming circuit. As bandgap references are one of the most reliable architectures that shows a lesser process, supply, and temperature dependency, it is constructive to design BJT-based references.

4.2 Literature Survey

Conventional voltage references such as [20, 21, 22, 23] work in μW range; these will have a huge impact on the system lifetime and hinder their use for the targeted low-power applications. Conventional bandgap references use BJT to make the voltage process, temperature, and supply insensitive, are power hungry, and consume in the tens and hundreds of μW range [24, 25, 26]. In Voltage reference, using Silicon-on-Insulator (SOI) has been proposed in [27] for high-temperature applications, but the power consumption is still in the μW range. To mitigate this issue [28, 29, 30, 31, 32] proposes voltage references with nW power consumption. However, high-value resistances have been used, which have a direct trade-off in the silicon area, and [32] operates for a low-temperature range. Also, [33] proposes a voltage reference using sample and hold to get an average power in the nW range using large sampling capacitors and resistance, thus occupying a large area in silicon. Moreover, its operating temperature range is limited to 125°C. To get a further power reduction, [34, 35, 36, 37] propose pW voltage references with a high-temperature range. However, the power consumption increases exponentially with temperature, and [34, 35, 36] report no functionality in negative temperatures. These constraints are mainly due to the dependency on the subthreshold leakage phenomenon. Moreover, they use native oxide devices (NVT MOSFETs), which are not provided by many foundries. [38] proposes a duty cycle-based, ultra-low-power voltage reference reporting high line sensitivity without accounting for the oscillator power consumption. This paper explores an ultra-low-power sub-BGR architecture for an mm-scale remote sensing system, where the system needs to operate for more than 125°C while maintaining low power.

This paper proposes a 2.3nW sub-bandgap voltage reference for high-temperature remote sensing applications, which avoids the usage of high-value resistors, native devices, or complex compensation

techniques that increase power, area, or supply voltage. The proposed sub-BGR exploits the thin oxide device's weak inversion mode gate leakage current properties to generate the reference voltage.

4.3 Proposed Sub-Bandgap Reference

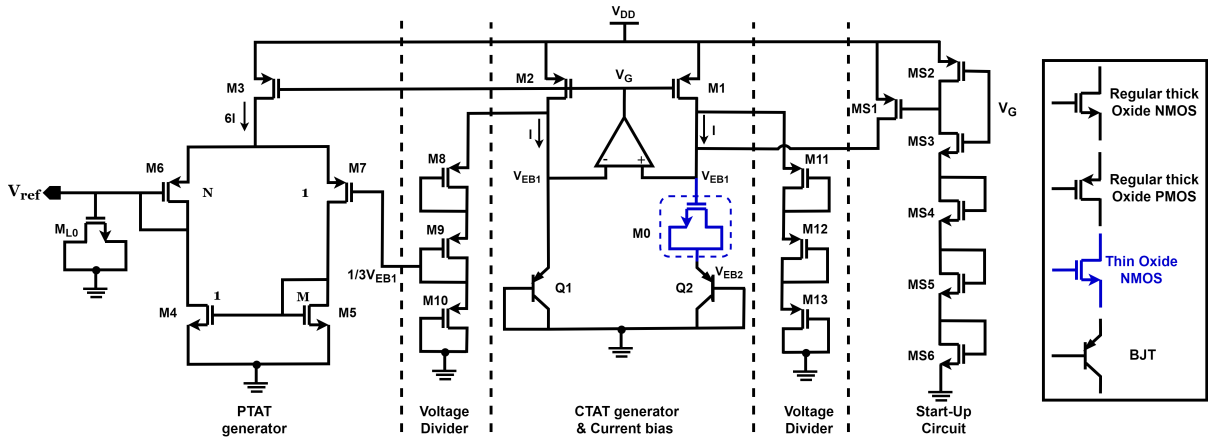

Figure 4.1: Block Diagram of the proposed sub-BGR

The architecture of the proposed sub-BGR is shown in Fig. 4.1. Apart from M0, all other transistors are regular thick oxide NMOS and PMOS devices. M0 is a thin oxide device; tunneling current flows through the transistor's gate due to its extremely low oxide thickness, allowing it to bias the circuit in a low current regime without using large valued resistors. The gate leakage transistor M0 is operated in weak inversion mode, whose I-V characteristics and expressions are discussed in the subsequent section. The circuit primarily consists of a PTAT and CTAT generator compensating accordingly to generate the reference voltage. The CTAT generator is the sub-BGR core which consists of Bipolar Junction Transistor(BJT) Q1 and Q2 and a two-stage NMOS OTA, which is biased by an accumulation mode gate leakage-based PTAT current reference of 137pA as shown in Fig.7(a). The current reference design is implemented to make the OTA functional across all corners in the wide temperature range. The PTAT generator consists of a differential pair and current mirror to generate PTAT voltage. To match the PTAT slope, a voltage divider is used to reduce the slope of the CTAT voltage to generate the reference voltage accordingly. The Voltage divider is symmetrically placed on either side of the sub-BGR core so that the loading effect is the same in both branches of the current mirror. A capacitor (C_{eq}=2.8pF) implemented using a thick oxide device (M_{L0}) is connected at the output to have a better power supply rejection ratio (PSRR) at higher frequencies. A start-up circuit [39] is implemented to avoid any degenerate conditions.

4.3.1 Derivation for weak inversion mode gate-leakage current

As mentioned above, a gate-leakage transistor is used to bias the circuit in a low current regime. As the gate-leakage transistor is operated in a weak inversion region, we have three major current components, the gate-to-source/drain current(I_{gs} and I_{gd}) and gate-to-channel current(I_{gc}). The gate to source current will be of the form [40]:

$$I_{gs} = K * V_{gs} \left(V_{gs} - V_{fbsd}\right) \tag{4.1}$$

Here K comprises the effective dimension of gate-leakage MOSFET and modelling constants, which are constant for a given technology node and is independent of temperature. Here V_{fbsd} is the flat-band voltage between gate and S/D which has an approximate value of 6.67mV as given in [40]. From the symmetry of the gate-leakage MOSFET, the gate-to-source current will be equal to the gate-to-drain and hence $I_{gsd}(= I_{gs} + I_{gd})$ will be twice of gate-to-source current(I_{gs}).

The total gate leakage also consists of the gate-to-channel current (I_{gc}), which is given by [41]:

$$\begin{aligned} I_{gc} = {} & W_{eff} L_{eff} \cdot A \cdot T_{ox\,\text{Ratio}} \cdot V_{gse} \cdot V_{aux} \cdot \exp[-B \cdot TOXE \\ & (AIGC - BIGC.V_{oxdepinv}) \cdot (1 + CIGC \cdot V_{oxdepinv})] \end{aligned} \tag{4.2}$$

$$V_{aux} = NIGC \cdot v_t \cdot \ln\left(1 + \exp\left(\frac{V_{gse} - V_{TH}}{NIGC \cdot v_t}\right)\right) \tag{4.3}$$

$$V_{\text{oxdepinv}} = K_{1ox}\sqrt{\phi_s} + (V_{gs} - V_{th}) \tag{4.4}$$

Here V_{oxdepinv} , V_{aux}, ϕ_s are defined in[41] and parameters A, $T_{ox\,\text{Ratio}}$, B, TOXE, AIGC, BIGC, CIGC, NIGC in Eq.(2) and Eq.(3) are constants for a given technology and are independent of temperature. Since the gate-leakage transistor is operated in weak inversion(V_{gs}-V_{TH} is negative), the exponential term is very small, therefore approximating logarithmic function to the first order as $\log(1+x) \approx x$ we get V_{aux} function as

$$V_{aux} = NIGC \cdot v_t \cdot \exp\left(\frac{\mathrm{V_{gs}} - V_{TH}}{NIGC \cdot v_t}\right) \tag{4.5}$$

Applying further approximation as done in [41], the exponential term in Eq.(2) can be approximated by a linear fit curve given by $f\left(V_{\text{oxdepinv}}\right) = K_2\left(1 + \alpha V_{\text{oxdepinv}}\right)$, where α is a constant whose value is small. The gate-to-channel current can be written as

$$I_{gc} = K_1 * K_2 * V_{gs} \exp\left(\frac{\mathrm{V_{gs}} - V_{TH}}{K'}\right)(1 + \alpha V_{oxdepinv}) \tag{4.6}$$

Where $K' = NIGC.v_t, K_1 = W_{eff} * L_{eff} * A * T_{\text{oxRatio}} * \mathrm{K'}$. Here W_{eff} , L_{eff} are the effective dimensions of the mosfet. The total gate leakage current can be written as

$$\begin{aligned} I_g = {} & K_1 * K_2 * V_{gs} \exp\left(\frac{V_{gs} - V_{TH}}{K'}\right)\left(1 + \alpha V_{\text{oxdepinv}}\right) \\ & + K * V_{gs}\left(V_{gs} - V_{fbsd}\right) \end{aligned} \tag{4.7}$$

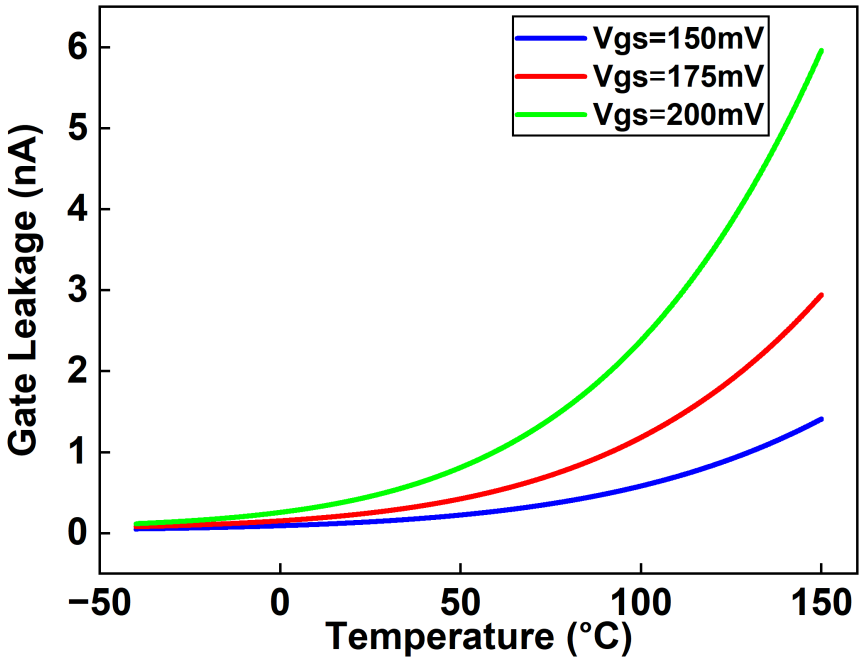

Figure 4.2: Gate Leakage current vs Temperature

From Eq.(7), the temperature coefficient of gate current depends only on Vgs. PTAT voltage across the gate leakage mosfet results in non-linear PTAT current, seen in Fig. 4.2. This non-linear PTAT current improves circuit operation at higher temperatures as threshold voltage reduces. A PTAT current is needed for the PTAT and CTAT generator to function correctly. Gate leakage transistor operation for wide temperature range measured in [42].

4.3.2 Temperature Compensation

From Fig. 4.1 V_{gs} across M0 is equal to V_{EB1} - V_{EB2}. As we know for a BJT V_{EB}=$V_T \ln\left(\frac{I}{I_{S2}}\right)$ Here, Q2 consists of n parallel units of Q1, so $I_{S2} = nI_{S1}$. V_{gs} across M0 is as follows,

$$\begin{aligned} V_{EB1} - V_{EB2} &= V_T \ln\left(\frac{I}{I_{S1}}\right) - V_T \ln\left(\frac{I}{I_{S2}}\right) \\ &= V_T \ln(n) \end{aligned} \tag{4.8}$$

This PTAT voltage across the gate leakage transistor generates the PTAT current shown in Fig. 4.2 and helps bias the PTAT generator at higher temperatures. It also generates the CTAT voltage V_{EB1}, after the voltage divider, which works as an input to the PTAT generator. In conventional sub-BGR circuits, PTAT voltage is generated using BJT and resistors. Moreover, we need high resistance for ultra-low power IoT applications, which takes a large silicon area. This paper incorporates a differential pair and a current mirror-based structure to generate PTAT voltage [43]. As MOSFET operates in the subthreshold region, V_{GG} can be expressed as follows.

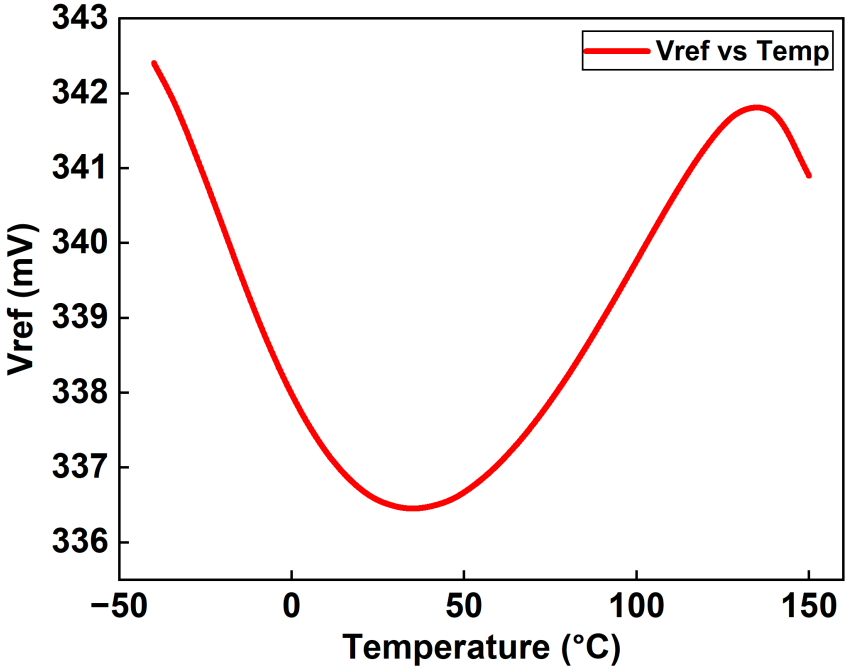

Figure 4.3: V_{ref} vs Temperature

$$\begin{aligned} V_{\mathrm{GG}} &= V_{\mathrm{ref}} - \frac{1}{3}V_{\mathrm{EB1}} = V_{\mathrm{SG},M7} - V_{\mathrm{SG},M6} \\ &= V_{\mathrm{TH}} + \eta V_T \ln\left(\frac{I_{M7}}{K_{M7}I_0}\right) - V_{\mathrm{TH}} - \eta V_T \ln\left(\frac{I_{M6}}{K_{M6}I_0}\right) \\ &= \eta V_T \ln\left(\frac{K_{M5}K_{M6}}{K_{M4}K_{M7}}\right) \end{aligned} \tag{4.9}$$

Where, I_0(=$\mu C_{\mathrm{OX}}(\eta-1)V_T^2$) is a process dependent parameter. K_{M6}, K_{M7}, K_{M4} and K_{M5} are the aspect ratios of the PMOS differential pair and the NMOS current mirrors, respectively.

$$\begin{aligned} V_{\mathrm{ref}} &= V_{\mathrm{GG}} + \frac{1}{3}V_{\mathrm{EB1}} \\ &= \eta V_T \ln\left(\frac{K_{M5}K_{M6}}{K_{M4}K_{M7}}\right) + \frac{1}{3}V_{\mathrm{EB1}} \end{aligned} \tag{4.10}$$

Considering the TC of V_{EB1} to be k_1, the TC of V_{ref} can be given as:

$$\frac{\partial V_{ref}}{\partial T} = \eta\frac{k}{q}\ln\left(\frac{K_{M5}K_{M6}}{K_{M4}K_{M7}}\right) + \frac{1}{3}k_1 \tag{4.11}$$

Therefore, a temperature-compensated voltage can be obtained by appropriately sizing the transistors M4-M7.

4.4 Results and Discussion

The proposed Sub-Bandgap reference is designed and implemented in the 65nm CMOS process. Fig. 4.3 shows the variation of the reference voltage w.r.t temperature; it depicts the temperature coefficient (TC) of the reference is 94ppm/°C. The statistical results for the Sub-Bandgap Reference are presented using Monte-Carlo simulation for both process and mismatch (1000 samples). Fig. 4.4(a)

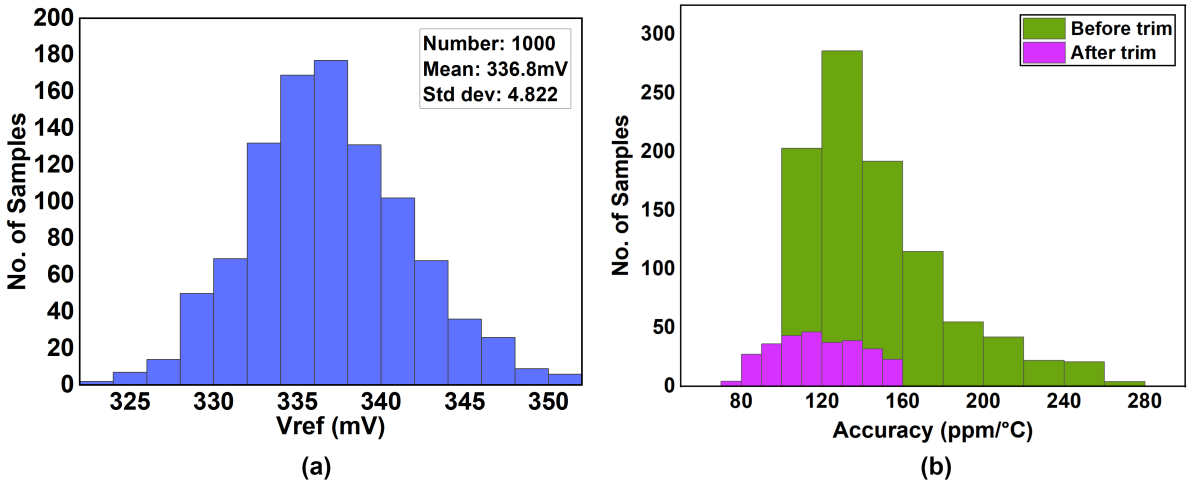

Figure 4.4: (a) MC of V_{ref} (b) MC of Accuracy pre and post trim

shows the V_{ref} variation w.r.t both process and mismatch, and the observed mean and standard deviation are 336.8mV and 4.822mV respectively, which results in $\pm 3\sigma$ variation of 4.295%. Fig. 4.6(a) shows the V_{ref} variation w.r.t temperature (from -40 to 150°) at different process corners. The variation of the absolute value and TC can be adjusted by adding a 1-point trim to the thin oxide gate leakage transistor M0. Here low-leakage and gate-boosted switches like [44, 45, 18] are used. Post-trim results of V_{ref} w.r.t temperature are given in Fig. 4.6(b), showing the effectiveness of trimming in a wide temperature range and different process corners. Fig. 4.4(b) shows the pre and post-trim results of accuracy; the pre-trim result shows the mean and standard deviation of 153ppm/°C and 49.01ppm/°C respectively, and 1-point trim gives an improved mean and standard deviation of 117.7819ppm/°C and 21.35ppm/°C respectively. This shows that the proposed circuit can be used even without trimming, with minimal compromise in accuracy. The PSRR at DC for the sub-Bandgap at 0.7V,1V, and 3V are -57.17dB, -89.39dB and -115.2dB, respectively, as shown in Fig. 4.5(a). The power supply rejection ratio at higher frequency can be increased by increasing the sizing of the gate-leakage-based capacitor at the expense of increased area. In the supply range of 0.7V-4V, the line sensitivity at SS, TT, and FF corners are observed to be 0.006623%/V, 0.0066%/V and 0.00844%/V, respectively, as shown in Fig. 4.5(b). As the current is not exponential in nature, the power consumption only varies by 30x times in the temperature range of -40°C to 150°C at different supply voltages (Fig. 4.7(a)) and varies by a factor of 1.025x over the supply range of 0.7V-4V (Fig. 4.7(b). The observed settling time for 99% of the steady state value

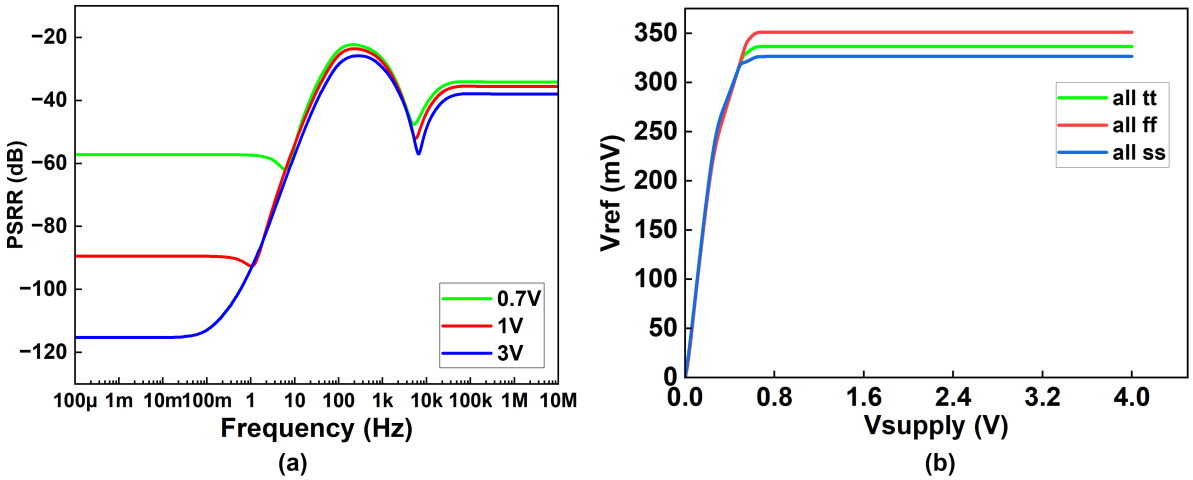

Figure 4.5: (a) PSRR of V_{ref} (b) Line Sensitivity of V_{ref}

is 21.89ms with the startup circuit, as seen in Fig. 4.8(b). The PTAT current shown in Fig. 4.8(a) helps to bias the circuit at higher temperatures. The layout of the proposed Sub-Bandgap reference takes an active area of 0.0851 mm^2 as illustrated in Fig. 4.9. Finally, Table 1 compares the performance of the proposed sub-bandgap reference with other state-of-the-art voltage references.

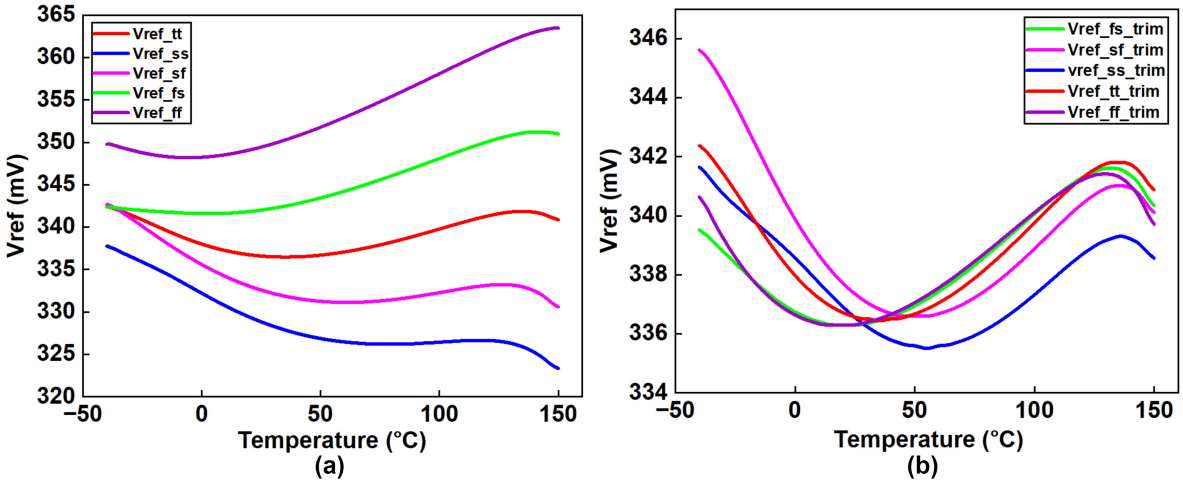

Figure 4.6: (a) V_{ref} at different corners w/o trimming (b) V_{ref} at different corners with trimming

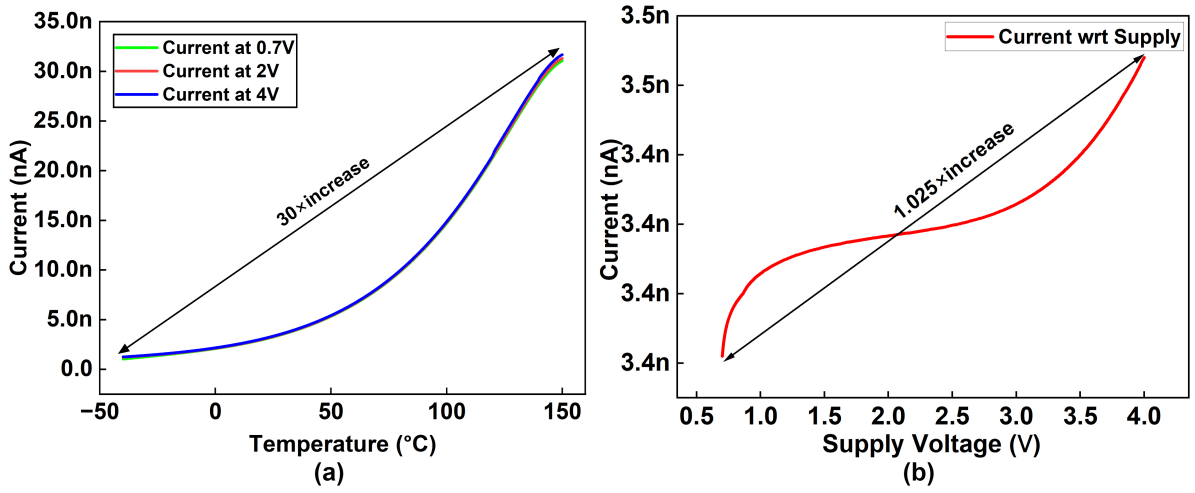

Figure 4.7: (a) Current vs temp at different supply (b) Current vs supply

Table 4.1: Comparison with State-of-the-Art Architectures

Specifications	**This Work**	[39]	[43]	[31]	[46]	[34]	[37]	[32]	[47]	[38]
Technology	**65nm**	180nm	180nm	180nm	65nm	180nm	180nm	180nm	180nm	65nm
Type	**Sub-BGR**	Sub-BGR	Sub-BGR	Sub-BGR	Sub-BGR	Vref	Vref	Sub-BGR	CMOS Vref	CMOS Vref
Vref (mV)	**336**	411.86	548	477	495	0.74(V)	1.048(V)	260	210	134
Temperature Range (^oC)	**-40 to 150**	-40 to 125	-40 to 120	-20 to 120	-40 to 120	0 to 170	-55 to 150	-50 to 85	-40 to 140	-40 to 125
TC (ppm/^oC)	**94**	33.7	114	51.2	42	27	45	95	82	18.1
Power Consumption	**2.3nW**	85nW	52.5nW	37nW	36nW	31.4pW	650pW	0.98nW	9.6nW	0.33nW
Power w.r.t temperature	**30x**	∼1.187x	NA	1.017x	—	23584x	16160x	NA	∼100x	2.16x
Start-up circuit	**Used**	Used	Used	Used	Used	Not used	Used	Not Used	Not Used	Not Used
Settling-time (ms)	**21.89**	NA	6	NA	5	1040	4.7	NA	NA	NA
Variation Coefficient $\sigma/\mu(\%)$	**1.435**	0.39	1.05	0.89	1.027	None	0.187	1.4192	0.31	3
Supply Range	**0.7V-4V**	0.9V-1.8V	0.7V-1.8V	0.8V-1.6V	0.5V-1V	0.9V-3.3V	1.5V-2.5V	0.65V-1.8V	0.4V-1.8V	0.9V-1.6V
Line sensitivity (%/V)	**0.0066**	0.06	6.47	0.0451	0.64	0.27	0.016	0.023	0.027	1.29
PSRR	**-89dB @ DC**	-61dB @10	-56dB @100	-58dB@50	-50dB@DC	NA	-71.8dB@100	—	-59dB@10	—
Area (mm^2)	**0.0851**	0.11	0.0246	0.034	0.0532	0.0076	0.0072	0.075	0.021	0.0046

4.5 Summary

This paper presents a novel high-temperature range Sub-bandgap reference that uses a single-stage PTAT voltage source, generated using asymmetric differential pair, compensated with scaled CTAT voltage obtained from the base-emitter voltage of the BJT to generate the reference voltage. The circuit consumes 2.3nW power and operates for the minimum supply voltage of 0.7V, with state-of-the-art line sensitivity of 0.0066%/V without using a native oxide transistor. The reduced power consumption range over temperature and supply, and other competitive specifications make it suitable for low-power and wide-temperature range applications.

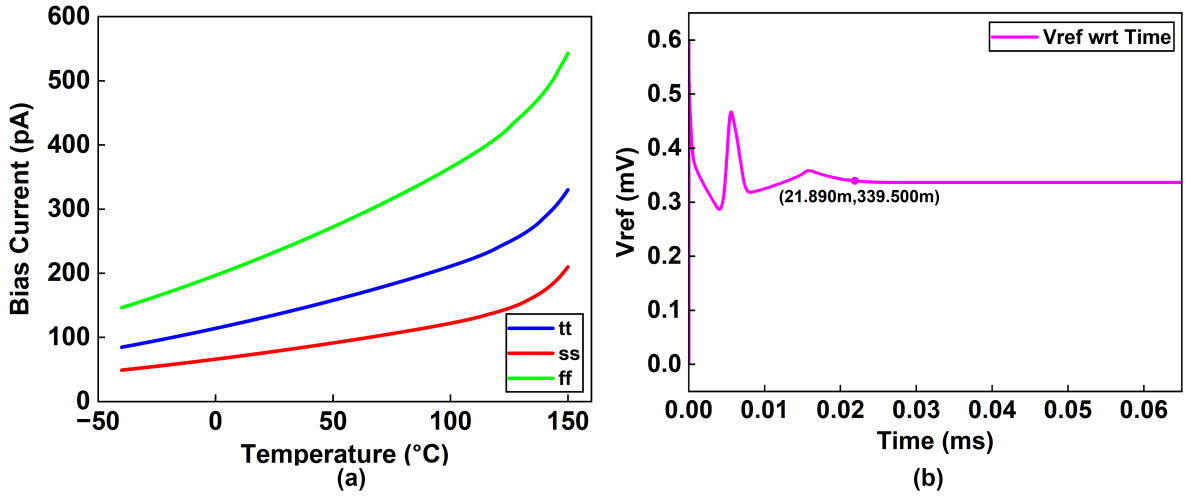

Figure 4.8: (a) Current Bias (b) Start-up time of V_{ref}

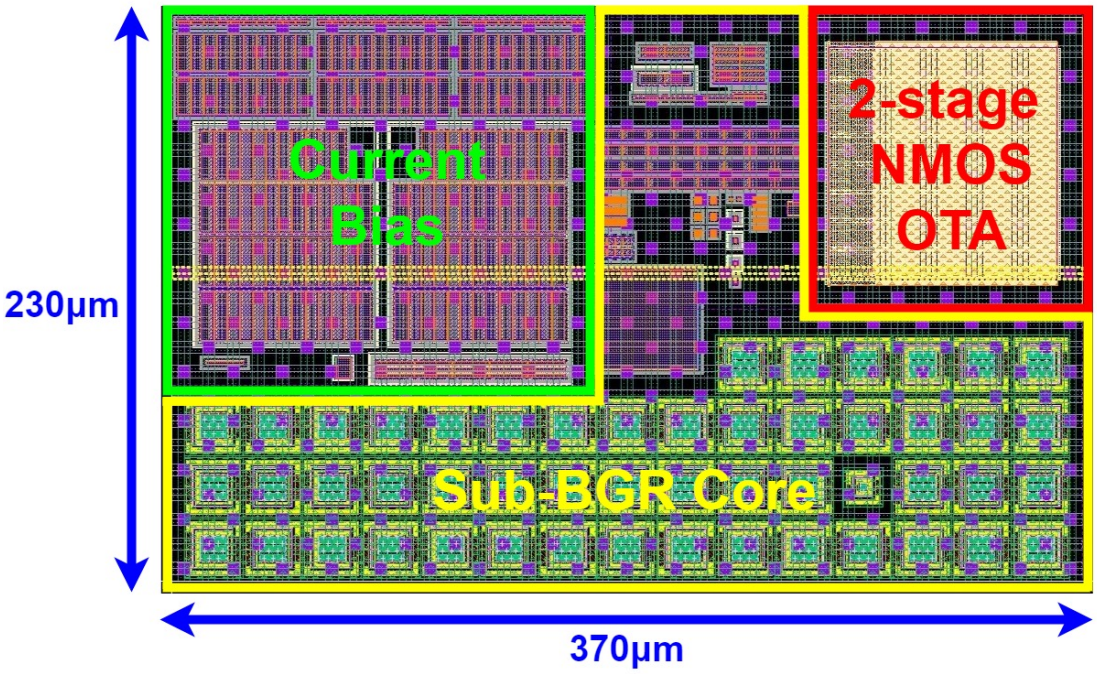

Figure 4.9: Layout of Proposed sub-BGR

Chapter 5

Ultra-low power Process Independent Voltage/Current Reference without using Resistors and Amplifiers

5.1 Introduction

In recent years, remarkable strides have been taken in advancing low-power designs, particularly crucial for battery-operated devices such as wearables and IoT devices, where managing power consumption is of paramount importance. Voltage and current references, pivotal components in any IoT system, must adapt their power scaling to meet evolving requirements. Furthermore, it is imperative for these references to function efficiently across a broad temperature range, ensuring accuracy and line sensitivity, all without the need for external trimming circuits. The incorporation of trim-free designs not only obviates the necessity for external calibration but also lowers manufacturing costs and enhances circuit reliability. Additionally, the integration of both voltage and current reference circuitry into a unified block proves advantageous.

5.2 Literature Survey

The voltage reference plays a pivotal role in the construction of analog, digital, and mixed-signal circuit systems. To ensure the proper functioning of operational amplifiers, comparators, and AD/DA converters, a stable reference voltage is indispensable. Traditional voltage references, realized using Bipolar Junction Transistors (BJTs), are commonly known as bandgap references (BGR) [48, 49]. While BGRs offer resilience to process, supply, and temperature (PVT) variations, they operate in the μW power range and demand high supply voltages.

In recent times, there has been considerable interest in CMOS subthreshold voltage references due to their operation at low supply voltages and minimal power consumption [50, 51, 52, 53]. A sub-μW voltage reference utilizing MOSFETs and resistors is proposed in [50]. However, the use of high resistance values to lower power consumption presents a direct trade-off with silicon area. Another

approach is presented in [51], introducing a resistor-less voltage reference with nW power consumption. Nonetheless, this design requires external trimming circuitry to address process variations.

In [52], a CMOS-based voltage reference is introduced with power consumption in the nW range, achieved without the use of resistors and trimming circuits. However, the design exhibits a notable process variation (σ/μ) of 7%. Seeking further power reduction, [53] proposes a pW voltage reference. Unfortunately, this design reports non-functionality at negative temperatures due to the exponential dependency of subthreshold leakage on temperature. Additionally, it relies on native oxide devices (NVT MOSFETs), which are not universally provided by many foundries [54].

The conventional method for generating current references involves variations of the beta multiplier, employing the V/R principle with operational amplifiers to effectively compensate for temperature coefficients of both resistance and voltage [55, 56]. However, resistance-based designs demand a considerably larger area to scale power consumption in the pW and nW regime. To address this challenge, [57] replaces the resistor in the beta-multiplier with a MOSFET in deep triode, achieving nW power consumption but at the expense of high process variation and a large voltage supply (Minimum supply $= 1.3V$). In [58], a current reference with lower supply and nW power consumption is proposed. However, the design exhibits a process variation (σ/μ) exceeding 10%. [59] enhances the process variation of the current reference with a process tracking circuit, but its power consumption, line sensitivity, and temperature range render it unsuitable for low-power IoT applications. Design [60] introduces a trim-free nW current reference with a low process variation of 8.8% (6σ). Nevertheless, the architecture operates from a minimum supply of 1.5V. [61, 62] proposes pico-watt current references using tunneling currents. While these references require less area, the susceptibility of tunneling currents to tox variations [63] (exceeding 600% across process corners) necessitates extensive trimming, thereby increasing costs.

Citations [64, 65, 66] delve into the integration of voltage and current references within a unified block. [64] advocates for a nanowatt (nW) voltage/current reference employing resistors and amplifiers, introducing additional design complexities such as offset and power consumption. On the other hand, [65] eliminates the need for an amplifier but necessitates a trimming circuit to mitigate process variations. Meanwhile, [66] achieves power consumption in the picowatt (pW) range but relies on native oxide devices and trimming circuits.

This paper introduces a novel approach, presenting a 37nW, trim-free voltage/current reference designed to operate efficiently across a wide temperature range from -40^{o}C to 100^{o}C, all achieved without the use of resistors, amplifiers, or native oxide devices. The subsequent sections of this paper are organized as follows: Section II outlines the proposed voltage/current reference, Section III provides the simulated results, and Section IV draws conclusions.

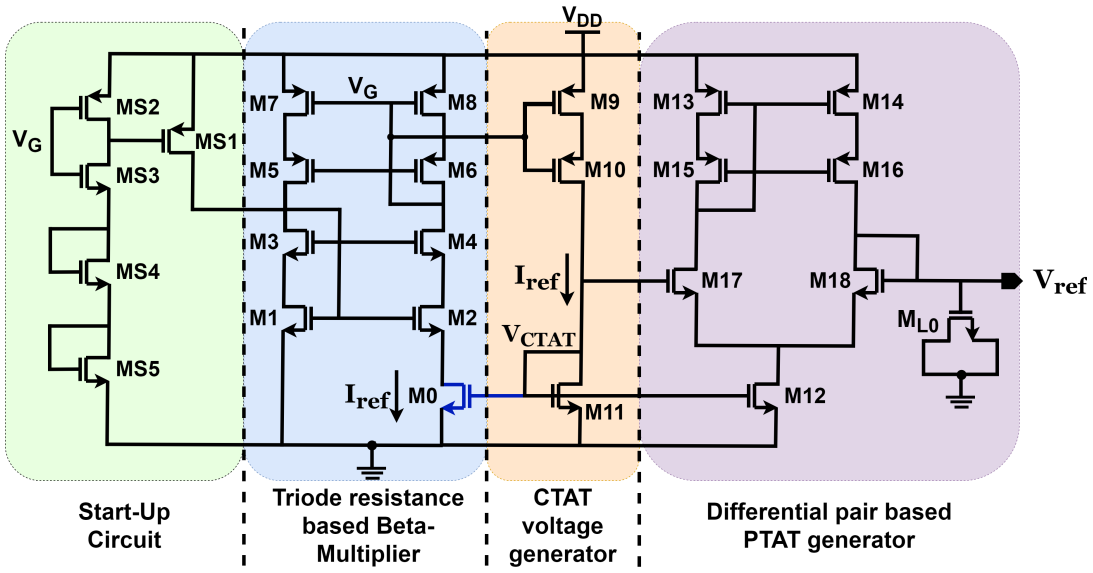

Figure 5.1: Proposed voltage/current reference

5.3 Proposed Voltage/Current reference

The architecture of the proposed circuit is shown in Fig. 5.1. All the MOSFETs except M0 are in the subthreshold saturation region. The MOS resistor M0 is operated in a strong inversion, deep-triode region. The design consists of a triode resistance-based Beta-multiplier, a CTAT generator, and a PTAT generator. A combination of triode resistance-based Beta-multiplier and CTAT generator results in a current reference[67] whereas the PTAT and CTAT generator compensates for any variation of the generated voltage reference. Moreover, the generated reference current (I_{ref}) is used to bias the PTAT generator. A capacitor (C_{eq}=2.17pF) implemented using a thick oxide device (M_{L0}) is connected at the output terminal to have a better power supply rejection ratio (PSRR) at higher frequencies. A start-up circuit [68] is added to avoid any degenerative conditions.

5.3.1 Temperature compensation of voltage/current reference

In the circuit, the current I_{ref} is generated by MOS resistor M0 with gate-source voltage $V_{GS,M0}$ and drain-source voltage $V_{DS,M0}$. When MOSFET M0 operates in strong inversion and deep triode region (V_{GS} - $V_{TH} > V_{DS}$) , the current through M0 is given by

$$I_{ref} = K_n \left(\frac{W}{L}\right) (V_{GS,M0} - V_{TH}) V_{DS,M0} \tag{5.1}$$

Where, K_n= $\mu_n C_{ox}$, $\frac{W}{L}$ is the aspect ratio of the MOSFET M0 and $V_{DS,M0}$ = $V_{GS,M1}$ - $V_{GS,M2}$. To analyze the temperature behavior of reference current (I_{ref}) , differentiating Eq.1 with respect to

temperature (T) we get

$$\frac{\partial I_{ref}}{\partial T} = K_n \left(\frac{W}{L}\right) V_{DS} \left(\frac{\partial V_{GS}}{\partial T} - \frac{\partial V_{TH}}{\partial T}\right) + K_n \left(\frac{W}{L}\right) (V_{GS} - V_{TH}) \left(\frac{\partial V_{DS}}{\partial T}\right) + \frac{\partial K_n}{\partial T}(V_{GS} - V_{TH})V_{DS} \quad (5.2)$$

Therefore, the circuit is designed in such a way that the CTAT term K_n gets compensated by the PTAT terms $V_{DS,M0}$(=$\eta V_T \ln n$) and (V_{GS} - V_{TH}) as shown in Fig. 5.2 to obtain the temperature-compensated reference current (I_{ref}).

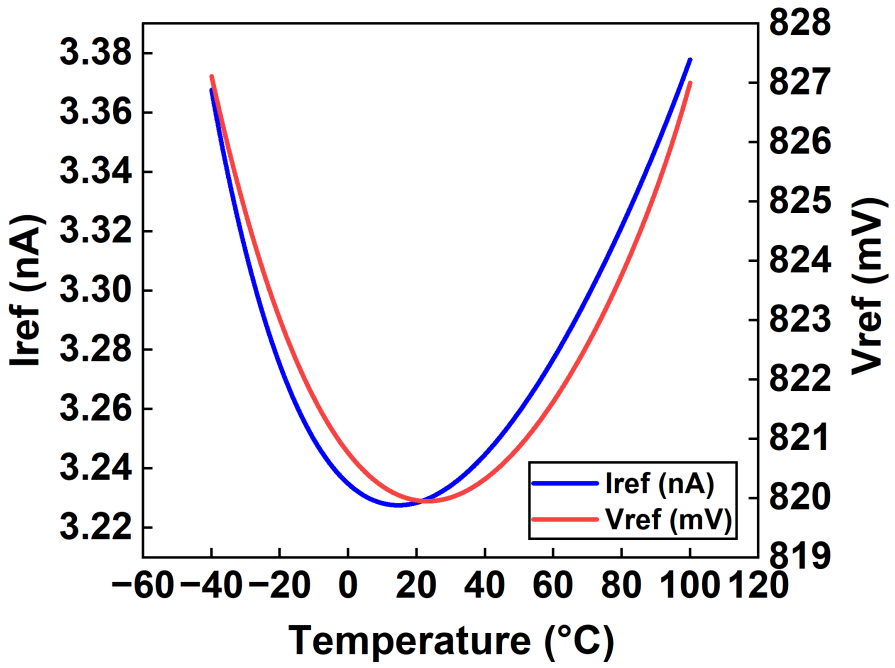

Figure 5.2: V_{ref} & I_{ref} vs Temperature

The PTAT generator along with a CTAT generator and a current reference is required to obtain a temperature-compensated voltage reference (V_{ref}). The CTAT generator is applied as an input to the PTAT generator and biased with the reference current (I_{ref}). Since the MOSFET operates in the subthreshold region, V_{GG} can be expressed as follows:

$$\begin{aligned} V_{GG} &= V_{ref} - V_{CTAT} = V_{GS,M18} - V_{GS,M17} \\ &= V_{TH} + \eta V_T \ln\left(\frac{I_{M18}}{K_{M18} I_0}\right) - V_{\mathrm{TH}} - \eta V_T \ln\left(\frac{I_{M17}}{K_{M17} I_0}\right) \\ &= \eta V_T \ln\left(\frac{K_{M14} K_{M17}}{K_{M13} K_{M18}}\right) \end{aligned} \quad (5.3)$$

Where, I_0= $\mu C_{OX}(\eta - 1)V_T^2$ is a process dependent parameter. K_{M17}, K_{M18}, K_{M13} and K_{M14} are the aspect ratios of the NMOS differential pair and the PMOS current mirrors respectively.

$$
\begin{aligned}
V_{ref} &= V_{GG} + V_{CTAT} \\
&= \eta V_T \ln\left(\frac{K_{M14}K_{M17}}{K_{M13}K_{M18}}\right) + V_{th} + \eta V_T \ln\left(\frac{I_{ref}}{I_0}\right) \\
&= V_{th} + \eta V_T \ln\left(\frac{K_{M14}K_{M17}I_{ref}}{K_{M13}K_{M18}I_0}\right)
\end{aligned}
\tag{5.4}
$$

Considering the temperature coefficient, V_{ref} can be given as:

$$
\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{th}}{\partial T} + \eta\frac{k}{q}\ln\left(\frac{K_{M14}K_{M17}I_{ref}}{K_{M13}K_{M18}I_0}\right) \tag{5.5}
$$

A temperature-compensated voltage can be obtained by appropriately sizing the transistors M13, M14, M17 & M18.

5.3.2 Process variation of voltage/current reference

To study the effect of process variation on the voltage/current reference, one needs to check the process variant terms present in the equations of V_{ref} and I_{ref}. Eq.1 shows that threshold voltage is mainly responsible for process variation, where $V_{GS,M0}$ = V_{TH} + $\eta V_T \ln(I_{ref}/I_0)$. After substituting the value of $V_{GS,M0}$ in Eq.1:

$$
\begin{aligned}
I_{ref} &= \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{TH} + \eta V_T \ln\left(\frac{I_{ref}}{I_0}\right) - V_{TH})V_{DS,M0} \\
&= \mu_n C_{ox}\left(\frac{W}{L}\right)\eta V_T \ln\left(\frac{I_{ref}}{I_0}\right)V_{DS,M0}
\end{aligned}
\tag{5.6}
$$

Here, V_{TH} cancellation takes place, which ultimately improves the process variation of the reference current. The value of V_{GS} - V_{TH} as shown in Fig. 5.3 at different process corners has minimal variation, demonstrating the reference current is less susceptible to process.

From Eq.4, it can be observed that the expression of V_{ref} has three process variant terms V_{TH}, η, and I_{ref}. V_{TH} contributes the most and I_{ref} contributes the least amongst these. The input to the PTAT generator i.e. V_{CTAT} voltage is generated by passing I_{ref} into a diode-connected MOSFET. In any process corner, if the V_{TH} increases, the corresponding current decreases, and as I_{ref} decreases the drain to source voltage V_{DS} (=$\eta V_T \ln(n)$) across the triode MOSFET M0 also decreases meaning that, η decreases for both PTAT terms. η is the subthreshold slope factor which depends on the gate oxide and depletion layer capacitances [69]. So, the process variation of V_{TH} is inversely related to the process variation of η and I_{ref}. The small process variation of I_{ref} along with the multiplication constant $(K_{M14}K_{M17}/K_{M13}K_{M18})$ that amplifies the process variation of η, mitigates the V_{TH} variation to a great extent, resulting in smaller process variation of the reference voltage (V_{ref}).

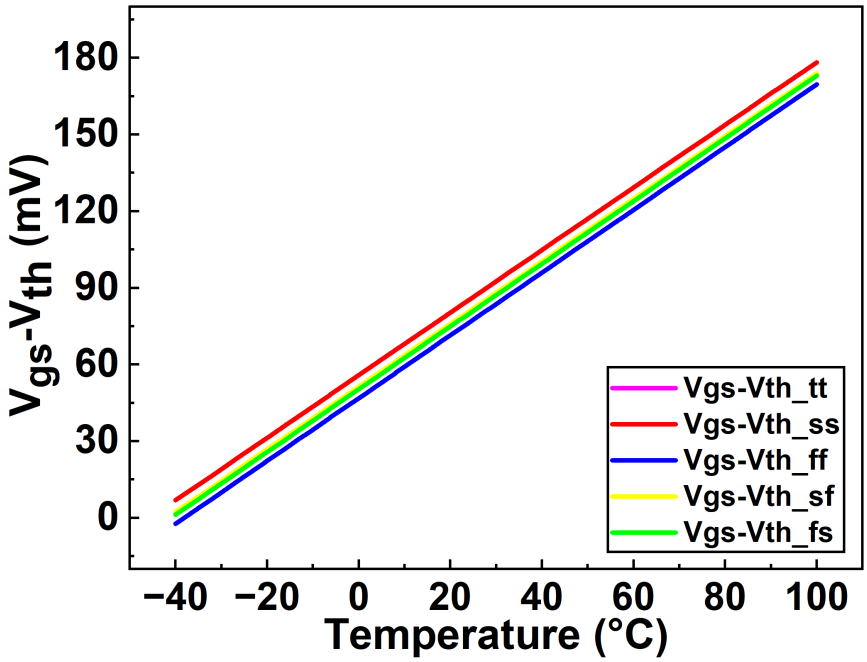

Figure 5.3: V_{gs} - V_{th} vs temperature across corners

5.4 Results and Discussion

The proposed voltage/current reference has been designed and implemented using a 90nm CMOS process. In Fig. 5.5(a), the Power Supply Rejection Ratio (PSRR) at DC for the voltage reference is illustrated at 1V, 1.8V, and 3V, yielding values of -48dB, -52dB, and -51dB, respectively. Moving to Fig. 5.2, the plots display temperature-compensated voltage and current reference characteristics, showcasing temperature coefficients (TC) of 62ppm/°C and 332pm/°C for the temperature range of -40 to 100°C. The nominal values for the current and voltage reference are 3.23nA and 820mV, respectively.

Fig. 5.5(b) shows the supply sensitivities of voltage and current references as 0.296%/V and 0.414%/V, respectively, for the supply range of 1 to 3.5V. As this architecture contains a self-biased loop, to avoid any degenerative conditions, a start-up circuit is added. Fig. 5.8 shows the 99% settling times for the voltage and current reference to be 11.73ms and 11.84ms, respectively. The statistical results for voltage and current reference are presented in Fig. 5.4. Using Monte Carlo simulation with 1000 samples, the observed mean and standard deviation from Fig. 5.4(a) for the voltage reference are 820mV and 10.99mV respectively, which results in process variation (σ/μ) of 1.34%. Fig. 5.4(b) illustrates the Monte Carlo results for the current reference. The mean and standard deviation are 3.23nA and 56.52pA, respectively, resulting in process variation (σ/μ) of 1.75%. Fig. 5.6(a) shows the Monte Carlo results for V_{ref} over the temperature range of -40 to 100°C, from which 3σ variation of $\pm 4.02\%$ can be observed. Similarly, from Fig. 5.6(b) $\pm 3\sigma$ variation of $\pm 5.25\%$ can be observed for the I_{ref} w.r.t temperature. Fig. 5.7(a) shows the Monte Carlo results (1000 points) for the TC of V_{ref}. The ob-

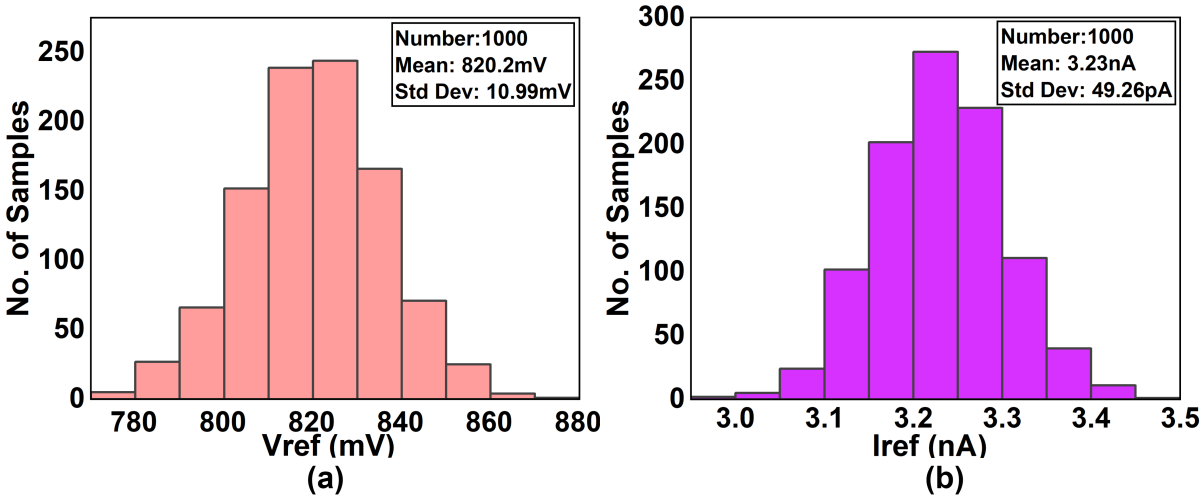

Figure 5.4: Monte Carlo results for (a) V_{ref} (b) I_{ref}

value at 27°C

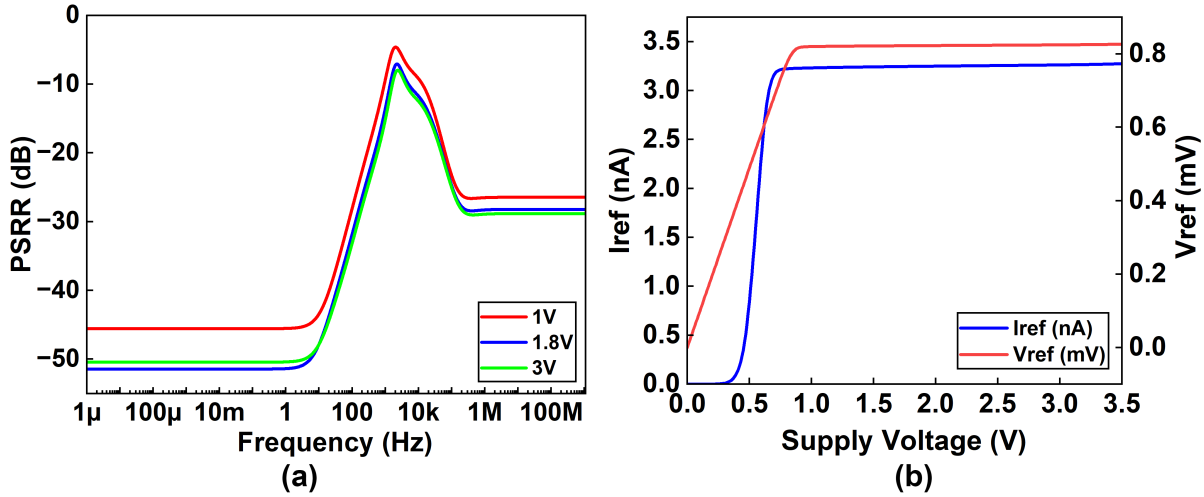

Figure 5.5: (a) PSRR (b) Supply sensitivity

of V_{ref} & I_{ref}

served mean and the standard deviation are 64.55ppm/°C and 2.564ppm/°C, respectively. Similarly, Fig. 5.7(b) shows the Monte Carlo results (1000 points) for the TC of I_{ref}, which comes out to have a mean of 337.17ppm/°C and a standard deviation of 15.16ppm/°C. These results prove that we can avoid trimming in this architecture, considering the achieved nominal values and accuracies for both voltage and current reference. The layout of the proposed voltage/current reference takes an area of 0.0112mm^2, as illustrated in Fig. 5.9.

Table 1 summarizes the performance of the proposed voltage/current reference circuit and compares its performance with the state-of-the-art designs. The designs [64, 65, 66] present both voltage/current references in a single circuit. The usage of resistors in the design[64] increases its area to 0.055mm^2.

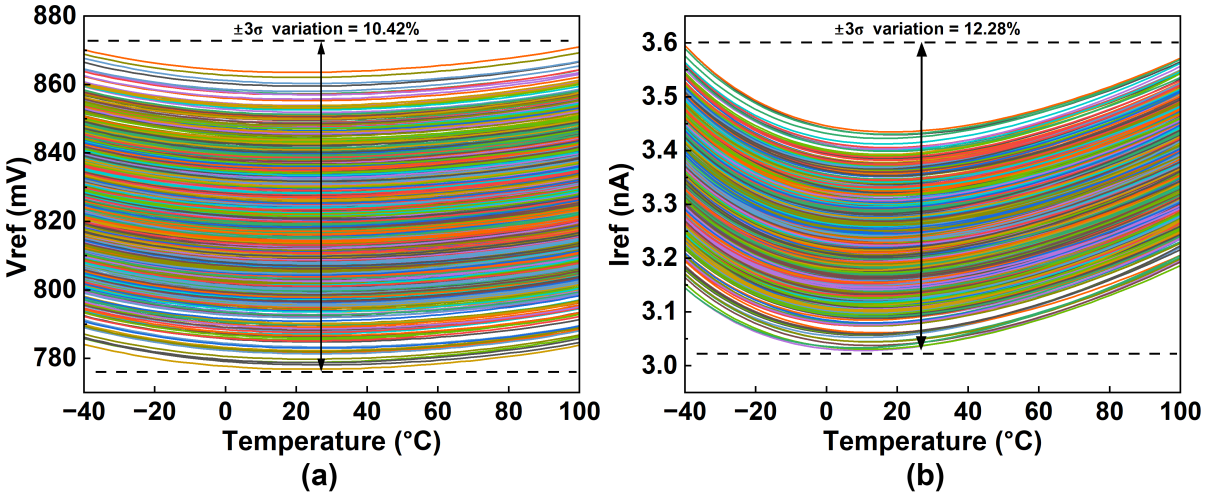

Figure 5.6: $\pm 3\sigma$ variation of (a) V_{ref} (b) I_{ref}

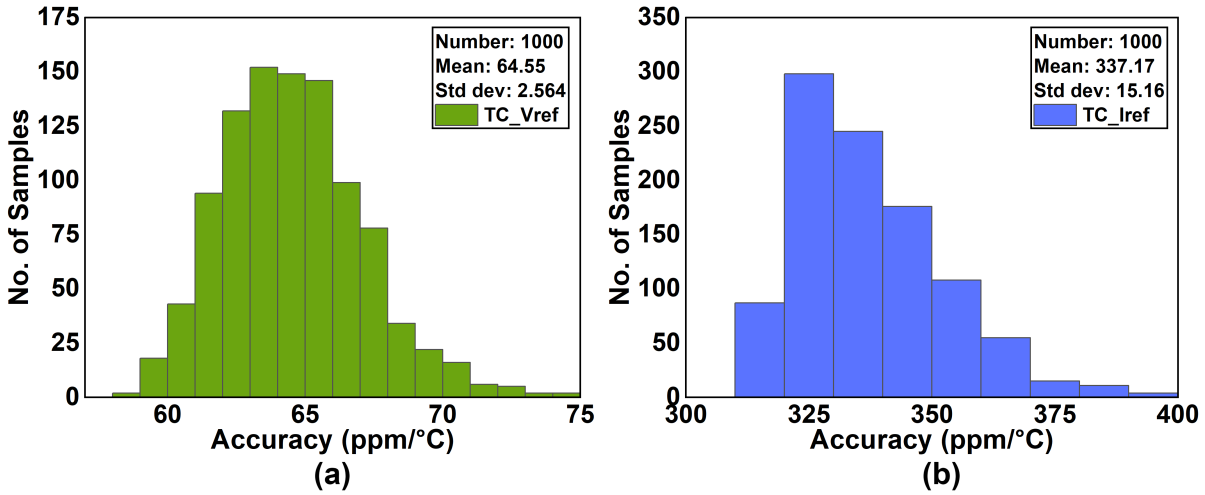

Figure 5.7: Monte Carlo results for TC of (a) V_{ref} (b) I_{ref}

The design [65] works for a minimum supply of 2V. Design [66] uses thin oxide devices to reduce its power consumption but usage of such devices has increased their process variations (σ/μ) to 4.2%/2%. When compared to the voltage reference designs [51] and [52], design [51] works for a high supply voltage $> 1.3V$, and design [52] consumes power greater than 350nW. Current reference designs [57] and [58] listed in Table 1 work for a supply voltage greater than $1V$, but design [57] exhibits a high-temperature coefficient of 1190ppm/^{o}C and substantial process variations. Furthermore, all these designs necessitate additional complex trimming circuitry, increasing the overall design area. Although the design [58] doesn't require trimming, it takes a huge power of 126.56μW and doesn't work for negative temperatures. The presented design in this paper eliminates the need for external trimming circuitry while maintaining other specifications, with process variations (σ/μ) of 1.34%/1.75% that are

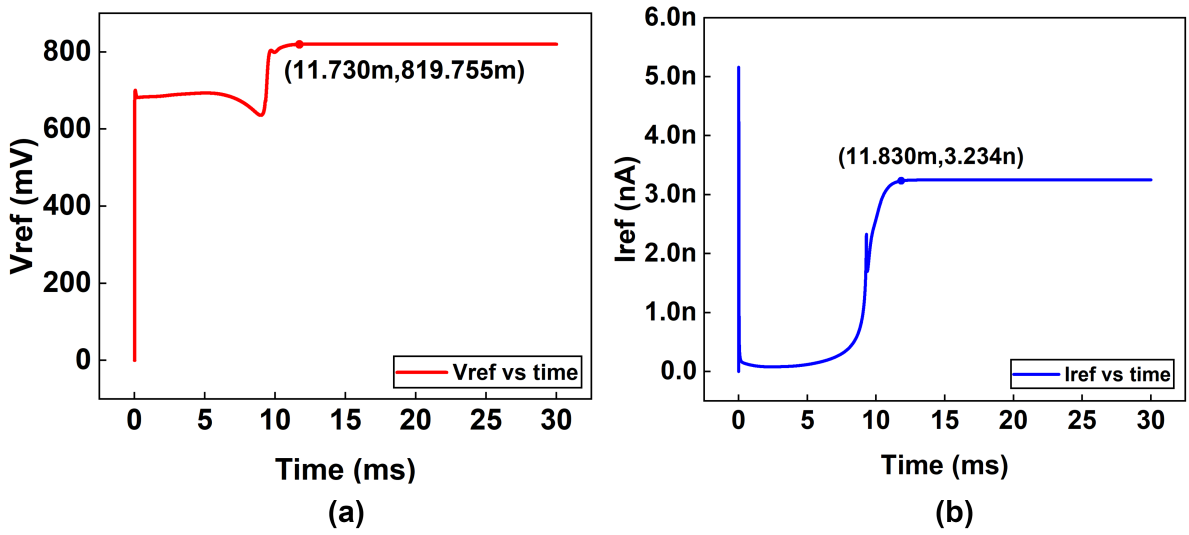

Figure 5.8: Start-up time of (a) V_{ref} and (b) I_{ref}

comparable to post-trim results of state-of-the-art designs. To the best of the author's knowledge, this paper presents a first and novel all-in-one trim-free, all-MOSFET V_{ref}/I_{ref} architecture.

5.5 conclusion

This paper presents a novel trim-free, low process variation, ultra-low power all CMOS voltage/current reference without using high-valued resistances, BJTs, or NVT devices. As it does not incorporate subthreshold leakage behavior, it works over a wide temperature range of -40 to 100°C. The circuit consumes 37nW and works from a minimum supply of 1V over the wide supply range of 1V - 3.5V. The proposed architecture is trim-free, as the variations of the temperature coefficients and the nominal values of both the voltage and current references are insignificant. All the above competitive specifications make it a desirable choice for various ultra-low power wearables and IoT applications.

Table 5.1: Performance summary and comparison with the state-of-arts

	This work	**[64]**	**[65]**	**[66]**	**[52]**	**[51]**	**[59]**	**[57]**
Technology(nm)	**90**	180	180	90	350	180	65	350
Type	**Vref/Iref**	Vref/Iref	Vref/Iref	Vref/Iref	Vref	Vref	Iref	Iref
V_{DD} (Supply range)	**1V-3.5V**	0.7V-2V	2-5V	1V-3V	1.4V-3V	0.8-2.2	1.2V-1.5V	1.3V-3V
Power(nW)	**37**	28	192	0.156	300	360	126560	88.53
V_{ref}(V)/I_{ref}(nA)	**0.820/3.23**	0.368/9.97	1.2/51	0.534/0.043	0.745/-	0.489/-	-/8800	-/9.95
$\sigma/\mu(\%)$	**1.34/1.75**	0.35/1.6	0.17/1.15	4.2/2	7/-	0.5/-	-/1.4	-/14.1
Trimming used	**No**	Yes	Yes	Yes	No	Yes	No	No
Temperature Range(°C)	**-40 - 100**	-40 - 125	-45 - 125	-55 - 100	-20 - 80	-30 - 110	0 - 100	-20 - 80
TC (ppm/°C)	**62/332**	43.1/149.8	32.7/89	22/58	7/-	6.5/-	-/276.8	-/1190
Line Sensitivity (%/V)	**0.296/0.414**	0.027/0.6	0.058/1.76	0.029/0.059	0.002/-	0.076/-	-/4.5	-/0.046
PSRR (db@DC)	**-48**	-59	-46	-77	-45	-75	-	-
Area (mm^2)	**0.0112**	0.055	0.063	0.00157	0.056	0.0180	-	0.12
Resistors/Amplifiers/Thin oxide	**Not Used**	Used	Used	Used	Not Used	Not Used	Used	Not Used
Result Type	**Simulated**	Measured	Measured	Simulated	Measured	Simulated	Simulated	Measured

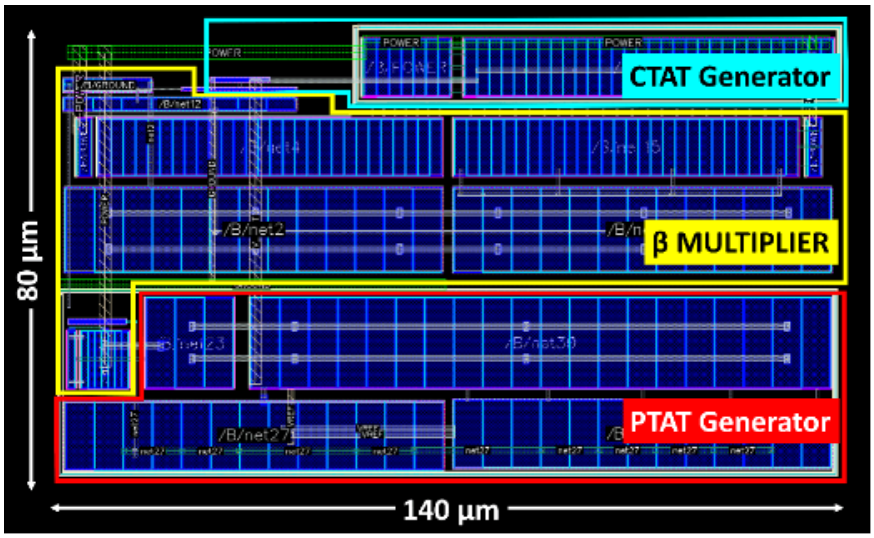

Figure 5.9: Layout of proposed voltage/current reference

Chapter 6

Conclusion and Future Work

This work presents the design and working of ultra-low power Resistance-to-Digital Converter (RDC) for miniature battery power sensing systems like biomedical systems and low-power IoT applications. Designed in 180nm CMOS process, the whole system works at 162nW, and the power consumption remains constant with a high input resistance range of 50kΩ to 1MΩ. This enables the RDC to be reconfigured to use as pressure sensors, temperature sensors, touch sensors, etc.

Along with that, it focused on designing always-on blocks like Voltage and Current References that are essential to almost all circuit design applications. It's really important to minimize the power consumption as low as possible. This thesis eliminates the use of high-value resistances in reference designs by using gate leakage currents of mosfet and designing a trim-free sub-Bandgap voltage reference. It consumes almost constant power for a very large temperature range and eliminates the exponential power consumption issue. It achieves one of the best line sensitivities of 0.0066%/V for a supply range of 0.7V to 4V and a PSRR of 89dB at DC and 1V supply. It works for a wide temperature range of -40°C to 150°C. Due to the use of BJT-based architecture, it works effectively without trimming. However, in general, it's more difficult to design trim-free ultra-low-power current references. Most of the low-power, low-voltage current references are CMOS-based, and they suffer from process variation. Hence, trimming is essential, which increases area and cost.

So, we focused on designing an ultra-low power CMOS Current/Voltage reference that works without trimming. This combined system is implemented without using any amplifiers and resistors. Hence, it doesn't get affected by amplifier offset errors and takes much less area by avoiding high-value resistances. Instead, we used the sub-threshold triode region of mosfet, which offers high resistance with low area. In this design, the process variation of both the voltage and current reference is cancelled, and this design can work without trimming. It achieves the process variation of the proposed voltage/current reference is $1.34\%(\sigma/\mu)$ / $1.75\%(\sigma/\mu)$.

There is a lot of scope for improvement in the presented work. Some of them are mentioned here:

1. Design of an RC to Digital converter in ultra-low power regime with large input range with reconfigurability and improved noise performance and FoM.

2. Development of current reference, voltage reference, and temperature sensor in ultra-low power range operational from 0.3V supply so it can be directly powered by energy harvesters.

Related Publications

6.1 Relevent Publications [Published]

1. **Arnab Dey**; I. Lee, A. Ali, A. Jain, A. Pullela and Z. Abbas ***"A 162nW, 0.845pJ/step Resistance-to-Digital Converter for Miniature Battery-Powered Sensing Systems,"***, *2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5, doi: 10.1109/ISCAS46773.2023.10181881.*

2. **Arnab Dey**; B. Subramaniam, A. Ali, B. Sahishnavi, A. Pullela and Z. Abbas ***"A 2.3nW Gate-Leakage Based Sub-Bandgap Voltage Reference with Line Sensitivity of 0.0066%/V from 40°C to 150°C for Low-Power IoT Systems,"***, *2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5, doi: 10.1109/ISCAS46773.2023.10182117.*

3. **Arnab Dey**; Chetan Mittal, Arnab Dey, Anubhab Banerjee, Ashfakh Ali, and Zia Abbas ***"A 37nW, All-in-One Trim-free Voltage/Current Reference without using Resistors and Amplifiers,"***, *2023 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Tempe, AZ, USA, 2023, pp. 50-54, doi: 10.1109/MWSCAS57524.2023.10405952.*

4. **Arnab Dey**, Bhartipudi Sahishnavi, Anubhab Banerjee, A Zahra, and Zia Abbas ***"A 275pW, 0.5V Supply insensitive Gate-leakage based Voltage/Current Reference circuit for a wide temperature range of -55 to 100°C without using Amplifiers and Resistors,"***, *Microelectronics Journal, Elsevier 2024, 106277, ISSN 0026-2692, https://doi.org/10.1016/j.mejo.2024.106277*

5. Chetan Mittal, **Arnab Dey**, Anubhab Banerjee, Ashfakh Ali, and Zia Abbas ***"A 0.8-V, 593-pA Trim-free Duty-cycled All CMOS Current Reference for Ultra-Low Power IoT Applications,"***, *2024 37th International Conference on VLSI Design and 2024 23rd International Conference on Embedded Systems (VLSID), Kolkata, India, 2024, pp. 599-604, doi: 10.1109/VLSID60093.2024.00106.*

6. Bhartipudi Sahishnavi, Sampath Kumar, Ashfakh Ali, **Arnab Dey**, Inhee Lee, and Zia Abbas ***"A 0.5V, pico-watt, 0.06%/V / 0.03%/V low supply sensitive current/voltage reference without using amplifiers and resistors,"***, *2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5, doi: 10.1109/ISCAS46773.2023.10181881.*

7. Abhinav Vajrala, Dheekshith Akula, **Arnab Dey**, Khanh M Le, and Zia Abbas ***"A 250pA, Gate-Leakage Based Trimming Free Current Reference, From -55^oC to 150^oC For Lower Power IoT Applications,"***, *2023 IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS), Tempe, AZ, USA, 2023, pp. 152-156, doi: 10.1109/MWSCAS57524.2023.10406027.*

Bibliography

[1] "iot-analytics.com/iot-market-size/,"

[2] D.-H. Seo, B. Chatterjee, S. Scott, D. Valentino, D. Peroulis, and S. Sen, "A wearable cmos biosensor with 3 designs of energy-resolution scalable time-based resistance to digital converter," *arXiv preprint arXiv:2011.00649*, 2020.

[3] E. Sacco, J. Vergauwen, and G. Gielen, "A 16.1-bit resolution 0.064-mm 2 compact highly digital closed-loop single-vco-based 1-1 sturdy-mash resistance-to-digital converter with high robustness in 180-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2456–2467, 2020.

[4] A. K. George, W. Shim, M. Je, and J. Lee, "A 114-af rms-resolution 46-nf/10-mω-range digital-intensive reconfigurable rc-to-digital converter with parasitic-insensitive femto-farad baseline sensing," in *2018 IEEE Symposium on VLSI Circuits*, pp. 157–158, IEEE, 2018.

[5] K.-C. Woo and B.-D. Yang, "0.3-v rc-to-digital converter using a negative charge-pump switch," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 2, pp. 245–249, 2019.

[6] B. Razavi, *Design of Analog CMOS Integrated Circuit*. McGraw-Hill Education, 2021.

[7] M. Jang, C. Lee, and Y. Chae, "Analysis and design of low-power continuous-time delta-sigma modulator using negative-r assisted integrator," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 277–287, 2019.

[8] S. Oh, Y. Shi, G. Kim, Y. Kim, T. Kang, S. Jeong, D. Sylvester, and D. Blaauw, "A 2.5 nj duty-cycled bridge-to-digital converter integrated in a 13mm 3 pressure-sensing system," in *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 328–330, IEEE, 2018.

[9] S. Jeong, Y. Kim, G. Kim, and D. Blaauw, "A pressure sensing system with$\pm$0.75 mmhg (3σ) inaccuracy for battery-powered low power iot applications," in *2020 IEEE Symposium on VLSI Circuits*, pp. 1–2, IEEE, 2020.

[10] S. Jeong, Z. Foo, Y. Lee, J.-Y. Sim, D. Blaauw, and D. Sylvester, "A fully-integrated 71 nw cmos temperature sensor for low power wireless sensor nodes," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1682–1693, 2014.

[11] A. Kempitiya, D.-A. Borca-Tasciuc, and M. M. Hella, "Low-power asic for microwatt electrostatic energy harvesters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 12, pp. 5639–5647, 2013.

[12] K. Yang, Q. Dong, W. Jung, Y. Zhang, M. Choi, D. Blaauw, and D. Sylvester, "9.2 a 0.6 nj- 0.22/+ 0.19 c inaccuracy temperature sensor using exponential subthreshold oscillation dependence," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 160–161, IEEE, 2017.

[13] W. Choi, Y.-T. Lee, S. Kim, S. Lee, J. Jang, J. Chun, K. A. Makinwa, and Y. Chae, "A 0.53 pjk 2 7000μm 2 resistor-based temperature sensor with an inaccuracy of$\pm$0.35° c (3σ) in 65nm cmos," in *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 322–324, IEEE, 2018.

[14] L. J. Nervegna, *A precision CMOS continuous-time autozeroed op-amp*. PhD thesis, Massachusetts Institute of Technology, 2001.

[15] S. Pan and K. A. Makinwa, "10.4 a wheatstone bridge temperature sensor with a resolution fom of 20fj. k 2," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 186–188, IEEE, 2019.

[16] D. Lee and G. Han, "High-speed, low-power correlated double sampling counter for column-parallel cmos imagers," *Electronics Letters*, vol. 43, no. 24, pp. 1362–1364, 2007.

[17] B. Tiwari, P. G. Bahubalindruni, S. Deb, and J. Goes, "Robust linear sampling switch for low-voltage sar adcs," *Analog Integrated Circuits and Signal Processing*, vol. 103, no. 2, pp. 345–353, 2020.

[18] B. Razavi, "The bootstrapped switch [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 3, pp. 12–15, 2015.

[19] B. Lee, H. Kim, J. Kim, K. Han, D.-i. D. Cho, and H. Ko, "A low-power 33 pj/conversion-step 12-bit sar resistance-to-digital converter for microsensors," *Microsystem Technologies*, vol. 25, no. 5, pp. 2093–2098, 2019.

[20] G. Ge et al, "A Single-Trim CMOS Bandgap Reference With a 3σ Inaccuracy of $\pm 0.15\%$ From -40^oC to 125^oC,"

[21] C. M. Andreou, S. Koudounas, and J. Georgiou, "A Novel Wide-Temperature-Range, 3.9 ppm/^{o}C CMOS Bandgap Reference Circuit," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 574–581, 2012.

[22] Z. Zhou, Y. Shi, Z. Huang, P. Zhu, Y. Ma, Y. Wang, Z. Chen, X. Ming, and B. Zhang, "A 1.6-V 25-μA 5-ppm/^{o} C Curvature-Compensated Bandgap Reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 4, pp. 677–684, 2012.

[23] K. Chen, L. Petruzzi, R. Hulfachor, and M. Onabajo, "A 1.16-V 5.8-to-13.5-ppm/^{o}C Curvature-Compensated CMOS Bandgap Reference Circuit With a Shared Offset-Cancellation Method for Internal Amplifiers," *IEEE Journal of Solid-State Circuits*, pp. 1–1, 2020.

[24] G. Ge, C. Zhang, G. Hoogzaad, and K. A. A. Makinwa, "A single-trim cmos bandgap reference with a 3σ inaccuracy of $\pm 0.15-40^{\circ}$c to 125°c," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 11, pp. 2693–2701, 2011.

[25] Z.-K. Zhou, Y. Shi, Z. Huang, P.-S. Zhu, Y.-Q. Ma, Y.-C. Wang, Z. Chen, X. Ming, and B. Zhang, "A 1.6-v 25-μ a 5-ppm/$^{\circ}$ c curvature-compensated bandgap reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 4, pp. 677–684, 2012.

[26] K. Chen, L. Petruzzi, R. Hulfachor, and M. Onabajo, "A 1.16-v 5.8-to-13.5-ppm/$^{\circ}$c curvature-compensated cmos bandgap reference circuit with a shared offset-cancellation method for internal amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 1, pp. 267–276, 2021.

[27] E. Boufouss, L. Francis, P. Gerard, M. Assaad, and D. Flandre, "Ultra low power cmos circuits working in subthreshold regime for high temperature and radiation environments," *Additional Papers and Presentations*, vol. 2011, no. HITEN, pp. 000243–000250, 2011.

[28] K. K. Lee, T. S. Lande, and P. D. Häfliger, "A sub-μw bandgap reference circuit with an inherent curvature-compensation property," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 1, pp. 1–9, 2015.

[29] W. Huang, L. Liu, and Z. Zhu, "A sub-200nw all-in-one bandgap voltage and current reference without amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 1, pp. 121–125, 2021.

[30] J. M. Lee, Y. Ji, S. Choi, Y.-C. Cho, S.-J. Jang, J. S. Choi, B. Kim, H.-J. Park, and J.-Y. Sim, "5.7 a 29nw bandgap reference circuit," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 1–3, 2015.

[31] M. Kim and S. Cho, "A 0.8v, 37nw, 42ppm/$^{\circ}$c sub-bandgap voltage reference with psrr of 81db and line sensitivity of 51ppm/v in 0.18um cmos," in *2017 Symposium on VLSI Circuits*, pp. C144–C145, 2017.

[32] G. Chowdary, K. Kota, and S. Chatterjee, "A 1-nw 95-ppm/$^{\circ}$c 260-mv startup-less bandgap-based voltage reference," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, 2020.

[33] Y.-P. Chen, M. Fojtik, D. Blaauw, and D. Sylvester, "A 2.98nw bandgap voltage reference using a self-tuning low leakage sample and hold," in *2012 Symposium on VLSI Circuits (VLSIC)*, pp. 200–201, 2012.

[34] I. Lee and D. Blaauw, "A 31 pw-to-113 nw hybrid bjt and cmos voltage reference with 3.6high-temperature iot systems," in *2019 Symposium on VLSI Circuits*, pp. C142–C143, 2019.

[35] I. Lee, D. Sylvester, and D. Blaauw, "A subthreshold voltage reference with scalable output voltage for low-power iot systems," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1443–1449, 2017.

[36] I. Lee, D. Sylvester, and D. Blaauw, "Subthreshold voltage reference with nwell/psub diode leakage compensation for low-power high-temperature systems," in *2017 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 265–268, 2017.

[37] C.-Z. Shao and Y.-T. Liao, "A 650 pw,- 71 db psrr, 205° c temperature range hybrid voltage reference with curvature-based temperature compensation and sbfl techniques," in *2021 Symposium on VLSI Circuits*, pp. 1–2, IEEE, 2021.

[38] M. Liu, A. van Roermund, and P. Harpe, "A 0.9v-vdd sub-nw resistor-less duty-cycled cmos voltage reference in 65nm for iot," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, 2017.

[39] L. Wang, C. Zhan, J. Tang, Y. Liu, and G. Li, "A 0.9-v 33.7-ppm/°c 85-nw sub-bandgap voltage reference consisting of subthreshold mosfets and single bjt," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 2190–2194, 2018.

[40] A. Pullela, A. Ali, S. Reddy, A. Jain, and Z. Abbas, "A 443pW Accumulation-Mode Gate-Leakage Based Bandgap Reference for IoT Applications," in *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 986–989, 2021.

[41] A. Ali, A. Pullela, A. Jain, and Z. Abbas, "A Sub-nW, 8T Current Reference Consuming Constant Power wrt Process & Temperature," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 730–733, IEEE, 2020.

[42] J. Lim, T. Jang, M. Saligane, M. Yasuda, S. Miyoshi, M. Kawaminami, D. Blaauw, and D. Sylvester, "A 224 pw 260 ppm/° c gate-leakage-based timer for ultra-low power sensor nodes with second-order temperature dependency cancellation," in *2018 IEEE Symposium on VLSI Circuits*, pp. 117–118, IEEE, 2018.

[43] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "1.2-v supply, 100-nw, 1.09-v bandgap and 0.7-v supply, 52.5-nw, 0.55-v subbandgap reference circuits for nanowatt cmos lsis," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1530–1538, 2013.

[44] H. Wang and P. P. Mercier, "A 51 pw reference-free capacitive-discharging oscillator architecture operating at 2.8 hz," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–4, IEEE, 2015.

[45] H. Wang and P. P. Mercier, "A 1.6%/v 124.2 pw 9.3 hz relaxation oscillator featuring a 49.7 pw voltage and current reference generator," in *ESSCIRC 2017-43rd IEEE European Solid State Circuits Conference*, pp. 99–102, IEEE, 2017.

[46] U. Chi-Wa, W.-L. Zeng, M.-K. Law, C.-S. Lam, and R. P. Martins, "A 0.5-v supply, 36 nw bandgap reference with 42 ppm/° c average temperature coefficient within- 40° c to 120° c," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 3656–3669, 2020.

[47] Y. Liu, C. Zhan, L. Wang, J. Tang, and G. Wang, "A 0.4-v wide temperature range all-mosfet subthreshold voltage reference with 0.027sensitivity," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 8, pp. 969–973, 2018.

[48] B. B. Yadav, K. Mounika, A. Bathi, and Z. Abbas, "67ppm/°c, 66na pvt invariant curvature compensated current reference for ultra-low power applications," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, 2020.

[49] B.-D. Yang, Y.-K. Shin, J.-S. Lee, Y.-K. Lee, and K.-C. Ryu, "An accurate current reference using temperature and process compensation current mirror," in *2009 IEEE Asian Solid-State Circuits Conference*, pp. 241–244, 2009.

[50] E. K. F. Lee, "Low voltage cmos bandgap references with temperature compensated reference current output," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pp. 1643–1646, 2010.

[51] J. Lee and S. Cho, "A 1.4-μw 24.9-ppm/°c current reference with process-insensitive temperature compensation in 0.18-μm cmos," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2527–2533, 2012.

[52] D. Osipov and S. Paul, "Compact extended industrial range cmos current references," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 6, pp. 1998–2006, 2019.

[53] M. Choi, I. Lee, T.-K. Jang, D. Blaauw, and D. Sylvester, "A 23pw, 780ppm/°c resistor-less current reference using subthreshold mosfets," in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, pp. 119–122, 2014.

[54] H. Wang and P. P. Mercier, "A 420 fw self-regulated 3t voltage reference generator achieving 0.47%/v line regulation from 0.4-to-1.2 v," in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, pp. 15–18, 2017.

[55] Q. Dong, I. Lee, K. Yang, D. Blaauw, and D. Sylvester, "A 1.02nw pmos-only, trim-free current reference with 282ppm/°c from 40°c to 120°c and 1.6% within-wafer inaccuracy," in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, pp. 19–22, 2017.

[56] K. Kimura, "Low voltage techniques for bias circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 5, pp. 459–465, 1997.

[57] M. S. Eslampanah Sendi, S. Kananian, M. Sharifkhani, and A. M. Sodagar, "Temperature compensation in cmos peaking current references," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 9, pp. 1139–1143, 2018.

[58] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, first ed., 2001.

[59] Y. Wang, Q. Sun, H. Luo, X. Wang, R. Zhang, and H. Zhang, "A 48 pw, 0.34 v, 0.019%/v line sensitivity self-biased subthreshold voltage reference with dibl effect compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 2, pp. 611–621, 2020.

[60] B. Ma and F. Yu, "A novel 1.2–v 4.5-ppm/°c curvature-compensated cmos bandgap reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 4, pp. 1026–1035, 2014.

[61] A. Ali, A. Pullela, A. Jain, and Z. Abbas, "A sub-nw, 8t current reference consuming constant power w.r.t process temperature," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 730–733, 2020.

[62] H. Wang and P. P. Mercier, "A 14.5 pw, 31 ppm/°c resistor-less 5 pa current reference employing a self-regulated push-pull voltage reference generator," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1290–1293, 2016.

[63] D. Lee, D. Blaauw, and D. Sylvester, "Gate oxide leakage current analysis and reduction for vlsi circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 2, pp. 155–166, 2004.

[64] A. Jain, A. Ali, S. Kiran, and Z. Abbas, "A high psrr, stable cmos current reference using process insensitive tc of resistance for wide temperature applications," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, 2019.

[65] C. M. Andreou, S. Koudounas, and J. Georgiou, "A novel wide-temperature-range, 3.9 ppm/°c cmos bandgap reference circuit," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 574–581, 2012.

[66] H.-M. Chen, C.-C. Lee, S.-H. Jheng, W.-C. Chen, and B.-Y. Lee, "A sub-1 ppm/°c precision bandgap reference with adjusted-temperature-curvature compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 6, pp. 1308–1317, 2017.

[67] W. Huang, L. Liu, and Z. Zhu, "A sub-200nw all-in-one bandgap voltage and current reference without amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 1, pp. 121–125, 2021.

[68] L. Wang, C. Zhan, J. Tang, Y. Liu, and G. Li, "A 0.9-v 33.7-ppm/°c 85-nw sub-bandgap voltage reference consisting of subthreshold mosfets and single bjt," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 2190–2194, 2018.

[69] L. Wang, C. Zhan, J. Tang, Y. Liu, and G. Li, "A 0.9-v 33.7-ppm/°c 85-nw sub-bandgap voltage reference consisting of subthreshold mosfets and single bjt," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 2190–2194, 2018.