Low Power Analog Circuit Design and Radio Frequency Circuits for Biomedical Applications

Thesis submitted in partial fulfillment
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CERTIFICATE

It is certified that the work contained in this thesis, titled ***"Low Power Analog Circuit Design and Radio Frequency Circuits for Biomedical Applications"*** by Samriddhi Agarwal, has been carried outunder my supervision and is not submitted elsewhere for a degree.

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Date Adviser: Dr. Zia Abbas

To *My Family and Friends*

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Abstract

In the last few years, implantable medical devices are being used for the treatment of a growing num-ber of pathologies. Implantable medical devices are sophisticated electronic circuits that are implanted into the body to restore or improve various body functions in patients. These devices can perform a range of tasks including sensing, control, and stimulation, which enables them to monitor and regulate the health of the patient. The electronics of a general biomedical device typically consist of several subsystems that work together to perform the desired functions. For example, energy delivery subsys-tem, analog-to-digital conversion subsystem, signal processing subsystem, communication subsystem. The stringent energy constraints dominate the design of biomedical systems. Additionally, systems powered through energy harvesting must be able to work with lower supply voltages.

Low power consumption, low supply voltage and accuracy are few of the most important parameters for bio-implants. With all these constraints in play, we have put efforts to design current reference and voltage reference as they are present in almost every analog and mixed signal system. Efforts were put to design a low power current reference with high line sensitivity using peaking current source by exploiting the back-gate effect of a MOSFET in sub-threshold region. The design works from a 0.55V supply voltage and generates a reference current of 5.6nA. A low line sensitivity of 0.022%/V is achieved and the design works for a temperature range of 0-80°C. This current reference shows the best result of line sensitivity among the previous state-of-the-art works. Consequently, we have come up with a switched capacitor network-based bandgap voltage reference (BGR) circuit designed to achieve high accuracy and low power consumption for implantable biomedical applications. A low-power clock generator circuit is proposed, to reduce the leakage current thereby reducing the circuit's power consumption to 18.5nW at typical conditions. The design works from a supply voltage of 0.5V and has a TC of 74.5ppm/°C over a temperature range of 0-80°C. Lastly, we have expanded our research to the field of RF circuits for biomedical applications. An on-chip Vector Network Analyzer (VNA) is designed to detect a biomolecule for medical diagnosis. This technique, known as RF sensing, can be used to detect changes in the dielectric properties of a sample, which can indicate the presence of certain biomolecule. In this part of the research, various blocks of the on-chip VNA is demonstrated and the future scope of this work is explained.

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Chapter 1

Introduction

1.1 Motivation of Low Power Design for Biomedical Applications

From the first integrated circuit (IC) to more advanced IC products found in every corner of the world, the semiconductor industry has continued forward from its first success by fast-pacing improvement in higher integration levels, lowered costs, higher speeds, lower power consumption, reduced and newer functionality. For portable applications that are battery-powered, power consumption directly determines battery life between recharge cycles, functionality, system performance, and the physical dimensions/weight of the system.Besides conventional applications, including the wristwatch, hearing aid, and pacemaker, new applications using low-power are appearing daily. Generally, these applications tend to have low speed, low accuracy requirements, and low activity rates, but at the same time, can greatly benefit from an energy efficiency that allows more portability, a reduced complexity, and cost reduction. With innovations in circuit design techniques, and with right technical approach complex biomedical applications are now becoming entirely implantable. The electronics of a general biomedical device typically consist of several subsystems that work together to perform the desired functions. These subsystems include:

- Energy delivery subsystem: This subsystem is responsible for supplying power to the device. It may consist of a battery or energy harvesting techniques to convert environmental energy into electrical energy.

- Analog-to-digital conversion subsystem: This subsystem is responsible for converting analog signals into digital signals for processing. This is often necessary for signals such as biomedical signals, which are typically analog in nature.

- Signal processing subsystem: This subsystem is responsible for processing the signals from the sensors and performing various tasks such as amplification, filtering, and signal analysis. The signal processing subsystem plays a critical role in determining the accuracy and reliability of the device.

- Communication subsystem: This subsystem is responsible for communicating data between the device and external devices, such as a monitoring system or control system. This subsystem may use wired or wireless communication protocols depending on the specific application and requirements.
- These subsystems work together to provide a complete solution for the biomedical device. The design and implementation of these subsystems must consider factors such as power consumption, accuracy, reliability, and compatibility with the human body to ensure safe and effective operation.

Various existing and emerging biomedical applications are listed below:

- Pacemaker and cardioverterdefibrillator
- Hearing aid
- Analog cochlear processor
- Neural recording
- Retinal stimulator
- Biomolecule detection for medical diagnosis

All these various biomedical applications can be covered under wide range of low power analog and RF circuits. First demonstrated in the 1950s, one of most common implanted biomedical devices is the pacemaker. The average power consumption of a pacemaker is in the order of five to ten microwatts, and is enabled by the minimal processing requirements and low analog-to-digital converter (ADC) speeds (100–1000 samples per second). Biomedical systems often have stringent energy constraints because they are powered by batteries or other limited energy sources, and they must operate for long periods of time without being recharged or replaced. Additionally, many biomedical systems are implantable or otherwise worn on the body, and they must be small and lightweight to minimize discomfort for the user. To meet these energy constraints, biomedical systems often use ultra-low-power circuits that require specialized techniques such as low-voltage and low-power design, power management, and energy harvesting. These techniques have specific trade-offs and limitations, such as reduced performance or increased complexity, that must be carefully considered during the design process.

1.2 Analog and RF circuits for Biomedical Applications

Among the various low power biomedical applications listed in the previous section, low power analog and RF circuit designs are developed to meet the requirements. Analog circuits are used in a variety of biomedical applications, including medical instrumentation, signal processing, and control systems.

In medical instrumentation, analog circuits are used to amplify, filter and condition signals from various sensors such as electrocardiogram, electroencephalogram and other biomedical sensors. These signals are usually weak and noisy, so the analog circuits are used to amplify the signal and filter out any unwanted noise. Analog circuits are also used in signal processing to extract relevant information from biomedical signals. For example, in ECG (Electrocardiogram) signal processing, analog circuits are used to filter out noise and detect the QRS complex which is used to detect the heart rate. In control systems, analog circuits are used to control various medical devices such as drug pumps, ventilators, and dialysis machines. These devices require precise control of the flow rate, pressure, and other parameters, and analog circuits are used to control these parameters in a continuous and smooth manner. In addition, analog circuits are also used in diagnostic systems such as electrocardiogram (ECG) and electroencephalogram (EEG) to measure and record electrical activity in the heart and brain respectively. The critical components of biomedical electronic devices, namely the energy subsystem, the signal processor, the ADC, and the communication transceiver, are treated and analyzed individually with specific consideration to state-of-the-art and emerging approaches to power management. Current and voltage references are one of the most crucial analog blocks used in bioimplants. Current references are needed for many major building blocks in analog circuits, such as operational amplifiers, analog buffers, oscillators, phase locked loops, analog-to-digital converters and digital-to-analog converters. A current reference circuit may be used to provide a bias current when high precision is required. The bias current provided by a current reference circuit ensures the stable and precise operation of the analog circuit in which it is used. Current references that are simple, efficient and easy to design are highly desired. The voltage reference is truly an essential and versatile circuit to almost all electronics systems. As a voltage reference circuit, one of most common applications is to generate different levels of bias voltage for system function and provide voltage thresholds for detecting various events. The generated voltage needs to be stable and accurate to qualify as a good reference to ensure system functionality and precision requirements

RF (Radio Frequency) circuits are used in a variety of biomedical applications, including medical imaging, wireless communication between medical devices, and therapeutic applications such as RF ablation (a treatment for certain types of cancer) and electrosurgery. In medical imaging, RF circuits are used in MRI (magnetic resonance imaging) scanners to generate the high-frequency electromagnetic fields that are used to produce detailed images of internal body structures. In wireless communication between medical devices, RF circuits are used to transmit data and control signals between devices such as implantable pacemakers and external controllers. In therapeutic applications, RF circuits are used to generate the high-frequency electrical energy that is used to destroy unwanted tissue or to control bleeding during surgery. Radio frequency (RF) signals can be used to detect biomolecules in medical diagnosis. This technique, known as RF sensing, can be used to detect changes in the dielectric properties of a sample, which can indicate the presence of certain biomolecules. For example, RF signals can be used to detect changes in the dielectric constant of a sample caused by the binding of a specific

biomolecule. This technique can be used in a variety of medical applications, such as cancer diagnosis, disease detection and drug discovery. The flow of the above concept is shown in Fig. 1.1

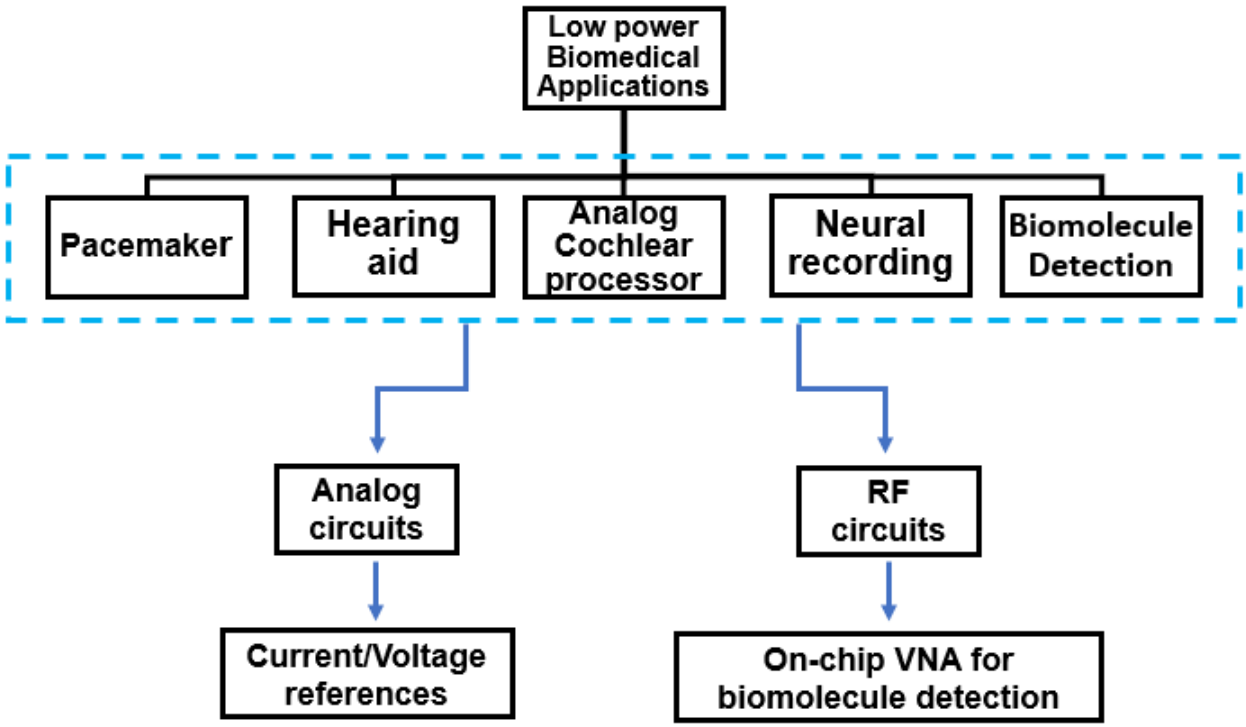


Figure 1.1 Flowchart of Biomedical Applications

1.3 Thesis Organization

In this manuscript, we present several circuit level techniques to cater various applications in biomedical designs. This thesis mainly presents commonly used bioimplants sub-system like current refernce, voltage reference. Along with current and voltage reference, this thesis expands to RF field and presents detection of biomolecule by using on-chip VNA.

In Chapter 2, we propose a nano-watt current reference design using a peaking current source by exploiting the back-gate effect of a MOSFET operating in sub-threshold region. The proposed current reference works on the principle of generating a temperature independent current reference by taking ratio of a compensated voltage and on-chip resistance without using an operational amplifier. The circuit works from a supply voltage of 0.55V and is designed for a reference current of 5.6nA. Furthermore, a pseudo-differential amplifier (PD-AMP) helps realize low line regulation of 0.022%/V in the supply range of 0.55 to 1.9V. An average temperature coefficient (TC) of 256.07ppm/°C is achieved for mismatch and process variations in Monte-Carlo simulations for 1000 samples over a temperature range of

-30°C to 70°C. The circuit consumes only 9.5nW of power (at room temperature and minimum supply voltage), making it suitable for ultra-low-power biomedical applications.

In Chapter 3, we propose a switched-capacitor network (SCN) based fractional bandgap voltage reference (BGR) circuit designed in 180nm CMOS process to achieve high accuracy and low power consumption for implantable biomedical applications. The design proposes a V_{EB} generator that employs a 2x charge pump and an improved SCN to generate a temperature independent reference voltage (V_{REF}). A low-power clock generator circuit is proposed, to reduce the leakage current thereby reducing the circuit's power consumption to 18.5nW at typical conditions. The design works from a supply voltage of 0.5V and has a TC of 74.5ppm/°C over a temperature range of 0-80°C. The PSRR of the circuit is -62.9dB at 100Hz. Based on the Monte Carlo simulations of 500 samples, we obtain an untrimmed $3\sigma/\mu$ of 2.6%. The design occupies an active area of $0.027mm^2$.

In Chapter 4, we propose various designs of on-chip Vector Network Analyser in 65nm CMOS technology to detect biomolecule for cell investigation, medical diagnosis and treatment. A fully integrated CMOS on-chip VNA is explained which detects the resonant frequency of the biosensor by varying the capacitance of the DUT. The design uses the concept of s-parameter to identify the DUT. The design works from a frequency range of 0.5GHz to 2GHz. The biomolecule/DUT is represented by a series RLC circuit. The objective of the work was to make an working concept of an on-chip VNA which can detect any change in the biomolecule. Shift in the resonant frequency is observed due to capacitance change caused by addition of sample with significant relative permittivity. From the resonant frequency information, the value of permittivity of the sample can be found out.

Finally in Chapter 5, we present the conclusions of the work done so far. We also discuss the improvements that can be further done, and the future scope of the work

Chapter 2

Low Power CMOS Current Reference

2.1 Introduction

With the development of non-intrusive wearable sensors in the biomedical field, low-supply voltage, temperature, and supply independent current reference has become a prerequisite to design low-power blocks like Op-Amps, oscillators etc. The design of biomedical devices like cochlear implants demands current reference to bias all internal analog circuitry. These implantable systems should comply with low power budget which restricts the power to nano-watt or sub nano-watt range. For fully implantable devices, there is a wireless transmission of digital data. Due to noise generated by digital switching, current reference should be able to work under noisy environment. Since there is a trade-off between the power consumption and the accuracy of a current reference, designing a current reference for implantable and portable biomedical circuits is a severe challenge.

A wide variety of circuit configurations have been proposed to realize a current reference. Broadly it can be categorized as shown in Fig 2.1. Conventional current reference is either the variants of beta multiplier or based on division of voltage and resistance using op-amp. The most recently reported current reference uses the sum of CTAT and PTAT currents[1, 2, 3]. Process insensitive temperature compensation is achieved in [4] by taking the ratio of compensated voltage and on-chip resistance, but at the

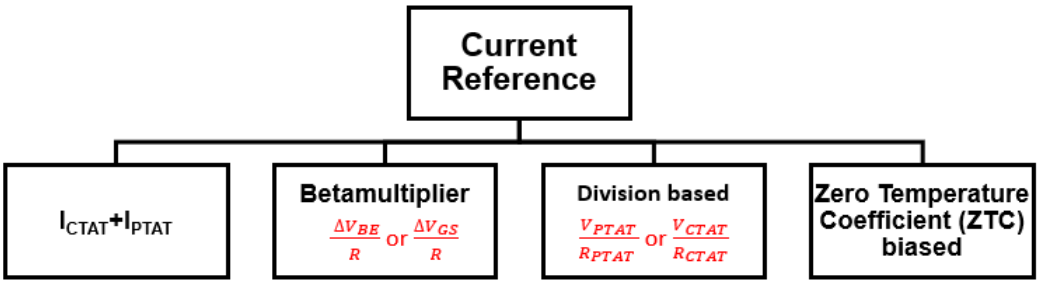


Figure 2.1 Categorization of current references

cost of higher supply voltage and power consumption. The design proposed in [5] achieved a current reference for a wide temperature range but has a poor line sensitivity and minimum supply voltage of 2.2 V. A resistor-less CMOS current reference is proposed in [6], but has a poor TC. Zero Temperature Coefficient (ZTC) biasing is proposed in [7] to generate temperature compensated current reference but has a limited minimum supply voltage (>1.5V), and the line regulation is also influenced due to second-order effects. One of the possible designs for current reference circuits is based on peaking current source[8]. Authors in [9] proposed a modification in the conventional peaking current source for temperature compensation by adding an n-well resistor but has a poor TC and the line regulation which is unacceptable in some applications due to short channel effects.

Considering the limitations of above state-of -the-art works, the proposed architecture deals with designing of a nano-watt current reference using a peaking current source by exploiting the back gate effect of a MOSFET in sub-threshold region. The rest of the chapter is broadly divided into seven sections. Section 2.2 provides the principle of proposed design. Section 2.3 discusses the design methodology of the proposed circuit. The supply independent peaking current source is explained in section 2.4. Section 2.5 discussed about the CTAT voltage generator. The proposed temperature compensation technique is discussed in section 2.6. Finally, section 2.7 discusses the results and section 2.8 summarizes the chapter.

2.2 Principle of Proposed Current Reference

The proposed current reference works on the principle of generating a temperature independent current by taking the ratio of a compensated voltage *(V_{comp})* and on-chip resistance without using an opamp as shown in equation:

$$I_{ref} = \frac{V_{comp}}{R} = \frac{V_{comp0}(1 + \alpha_{comp}\triangle T)}{R_0(1 + \alpha_R \triangle T)} \tag{2.1}$$

where, V_{comp0} and R_0 are the voltage and the resistance at nominal temperature T_0, and α_{comp}, α_R are their TCs, respectively. By making the TC of V_{comp} equal to the TC of the resistance, I_{ref} can be made temperature independent. This design uses the concept of the back-gate effect of critical MOSFET to generate complementary to absolute temperature (CTAT) voltage which is explained in section 2.6 of this chapter. The proportional to absolute temperature (PTAT) voltage is generated from the supply independent peaking current block by taking the difference of the gate to source voltage of the MOSFET as explained in section 2.4. Fig. 2.2 explains the top level architecture of the proposed idea.

2.3 Design of the proposed current reference

The proposed current reference is illustrated in Fig. 2.3. As explained in previous section the PTAT voltage is generated from the supply independent peaking current block by taking the difference of the gate to source voltage of the MOSFET MP3 and MP4. The CTAT voltage is generated by exploiting the

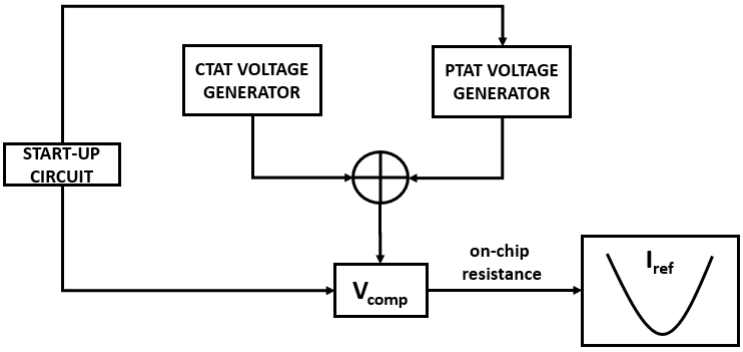


Figure 2.2 Architecture of proposed current reference

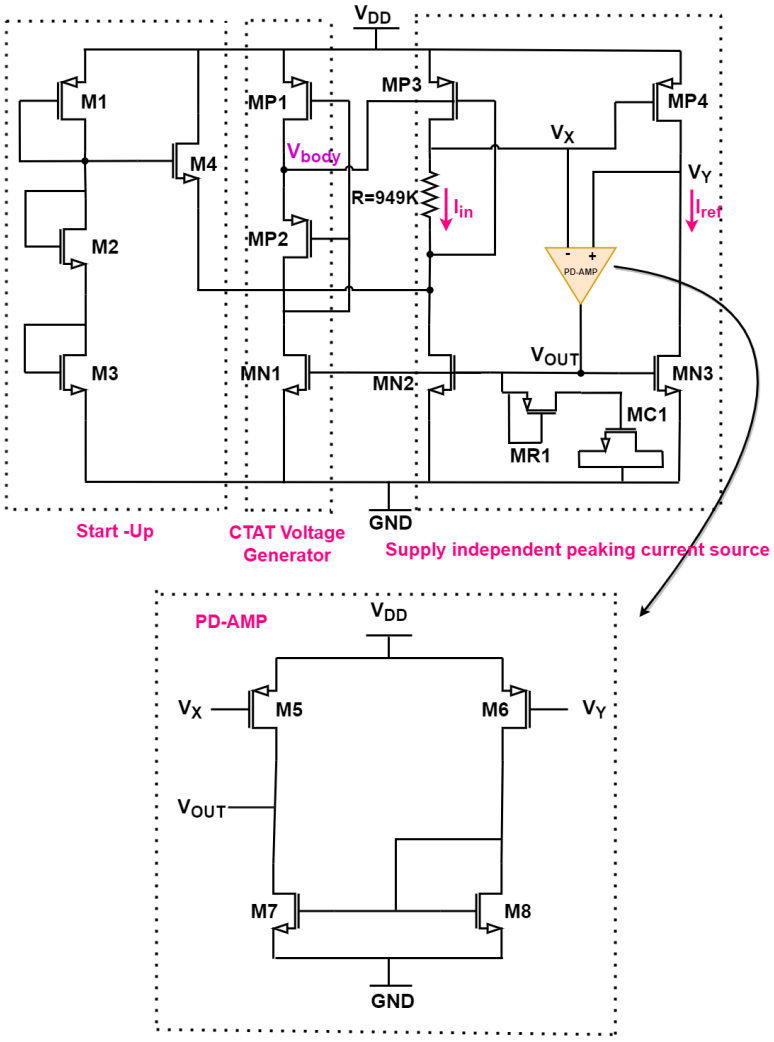


Figure 2.3 Design of proposed current reference

dependence of threshold voltage of MP3 on its body to source voltage. Transistors MR1 and MC1 is used for frequency compensation. All the MOSFETs operate in the sub-threshold region, which results in low power consumption. Transistors M1-M4 consist of the start-up circuit that brings out the core circuit from a dead operating point (zero current) to its normal operating point. When the circuit reaches the desired operating point, the start-up operation gets over.

2.4 Supply Independent peaking current source

2.4.1 Nagata current mirror

The conventional peaking current source called as Nagata Current source is shown in Fig. 2.4 [8].

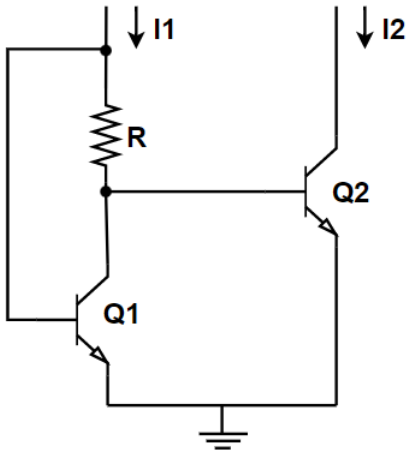


Figure 2.4 Conventional Nagata current mirror [8]

The relationship between the collector current and base to emitter voltage of a BJT can be expressed as:

$$I_C = I_S exp(\frac{V_{EB}}{V_T}) \tag{2.2}$$

where, V_T= KT/q is the thermal voltage, k is the Boltzman's constant , I_S is the saturation current for transistor. The relation between $I1$ and $I2$ current of a Nagata current mirror can be expressed as

$$I_2 = KI_1 exp(\frac{-RI_1}{V_T}) \tag{2.3}$$

We obtain the peak value when I_2 = KI_1/e at RI_1 = V_T [8]. Hence, Nagata current mirrors are also known as peaking current mirrors. Nagata current mirrors can also be composed of MOS transistors. Using this concept, we have implemented a peaking current source using NMOS current mirror as shown in Fig. 2.5

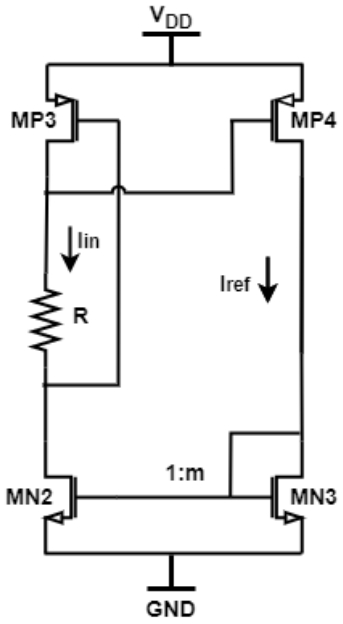


Figure 2.5 Proposed peaking current source

2.4.2 Proposed peaking current source

In this subsection, we illustrate the modification in the peaking current source demonstrated in [9]. The proposed design uses NMOS current mirror. Considering the supply independent peaking current block shown in Fig. 2.5

$$I_{in} = \frac{(V_{SG_{P3}} - V_{SG_{P4}})}{R} \tag{2.4}$$

When the drain-source voltage of a transistor *(V_{DS})* is more than *$4V_T$*, the well known subthreshold current equation can be written as: (well illustrated in [1])

$$I_D = I_S(\frac{W}{L})exp(\frac{V_{GS} - V_{TH}}{\eta V_T}) \tag{2.5}$$

where, $I_S = \mu_n(\eta - 1)C_{ox}V_T^2$; (W/L) is the ratio of transistor's width and length, V_{GS} is the gate to source voltage of the MOSFET, V_{TH} is the threshold voltage of the transistor, $V_T = KT/q$ is the thermal voltage which has a linear temperature dependency, μ_n is mobility and η is the subthreshold slope factor. From Eq. 2.3 and Eq.2.6 , I_{in} can be written as shown in Eq. 2.4.

$$I_{in} = \frac{V_{TH_{P3}} - V_{TH_{P4}} + \eta V_T ln(\frac{I_{in}K_4}{I_{ref}K_3})}{R} \tag{2.6}$$

Where, $K4/K3 = (W/L)_{MP4}/(W/L)_{MP3}$. MP3 and MP4 being similar V_{TH} MOSFET, I_{ref} can be written as:

$$I_{ref} = I_{in}\frac{K_4}{K_3}exp(\frac{-RI_{in}}{\eta V_T}) \tag{2.7}$$

Considering the current mirror, and assuming $m = (W/L)_{MN3}/(W/L)_{MN2}$ and MP3 and MP4 being similar V_{TH} MOSFET, Eq.2.7 can be written as shown in Eq. 2.8.

$$I_{ref} = \frac{m\eta V_T}{R} ln(\frac{K_4}{K_3 m}) \tag{2.8}$$

From Eq. 2.8 temperature coefficient of the output current is derived as

$$TC_{I_{ref}} = \frac{1}{I_{ref}} \frac{\partial I_{ref}}{\partial T} = -TC_R + TC_{V_T} \tag{2.9}$$

in which TC_R and TC_{V_T} are temperature coefficients of thermal voltage and R, respectively. To make $TC_{I_{ref}} = 0$, we have to make $TC_R = TC_{V_T}$. From the expression of V_T, we know $TC_{V_T} = 1/T$. I_{ref} can be made independent of temperature if $T = 1/TC_R$, which amounts to T=1000k which is not a feasible temperature value for any design. From Eq. 2.9, the reference current of a peaking current source cannot be made temperature independent.

The proposed architecture of peaking current source is made supply independent by pseudo-differential amplifier shown in Fig 2.3. For $V_{DS} \geq 4V_T$ the drain current of a MOSFET becomes almost independent of drain voltage (Eq. 2.5). Such current saturation is observed in long channel MOSFET where DIBL effect is negligible. In short channel MOSFET due to DIBL, drain current depends on V_{DS} since the threshold voltage becomes a function of V_{DS} [10].

$$V_{TH} = V_{TH_{int}} - \lambda_D V_{DS} \tag{2.10}$$

where, $V_{TH_{int}}$ is threshold voltage for V_{DS}=0 and λ_D is the DIBL effect factor. Therefore, currents in MP3 and MP4 are not exactly equal and vary with supply. A PD-AMP is used instead of a traditional op-amp to make the node voltage at V_X and V_Y equal so that the effects of DIBL is compensated. A MOSFET MC1 is used as a capacitor and MR1 is used as a resistor for frequency compensation. The PD-AMP consumes a current of 0.62nA which makes it suitable for ultra-low power applications. A phase margin of 37.50° is achieved for the feedback and loop gain of feedback is 39.5dB (Fig. 2.6) which is good enough to ensure low line regulation of 0.022%/V.

2.5 CTAT Voltage Generator

CTAT voltage generator block is depicted in Fig. 2.3. MP1 and MP2 are similar V_{TH} MOSFET. MP1, MP2 and MN1 are kept in subthreshold region. Since the current through MP1 and MP2 is equal, V_{body} can be expressed as:

$$V_{body} = \triangle V_{TH_{1,2}} + V_{DD} - \eta V_T ln(\frac{K_2}{K_1}) \tag{2.11}$$

$$\triangle V_{TH_{1,2}} = V_{TH_{P2}} - V_{TH_{P1}} \tag{2.12}$$

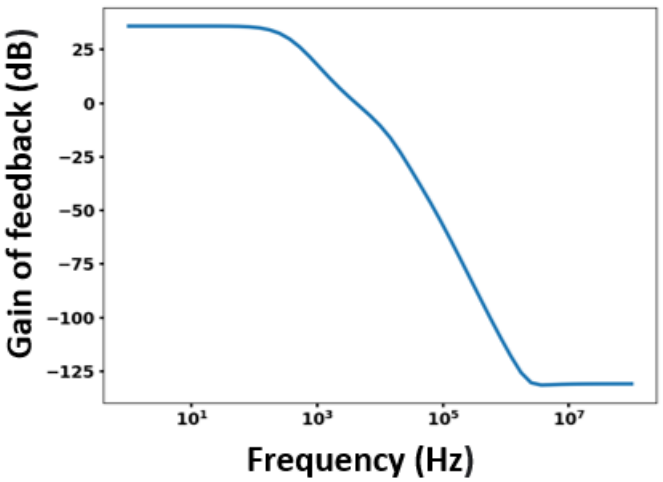


Figure 2.6 Loop gain of feedback

The term $V_{DD} - \eta V_T lnK2/K1$ in Eq. 2.11 generates a CTAT voltage. $\triangle V_{TH_{(1,2)}}$ is a very small value and MP1 and MP2 are similar type of MOSFET, so it can be neglected. By proper sizing of MP1 and MP2, the CTAT term can be controlled. The generated V_{body} can track V_{DD} making a constant $V_{body} - V_{DD}$ with respect to supply. As shown in Fig. 2.3, we use V_{body} to bias the body terminal of MOSFET MP3. Since $V_{body} - V_{DD}$ is constant, $|V_{BS}|$ of MP3 is supply insensitive as shown in Fig. 2.7.

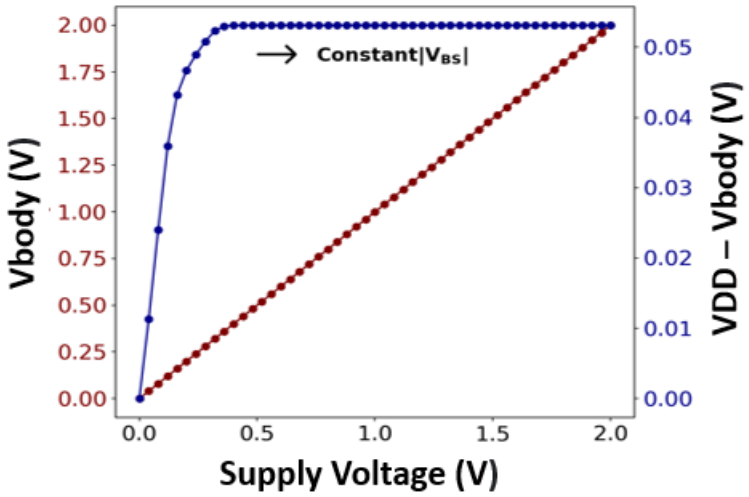


Figure 2.7 V_{body} tracks V_{DD} change and creates constant $|V_{BS}|$ for MP3

2.6 Proposed Temperature Compensation Technique

The key idea of the architecture is to generate temperature independent current reference by taking the ratio of compensated voltage (V_{comp}) and on-chip resistance R as shown in Eq. 2.1 By making the TC of V_{comp} equal to the TC of the resistance, I_{ref} can be made temperature independent. As MP3 and MP4 are the same type of MOSFET, the CTAT voltage is generated from the body bias effect on the V_{TH} of MP3. Voltage V_{SB} of a transistor changes its threshold voltage. If V_{SB}=0, i.e there is no substrate biasing, V_{TH0} is expressed as:

$$V_{TH0} = V_{FB} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \tag{2.13}$$

If a substrate voltage is applied to the transistor, threshold voltage is expressed as:

$$V_{TH} = V_{TH0} + \gamma[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \tag{2.14}$$

where γ is the body bias coefficient. Threshold voltage increases as V_{SB} increases. This is called body effect or back gate effect. From Eq. 2.6 and Eq. 2.14, I_{ref} can be expressed as:

$$I_{ref} = m\frac{\gamma[\sqrt{2\phi_F - \eta V_T ln\frac{K_2}{K_1}} - \sqrt{2\phi_F}] + \eta V_T ln\frac{I_{in}K_4}{I_{ref}K_3}}{R} \tag{2.15}$$

The term $2\phi_F - \eta V_T ln(K_2/K_1)$ in Eq. 2.12 generates a CTAT voltage, where K_2/K_1=$(W/L)_{MP2}$ /$(W/L)_{MP1}$ and the second term generates a PTAT voltage. Taking derivative of Eq. 2.15 with respect to temperature and equating it with zero, we come to a relation between the TC of on-chip resistance (α_R) and the aspect ratio of MOSFETs MP1-MP4. The TC of on-chip resistance can be written as shown in Eq. 2.16 and, after some mathematical derivations we arrive at Eq. 2.17.

$$\frac{1}{R_0}\frac{\mathrm{d}R}{\mathrm{d}T} = \alpha_R \tag{2.16}$$

$$\alpha_R = \frac{\gamma[2\frac{\mathrm{d}\phi_F}{\mathrm{d}T} - \frac{\eta K}{q}ln(\frac{K_2}{K_1}) - \frac{1}{2\sqrt{2\phi_F}}\frac{\mathrm{d}\phi_F}{\mathrm{d}T}] + \frac{\eta K}{q}ln(\frac{mK_4}{K_3})}{\gamma[\sqrt{2\phi_F - \eta V_T ln(\frac{K_2}{K_1})} - \sqrt{2\phi_F}] + \eta V_T ln(\frac{mK_4}{K_3})} \tag{2.17}$$

Where, γ denotes the body effect coefficient whose typical value lies in the range of 0.3 to 0.4 $V^{1/2}$ and ϕ_F is the Fermi potential of the MOSFET which is temperature dependent [11]. Temperature independence of I_{ref} can be achieved by proper choice of on-chip resistance and proper sizing of the aspect ratio of MOSFET MP1-MP4 such that TC of R becomes equal to RHS of Eq. 2.17. The process dependence of the on-chip resistance depends upon how R and α_R are related to process variation. Fig. 2.8 illustrates the value of R in various process corner (TT, FF, SS). The plot of I_{ref} at different process corners is shown in Fig. 2.9. The component parameters used in the proposed circuit is shown in Table 2.1.

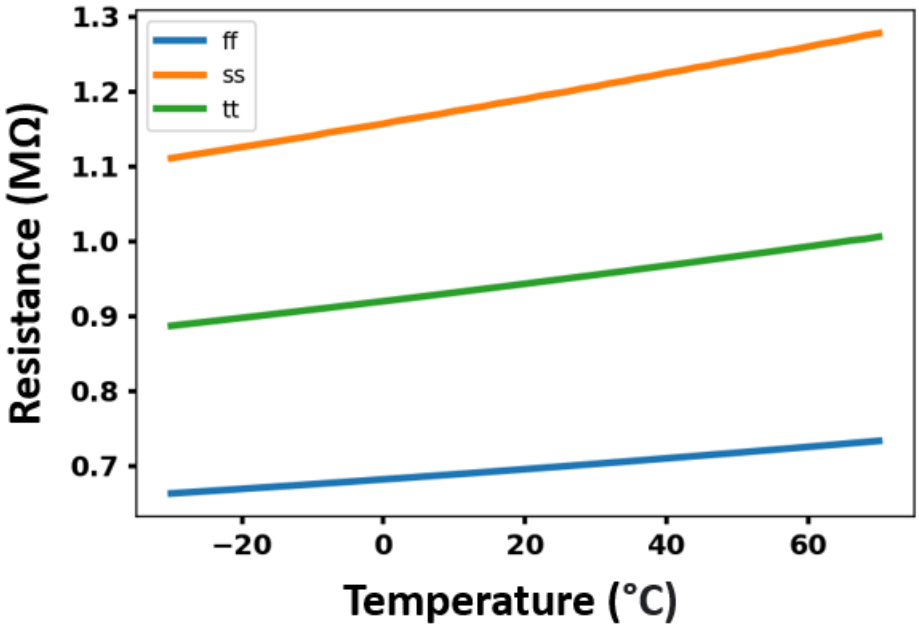


Figure 2.8 R at different process corners

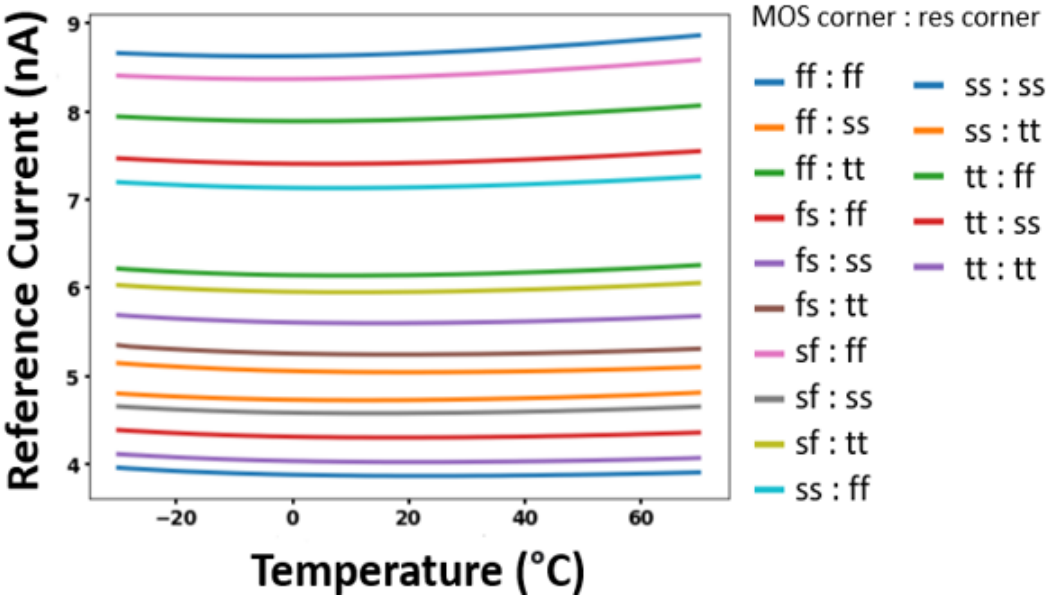


Figure 2.9 I_{ref} vs temperature at different corners

Table 2.1 Design Values

Device	**Width** (μm)	**Length** (μm)	**Multiplier**
MN1-MN3	1	10	50
MP1	1	10	16
MP2	1	10	60
MP3	1	10	15
MP4	1	10	27
M5-M8	0.5	10	3

2.7 Results and Discussion

The proposed current reference is designed in TSMC 180nm technology, and the simulation results are demonstrated. The resistor is implemented using a p-poly resistor. All MOSFETs operate in sub-threshold region. The circuit consumes only 9.5nW of power from a 0.55V supply. This current reference reduces the power in orders of 3 compared to the low power design [9] at typical conditions (minimum supply voltage and room temperature). A line sensitivity of 0.022%/V is achieved for a supply voltage range of 0.55V to 1.9V, as shown in Fig. 2.10. The variation of I_{ref} with respect to temperature is shown in Fig. 2.11. A TC of 162ppm/°C is achieved at typical corner for the temperature range of -30°C to 70°C. Fig. 2.12 shows the dependence of I_{ref} on supply and temperature variation.

In order to look into the effect of process variations on reference current and its TC, Monte-Carlo simulations are performed (Fig. 2.13) for 1000 samples. The reference current has a mean (μ) of 5.6nA and the standard deviation (σ) is 580.5pA. An average TC of 256.07ppm/°C and standard deviation (σ) of 109.1ppm/°C is noted. To prove the property of the circuit for ultra-low-power applications, Monte Carlo simulations is performed for power consumption on 1000 samples and the obtained plot with a mean (9.58nW) and standard deviation (996.2pW) is shown in Fig. 2.14. Fig. 2.15 shows the comparison of proposed and previous work in terms of TC and power consumption. Layout for the circuit is done and occupies an active area of 0.0326mm^2 as shown in Fig. 2.16. The proposed current reference is compared with the reported state of the art in Table 2.2. Although the proposed design achieves a larger TC compared to [1], [4], [12], it can be seen that the proposed current reference achieves the lowest supply voltage of 0.55V and lowest line sensitivity of 0.022%/V. All results are shown for post layout simulations.

2.8 Summary

Low power and low voltage CMOS current reference with a 0.55V supply and is herein presented. A peaking current source is proposed which cancels out the ratio of the compensated voltage and on-chip resistance by employing a CTAT voltage generator which exploits the threshold voltage dependence on the body to source voltage of the MOSFET, while consuming only 9.5nW of power and generating 5.6nA of reference current. The design enhances the performance of line regulation with the adopted PD-AMP which consumes only 0.62nA of current. The performance of the proposed circuit makes it suitable for biomedical applications that require low-supply voltage and power consumption.

While the viability of the proposed concept has been shown, for future work auto-trimming circuits can be designed for process independent current. As other applications, because of the competitive specifications of temperature coefficient, line sensitivity and power consumption, the proposed work can be used as an elementary circuit block for IoT applications.

Table 2.2 Performance summary and comparison with previous work

	[12]	**[4]**	**[1]**	**[7]**	**[9]*****	**This work**
Technology(nm)	180	180	180	180	180	**180**
Area(mm^2)	0.009	0.023*/0.123**	0.098	0.017	0.003	**0.032**
Min Voltage(V)	1.4	1*/1.2*	1.38	> 1.5	1.8	**0.55**
Power(W)	0.3μ	$1.4\mu^{*}/32.7\mu^{**}$	275.1n	1.02n	2.7μ	**9.5n**
Temperature Range(°C)	-55 - 125	0 - 100	-50 - 100	-40 - 120	-40 - 100	**-30 - 70**
I_{ref}(A)	50n	7.81μ	66n	35n	1.5μ	**5.6n**
I_{total}/I_{ref}	4.28	NA	3.0209	NA	1.14	**3.08**
TC (ppm/°C)	11.6	24.9*	67.04	282	571	**256.07**
Line Sensitivity(%/V)	0.05	0.13**	1.413	3	NA	**0.022**
Current Reference Trim	yes	no	yes	no	no	**no**

*core only,**with BGR,***weak inversion

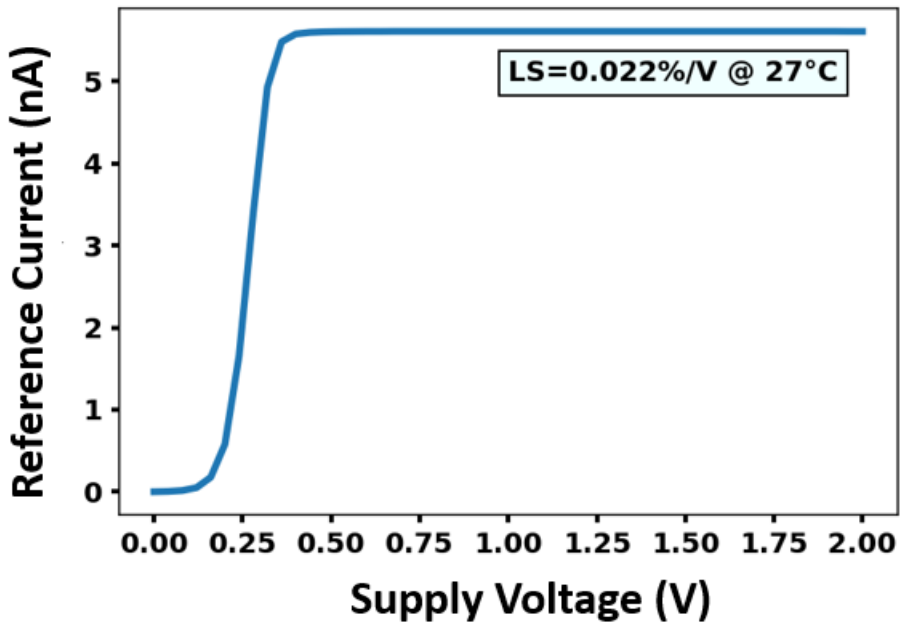


Figure 2.10 Influence of supply variations on I_{ref} @ TT corner

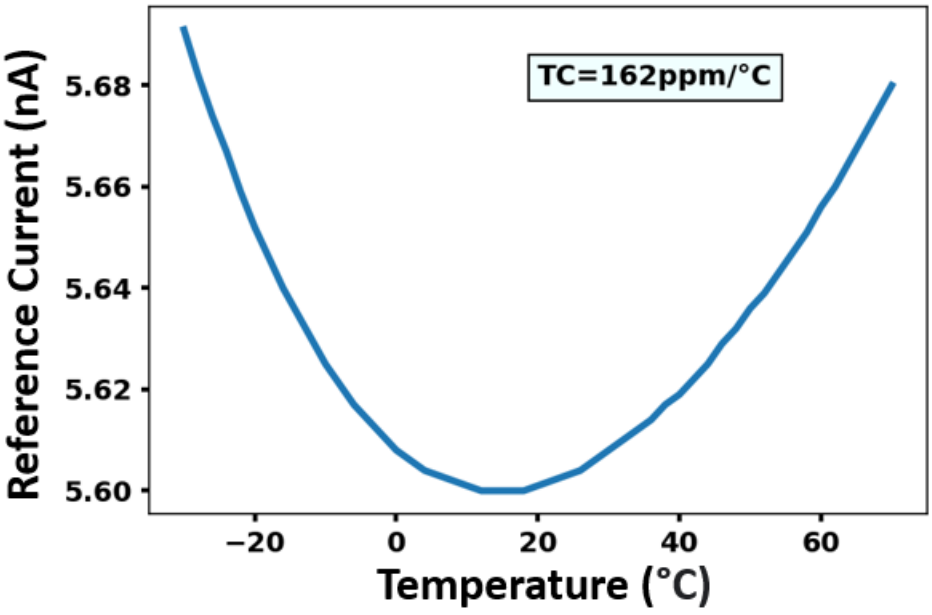


Figure 2.11 Influence of temperature variations on I_{ref}

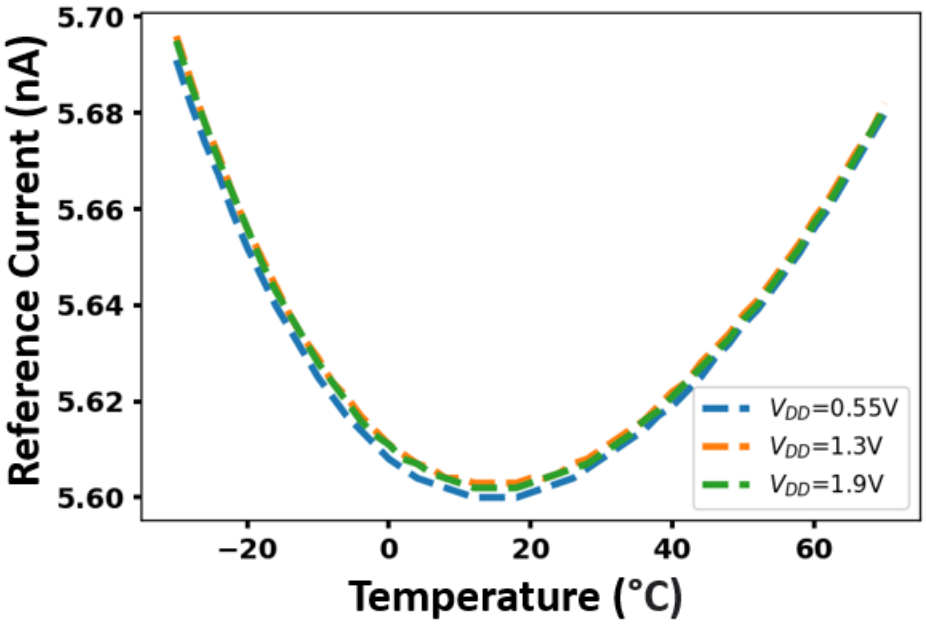


Figure 2.12 I_{ref} at different values of supply voltage

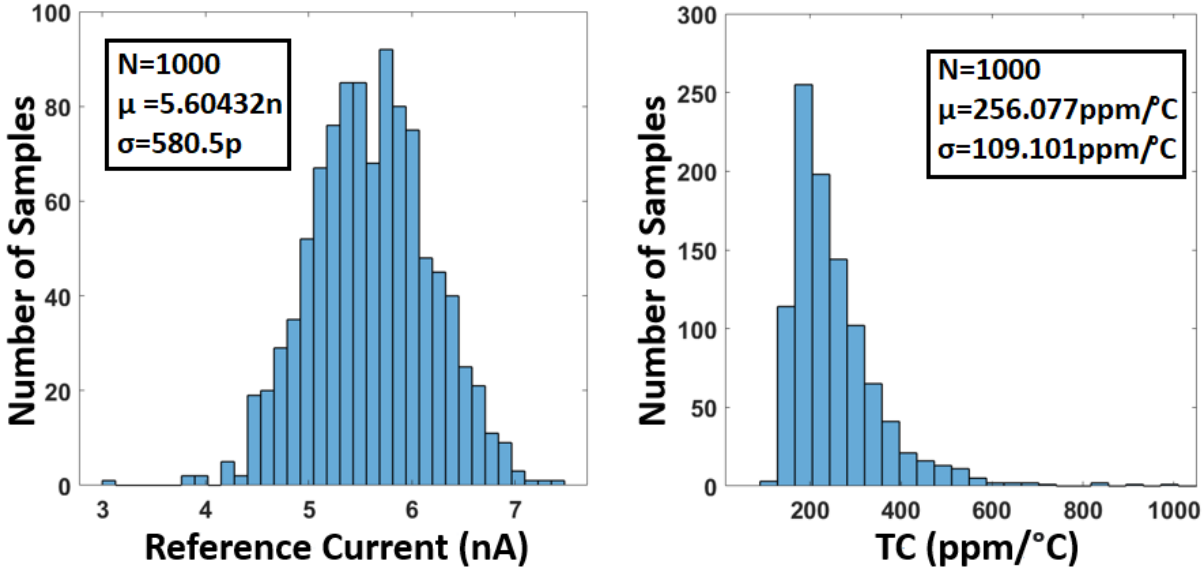


Figure 2.13 Monte Carlo for I_{ref} and TC

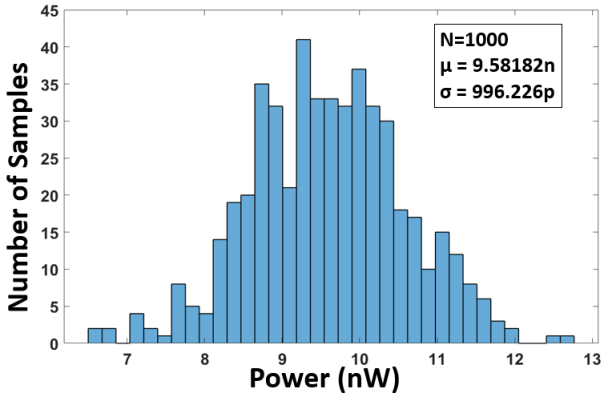


Figure 2.14 Monte Carlo simulation for power

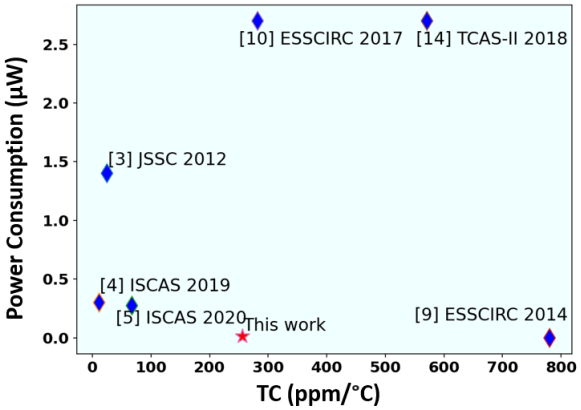


Figure 2.15 Comparison of proposed work with existing work

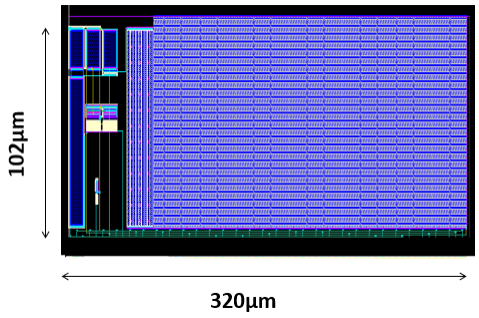


Figure 2.16 Layout of the proposed design

Chapter 3

Low Power Switched Capacitor Bandgap Voltage reference

3.1 Introduction

As low power enabled technologies are becoming more popular, specifications focusing advancement in wireless sensing systems for bio-implantable devices has opened up new challenges for miniaturization and power consumption reduction. Besides conventional applications, including the wristwatch, hearing aid, and pacemaker, new applications using low-power are appearing daily. For such ultra-low-power (ULP) systems, the voltage reference is an essential and fundamental part of system-on-chips (SoCs). A voltage reference generates a fixed voltage that is insensitive to process, voltage, and temperature (PVT) variation. Its application includes on-chip design, used to interface circuit blocks on a common IC; and off-chip design, used to interface other ICs within a system. The generated voltage needs to be stable and accurate to qualify as a good reference. As a voltage reference circuit, one of most common applications is to generate different levels of bias voltage for system function and provide voltage thresholds for detecting various events. The voltage regulator is often used as a power supply for other circuits. A low dropout regulator is a variation of the voltage regulator with a minimum input-output voltage drop, which preserves the maximum voltage headroom for subsequent circuits. This chapter places an emphasis on designing a bandgap voltage reference circuit based on switched capacitor network (SCN). Low power switched capacitor circuits are electrical circuits that use switched capacitors to perform various functions, such as filtering, amplification, and conversion, while consuming minimal power. These circuits use switching techniques to transfer charge between capacitors, rather than traditional linear techniques such as resistors and operational amplifiers. This allows for a significant reduction in power consumption, making them well suited for battery-powered or other low power applications. Some examples of low power switched capacitor circuits include switched capacitor filters, switched capacitor voltage converters, and switched capacitor power amplifiers. The goal of this effort is to design a bandgap reference working at low supply voltage and PVT invariant simultaneously. The rest of the chapter is broadly divided as follows: Section 3.2 emphasizes on literature survey done. Section 3.3 explains about types of bandgap references. The working of switched capacitor circuits is explained in section 3.4. Section 3.5 explains the proposed BGR architecture. The working of core

BGR circuit is explained in section 3.6. The clock generator circuit is explained in section 3.7. Finally section 3.8 presents the simulation results and conclusion is drawn in section 3.9.

3.2 Literature Survey

Conventional BGRs generate reference voltage with high PVT insensitivity but can hardly work for low supply voltage and low-power applications [13, 14, 15, 16, 17, 18]. Recently, CMOS-only reference circuits [19, 20, 21] are designed based on the MOSFET threshold voltage (V_{TH}). For example, [20] used curvature compensation technique to reduce the TC but operates at a supply of 1.45V. [21] reduced the supply voltage to 0.25V but consumes a power of 5.3μW. Also, V_{TH}-based references suffer from significant process variations without trimming circuit. To make BGR circuits suitable for ULP systems, leakage-based proportional-to-absolute-temperature (PTAT) voltage circuits [22, 23, 24] have been proposed. [22] reduced the power consumption to 29nW but occupied a large silicon area. [23] reduced the area and power consumption but suffered from settling behavior and stability issues due to leakage current. [24] reduced the power consumption to 19nW but resulted in a higher supply voltage (1.4V), high active area, and low PSRR (-42dB at 100Hz).

The SCN-based BGR [25, 26, 27, 28, 29, 30] is suitable for low-power applications when compared to conventional BGR. A switched capacitor voltage reference is a type of voltage reference circuit that uses a series of capacitors to maintain a constant output voltage. The circuit uses a switching mechanism to periodically transfer charge between the capacitors, allowing it to maintain a stable output voltage despite changes in input voltage or load. Switched capacitor voltage references are often used in power management and other applications where a stable voltage reference is required. In addition, SCN-based BGR significantly saves the required on-chip area by using capacitance of a few pF instead of large resistors. [25] proposed a 2x charge pump and a clock-generating circuit using a current-starved ring oscillator. However, the work consumes a power of 71nW for cascaded structure due to high leakage current. [26] employed the reverse bandgap concept to reduce the supply voltage to 0.75V but resulted in poor power consumption (170nW) and PSRR. [27] proposed a resistor-less PTAT voltage generator and low voltage current source, but the oscillator for the clock signal limit the total power consumption to 40nW. [28] proposed a curvature compensation scheme to extend the temperature range but at the cost of increased power consumption (83nW) and low untrimmed accuracy (3.2%). A similar analysis of clock generator circuits for SCN-based BGR has been proposed in [29, 30]. To overcome the limitations in [29], a dual PTAT clock topology is employed in [30], which also reduces the settling error of SCN. However, to generate a PTAT clock signal, an oscillator with PTAT current biasing is employed, which uses a resistor of 10MΩ, thereby increasing the on-chip area to 0.042mm^2. Considering the limitations of the previous state-of-the-art works, this work targets reducing power consumption by proposing a novel low-power SCN-based BGR circuit driven by low frequency (14.7kHz) clock signals to reduce the leakage current. PSRR determines the performance limit and is the circuit's ability to reject noise from power supply. A PSRR of -62.9dB at 100Hz and -74.2dB at 100kHz is achieved, which ensures noise

rejection in the operating frequency range. The proposed clock generating circuit uses a higher threshold device to reduce power consumption. The proposed ring oscillator (RO) reduces the power by 33% and 44% compared to the PTAT oscillator in [25] and [30] by generating a PTAT frequency clock signal which exploits the complementary-to-absolute-temperature (CTAT) resistance of a MOSFET biased in the sub-threshold region. The proposed design achieves a total power consumption of 18.5nW, which is 42.1% and 23% less compared to [25] and [30], respectively. Moreover, the circuit works from a supply voltage of 0.5V and generates a reference voltage of 577mV at room temperature. The design achieves a TC of 74.4ppm/°C over a temperature range of 0-80°C.

3.3 Continuous and Discrete time Bandgap References

The voltage reference is a type of circuit that generates a well-controlled voltage. The selection of a qualified reference needs to meet three criteria: universal, replicable, and practical. The continuous-time bandgap refers to a bandgap voltage reference whose output voltage is valid at all times. The output voltage of a common bandgap circuit is 1.2 V, by summing VBE of a single diode and a PTAT established by the VBE difference of two diodes. For applications requiring a higher bandgap voltage, the output of an integer multiple of 1.2 V can be achieved by applying amplifier gain. It is also possible to achieve a higher reference voltage with a voltage regulator. However, to get a bandgap voltage lower than 1.2-V, a sub-1 V bandgap architecture is needed. With a sub-1 V bandgap circuit, the output voltage can be lower than the predetermined bandgap voltage, or 1.2 V. Instead of summing in the voltage domain, the PTAT and CTAT voltages are converted into the current domain, summed together, and converted back to voltage. A simplified sub-1 V bandgap reference is shown in Fig. 3.1 [31].

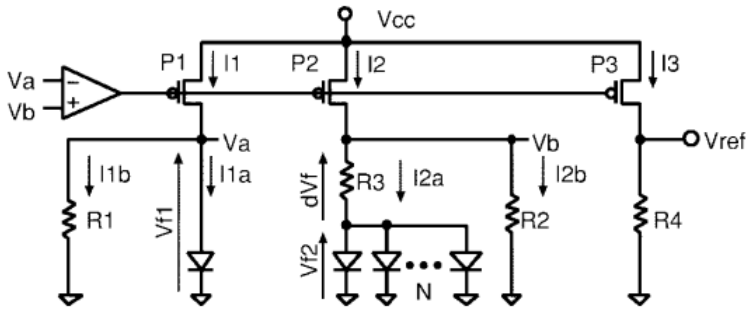


Figure 3.1 Current mode sub-1V Bandgap Reference

A discrete-time bandgap represents a different category of bandgap implementations as compared to the continuous-time bandgap reference circuit. A discrete-time bandgap establishes the bandgap voltage using a switched capacitor network. The generated output voltage is not continuous in time and is most often used in clocked systems. Another benefit of using a discrete-time bandgap is replacing resistors with capacitors which can generally lead to better component matching and hence, improved

yield. Switched capacitor-based designs are more tolerant to process variations as critical specifications of such circuits depend on capacitance ratios, which are better controlled than transconductances and resistors. Fig. 3.2 shows a switched capacitor cirucit developed by Ulmer et al [32].

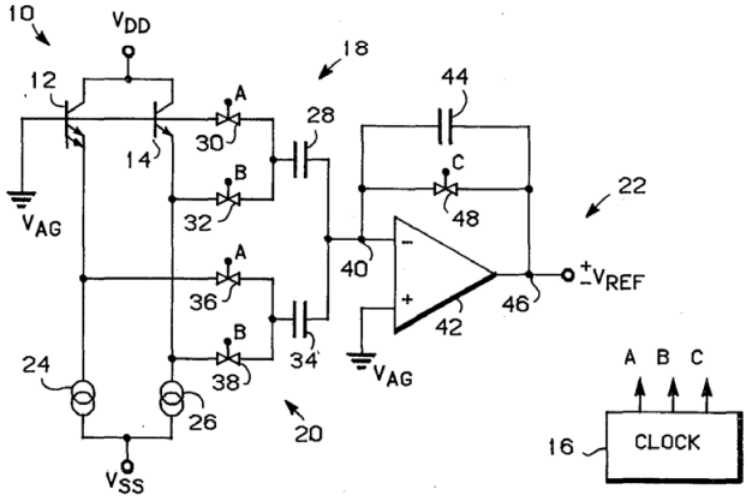


Figure 3.2 Switched Capacitor voltage reference

3.4 Switched capacitor circuits

A switched capacitor is a circuit element that uses switches to transfer charge in and out of a capacitor. This is typically done using non-overlapping signals to control the switches, which ensures that all switches are open for a short period of time during the switching transitions. This type of circuit element is commonly used in discrete time signal processing systems.

3.4.1 Concept of charge transfer

From Fig. 3.3, q =CV gives the value of charge stored in a capacitor where V is the voltage. Fig. 3.3 shows two capacitors, C1 and C2, charged to voltages V1 and V2, respectively. The total charge on the parallel combination of the two capacitors is:

$$Q_{total} = C1V1 + C2V2 \tag{3.1}$$

According to law of conservation of charge, this charge is redistributed between the capacitors, so the final voltage, V_{total}, across the parallel combination of capacitor is equal to:

$$V_{total} = \frac{Q_{total}}{(C1 + C2)} = \frac{(C1.V1 + C2.V2)}{(C1 + C2)}. \tag{3.2}$$

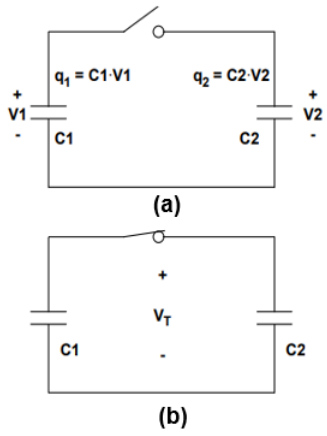


Figure 3.3 Charge redistribution between capacitors

3.4.2 Switched capacitors voltage doubler

Fig. 3.4 shows the basic topology of 1:2 switched capacitor voltage converter(doubler). ϕ_1 and ϕ_2 are non-overlapping clock signals normally occupying half of the clock cycle. In both cases, during ϕ_1, C_{fly} charges up to V_{in}, which makes it contain a total charge of $C_{fly} \times V_{in}$. The charge stored in the flying capacitors remains unchanged during the transition from phase 1 to phase 2, which makes V_{out}= 2 V_{in}.

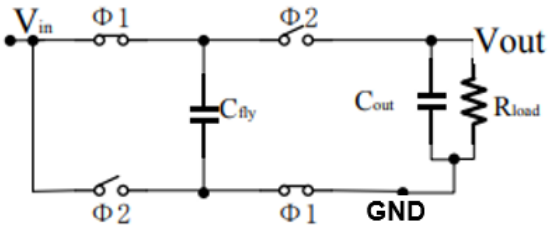
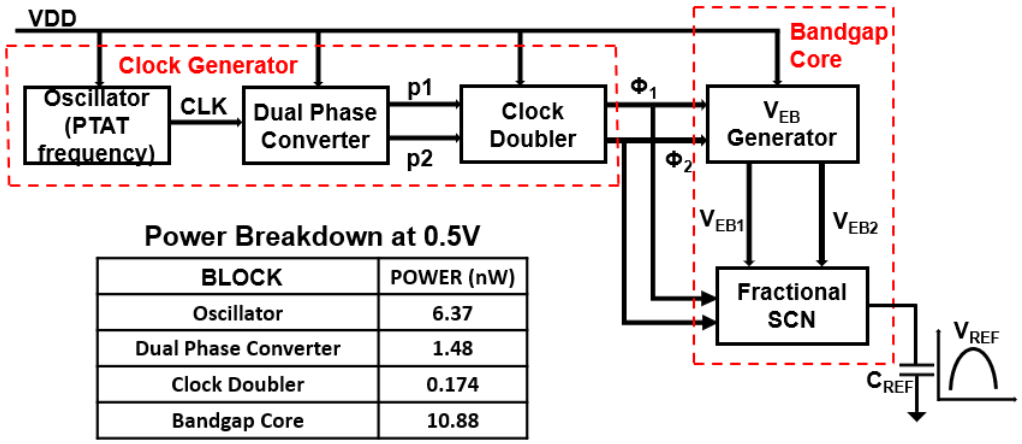


Figure 3.4 Basic architecture of switched capacitor circuit

3.5 Proposed BGR Architecture

The architecture of the proposed design is demonstrated in Fig. 3.5. An oscillator with PTAT frequency is employed which generates a clock signal CLK. A low-power dual phase converter circuit is proposed to get the non-overlapping clock signals p1 and p2. The clock doubler circuit doubles the swing of the output clock to 2VDD which drives the V_{EB} generator. An additional resistor and OPAMP are used in [29] for PTAT current biasing of BJT, which takes more area and power. To overcome these limitations, a 2x charge pump is directly employed to generate V_{EB1} and V_{EB2}. A fractional SCN

is used to generate coefficients of V_{EB} and $\triangle V_{EB}$ which together generate temperature compensated V_{REF} across C_{REF}.



Power Breakdown at 0.5V

BLOCK	POWER (nW)
Oscillator	6.37
Dual Phase Converter	1.48
Clock Doubler	0.174
Bandgap Core	10.88

Figure 3.5 Architecture of proposed BGR circuit

Specifically, the contributions of this work are:
1) The RO generates slow clock signals of frequency 14.7kHz, which drives the core BGR circuit, thereby reducing the power to 10.88nW. The slow clock signals reduce the leakage-induced errors in the SCN [30], resulting in total power consumption of 18.5nW.
2) The PTAT clock signal is generated by exploiting the CTAT resistance of MOSFET biased in sub-threshold region instead of using a PTAT current biasing circuit [25], [29], [30].
3) The proposed clock generating circuit uses high threshold voltage (HVT) device to reduce MOSFET leakage current. Fig. 3.6 shows the comparison of TC, power, and PSRR of the proposed work with prior works.

3.5.1 MOSFET leakage current dependency

The associated switches can cause charge leakage due to the MOSFET leakage current. The sub-threshold leakage current of the MOS transistor is well defined in [28] and is expressed as:

$$I_{leakage} = I_S(\frac{W}{L})exp(\frac{V_{GS} - V_{TH}}{\eta V_T})[1 - exp(\frac{-V_{DS}}{V_T})] \tag{3.3}$$

where, $I_S = \mu_n(\eta - 1)C_{ox}V_T^2$; (W/L) is the ratio of transistor's width and length, V_{TH} is the threshold voltage of the transistor, $V_T = KT/q$ is the thermal voltage which has a linear temperature dependency, μ_n is mobility and η is the sub-threshold slope factor. From Eq. 3.3, leakage current is a function of the threshold voltage. Based on this idea, the proposed work uses HVT devices in clock generating circuit to reduce the leakage current. Fig. 3.7 shows the simulated leakage current of different switches at 27°C and TT corner. The current consumption of the clock generating circuit is

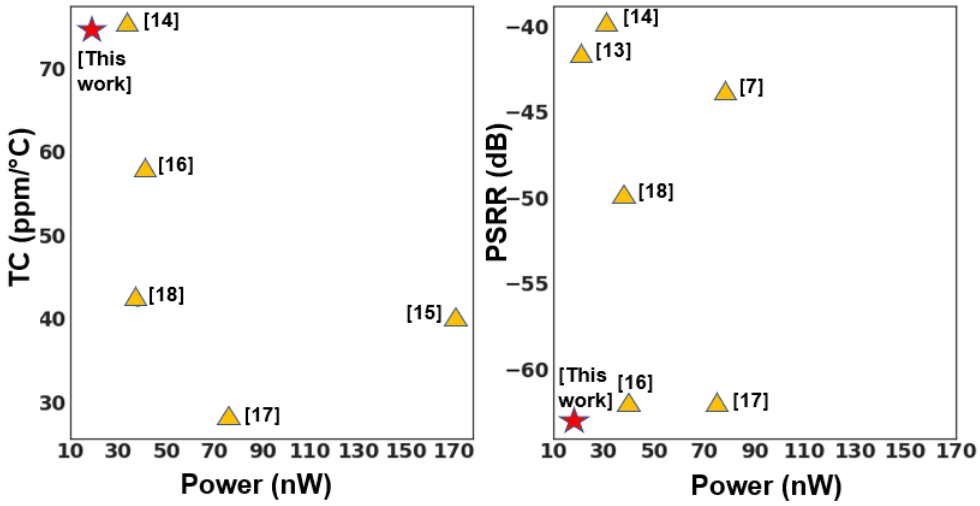


Figure 3.6 Comparison of proposed work with previous works

reduced by 37% when compared with [25] and the overall power consumption of the proposed circuit is reduced by 42% and 23% when compared to [25], [30] respectively.

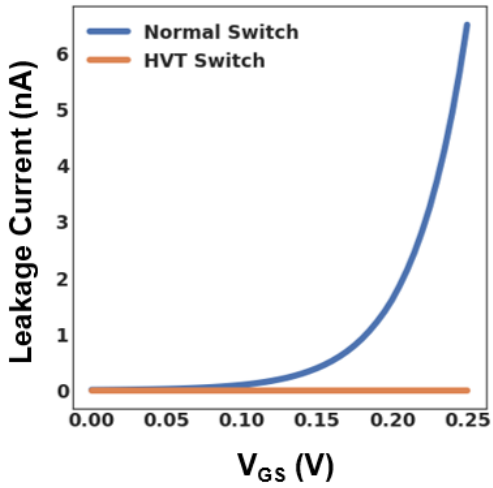


Figure 3.7 Leakage current in different switches

3.6 Core BGR Circuit

The core BGR circuit reported in [25] is adopted in this paper as shown in Fig. 3.8 and is optimized according to our system requirement. The PTAT clock signals ϕ_1 and ϕ_2 drives the 2x charge pump, which generates CTAT voltage V_{EB1} (Fig. 3.9a) and V_{EB2} (Fig. 3.9b) across C_{L1} and C_{L2}.

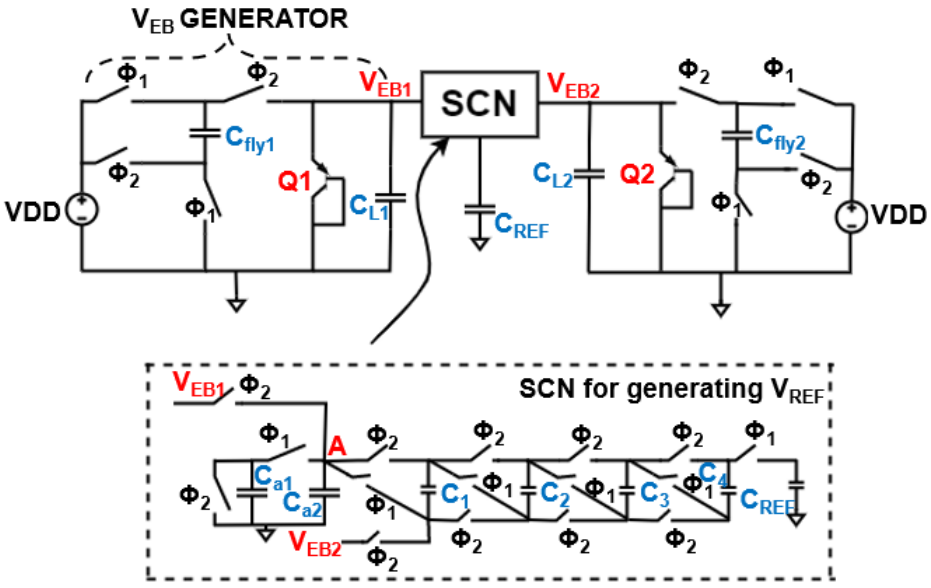


Figure 3.8 Schematic of core BGR circuit

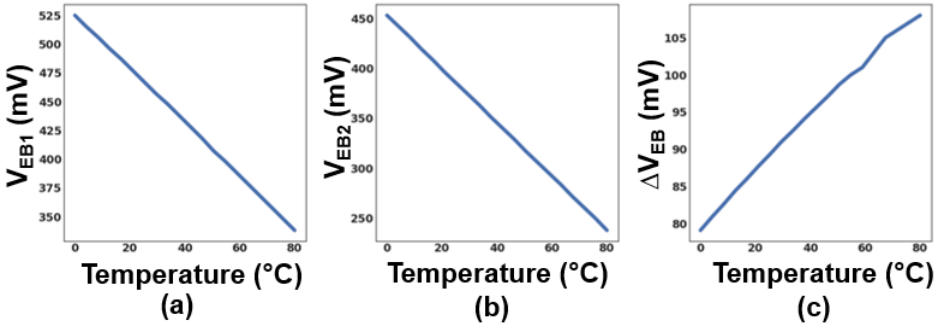


Figure 3.9 (a)Variation of V_{EB1} with temperature (b) Variation of V_{EB2} with temperature (c) Variation of ΔV_{EB} with temperature

The proposed voltage divider SCN generates a fractional CTAT coefficient α for CTAT voltage V_{EB1} and scales the PTAT voltage ($\triangle V_{EB}$). In phase ϕ_2, V_{EB1} and V_{EB2} is sampled by the SCN and the difference $\triangle V_{EB}$ (Fig. 3.9c) is stored across the capacitor $C1 - C4$. In phase ϕ_1, the voltage at node A is α times V_{EB1}, where α is $C_{a1}/(C_{a1} + C_{a2})$. The difference $V_{EB1} - V_{EB2}$ stored in $C1 - C4$ and the voltage at node A together sums up to form temperature-independent reference voltage, which is stored across capacitor C_{REF} as shown in Eq. 3.4.

$$V_{REF} = \frac{V_{EB1}C_{a1}}{C_{a1} + C_{a2}} + 4\triangle V_{EB} \tag{3.4}$$

Slow PTAT clock signals is used to drive the core BGR reducing the power consumption to 10.88nW which is 45% less than the work reported in [25]. Previously mentioned state-of-the-art works use MIM capacitors in their proposed design, but due to the high thickness of oxide between metal layers, the capacitance per unit area is smaller [33]. The proposed design uses MOS capacitors, reducing the area by 35.7% compared to [30] and 47.7% compared to [29]. The capacitor values are selected such that temperature-independent V_{REF} is achieved. The switches in the SCN are designed with a minimum width to reduce the leakage current, which also helps to reduce power consumption.

3.7 PTAT frequency clock generator

Fig. 3.10 shows the circuit configuration of the clock generator, which consists of a ring oscillator (RO), a low-power single-to-dual phase clock converter, and a clock doubler circuit. The design works from a supply of 0.5V. A PTAT clock signal of frequency 14.7KHz is generated to bias the core BGR to reduce the settling error problem and leakage-induced errors [30]. As shown in Fig. 3.10, the proposed architecture of the RO exploits the CTAT resistance of a MOSFET biased in the sub-threshold region to generate a PTAT frequency. The proposed design saves power compared to the current starved RO as proposed in [25], [30]. The frequency of oscillations can be expressed as shown in Eq. 3.5

$$f = \frac{1}{2N\triangle t} \tag{3.5}$$

where N is the number of stages and $\triangle t$ is the propagation delay of the inverter, which is equal to the RC delay offered by the inverter. Resistance of a MOSFET in sub-threshold region is expressed as shown in Eq. 3.6.

$$R_{sub\_th} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(\eta - 1)V_T exp(\frac{V_{GS}-V_{TH}}{\eta V_T})exp(\frac{-V_{DS}}{V_T})} \tag{3.6}$$

, where there are three temperature-dependent terms. The term $\mu_n V_T$ makes a small CTAT and $exp(\frac{-V_{DS}}{V_T})$ gives a dominating PTAT term. The numerator and denominator of the term $exp(\frac{V_{GS}-V_{TH}}{\eta V_T})$ varies linearly with temperature making it temperature-independent. Therefore, we get a PTAT frequency of the

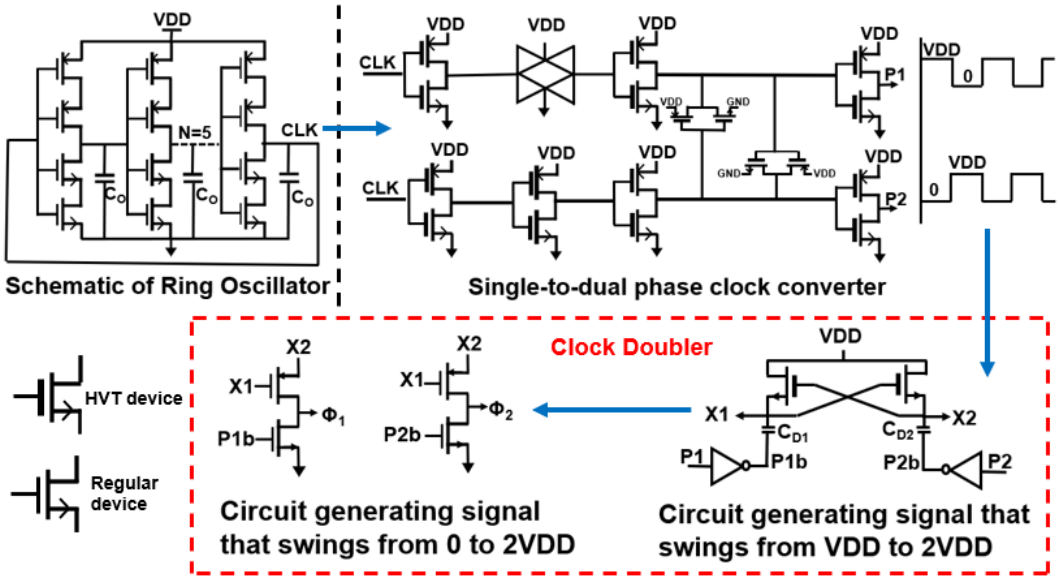


Figure 3.10 Schematic of proposed clock generating circuit

clock signal as shown in Fig. 3.11. The clock signal passes through the proposed low-power single-to-dual phase clock converter, which consists of a transmission gate and back-to-back inverters to obtain sharp rising and falling edge and non-overlapping phase of P1 and P2. The structure of the clock doubler includes a cross-coupled switched-capacitor circuit to generate a signal which swings from VDD to 2VDD. The circuit generating $\phi 1$ and $\phi 2$ which swings from 0 to 2VDD is similar to [25], and is optimized according to our design.

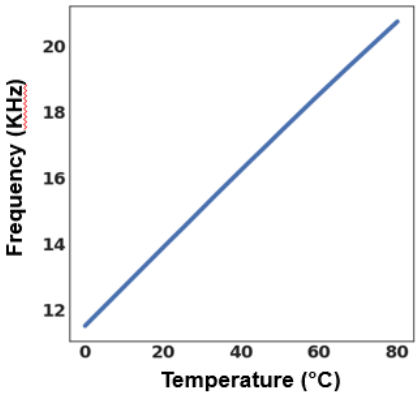


Figure 3.11 Variation of frequency of clock signal with temperature

3.8 Simulation Results

The proposed design is implemented in 180nm CMOS process and occupies a chip area of $0.027mm^2$ (Fig. 3.12). The SCN-based BGR works from a supply voltage of 0.5V. Fig. 3.13 shows the temperature variation of V_{REF}. A TC of 74.5ppm/°C is achieved over a temperature range of 0 - 80°C. The output voltage of the BGR achieves a $3\sigma/\mu$ variation of 2.6% across the process for 500 samples which is demonstrated in Fig. 3.14. Fig. 3.15a demonstrates the settling time of 2.6ms with a 2% tolerance band. The PSRR achieved is -62.9dB at 100Hz, and better than -40dB over the full frequency range as shown in Fig. 3.15b. Fig. 3.16a shows the current consumption with temperature. Fig. 3.16b shows the BGR power consumption of 18.5nW at 0.5V supply which is the lowest among the previous state-of-the-art works. Fig. 3.17a shows the power consumption of the BGR with temperature variations. Monte Carlo simulations for power consumption on 500 samples is performed, and the plot is shown in Fig. 3.17b. Table in Fig. 3.5 shows the power consumption of each block of the proposed circuit. The power consumed by the BGR core is 10.8nW which is 45% less compared to [25]. Table 3.1 summarises the performance compared to previous works. The area occupied is smallest compared with the previous works except [25]. Compared with [26, 27, 28, 29], the proposed work achieves a better $3\sigma/\mu$ variation before trimming. Also, it shows that the BGR consumes the lowest power of 18.5nW and similar TC compared with [25].

3.9 Conclusion

This paper presents a low-power SCN-based BGR suitable for biomedical applications. The proposed design demonstrates improved power consumption by employing a low-power novel clock generator circuit and driving the core BGR with slow PTAT clock signals. Biomedical signals has low frequency and voltage attribute, which is satisfied by the proposed work. We also explored the CTAT resistance of MOSFET to generate a PTAT clock signal. This work provides the lowest power consumption and on-chip area among the previous works, thereby contributing towards a new solution for low power and miniaturized wireless sensing systems.

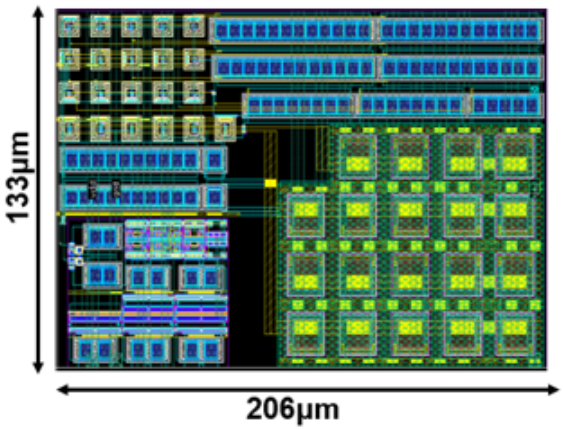


Figure 3.12 Layout of the proposed design

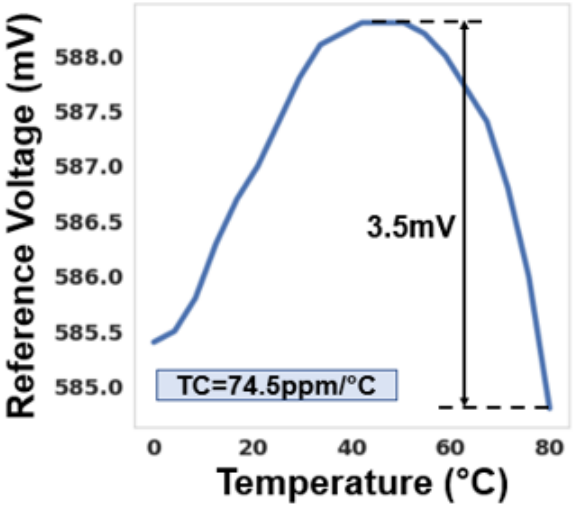


Figure 3.13 Variation of V_{ref}

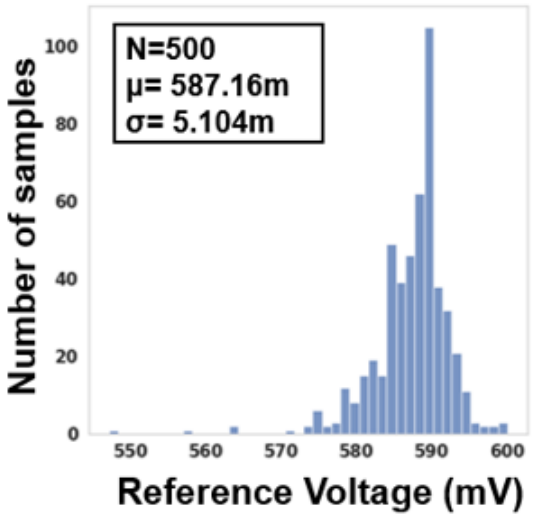


Figure 3.14 Monte Carlo simulation for V_{ref}

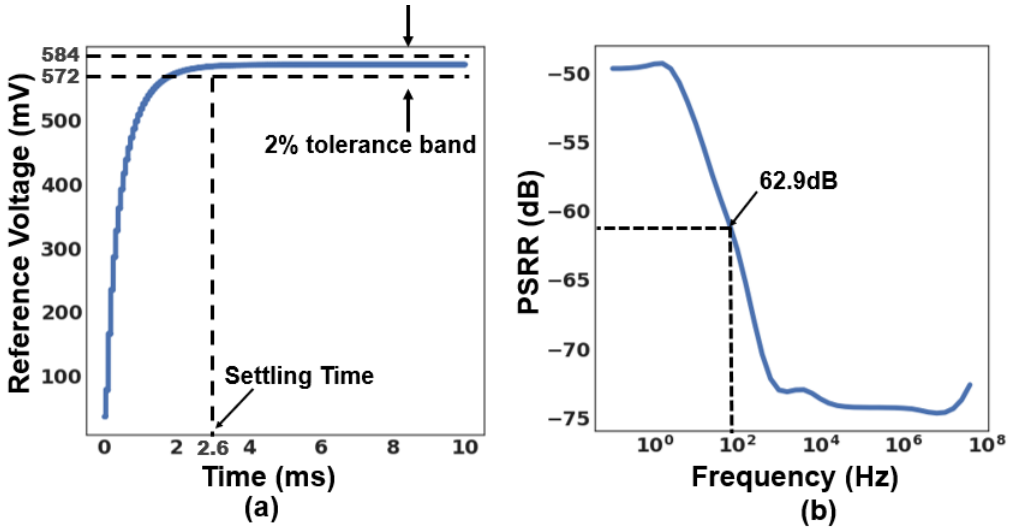


Figure 3.15 (a) Settling time of BGR (b) Plot of PSRR

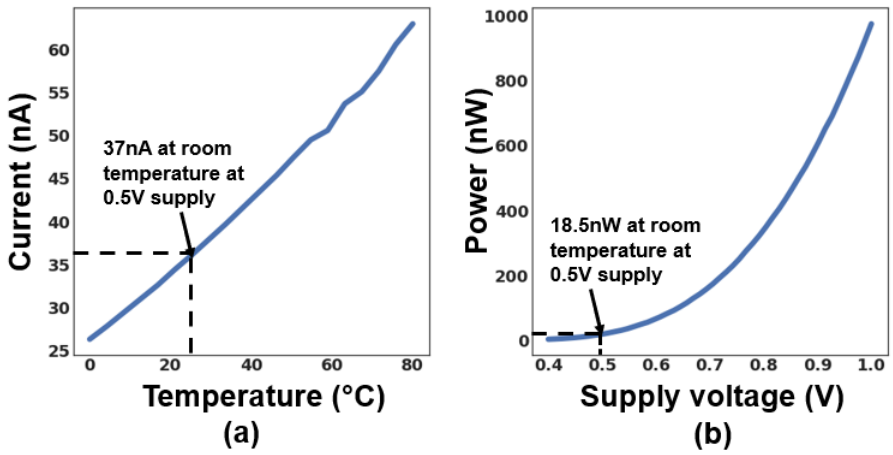


Figure 3.16 (a) Current consumption of BGR over temperature (b) Power consumption of BGR over supply

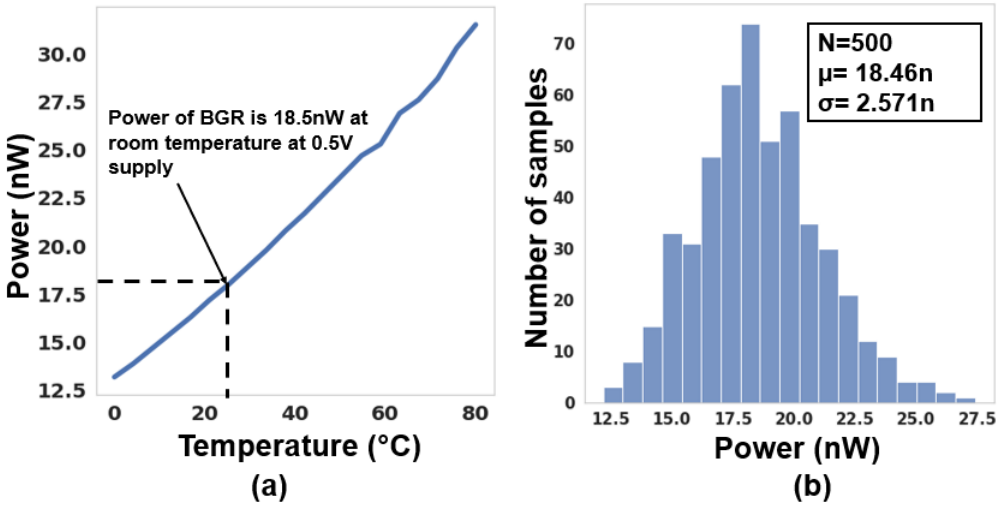


Figure 3.17 (a) Variation of power consumption of BGR with temperature (b) Monte carlo simulation for power

Table 3.1 COMPARISON OF BGR METRICS WITH PREVIOUS STATE-OF-THE-ART WORKS

	[7]	[11]	[14]	[15]	[16]	[17]	[18]	[19]	**This work**
Technology(nm)	180	350	130	130	180	180	65	65	**180**
Area(mm^2)	0.11	0.48	0.026	0.07	0.058	0.061	0.0522	0.042	**0.027**
Min Voltage(V)	0.9	1.4	0.5	0.75	0.5	0.55	0.5	0.5	**0.5**
Reference voltage (V)	0.411	1.17	0.502	0.184	0.24	0.46	0.49	0.50	**0.57**
Power(nW)	85	28.7	32	170	40	83	38	24	**18.5**
Temperature Range(°C)	-40-125	-10-100	0-80	-20-85	-40-80	-45-120	-40-120	-40-120	**0-80**
TC (ppm/°C)	33.7	12.75	75	40	58	28	42	32	**74.5**
PSRR (dB) @ 100Hz	-44	NA	-40 @DC	NA	-62	-62	-50 @DC	-50 @DC	**-62.9**
Untrimmed accuracy ($3\sigma/\mu$)[%]	1.17	0.6	2	3	3	3.2	3.08	1.37	**2.6**

Chapter 4

On-Chip VNA Design for Biomolecule Detection

4.1 Introduction

Over a few decades bio-molecule sensing technique using radio and microwaves has been proposed and utilized [34, 35, 36, 37, 38]. Interaction of high frequency signals with matter is a crucial feature of everyday lives. Electromagnetic interactions with matter such as person's body fluid has provided a means of biological analysis on macroscopic to microscopic range. Electromagnetic techniques have primarily focused on optical and infrared analysis with radio frequency (RF), microwave and terahertz frequencies. Consequently, discoveries such as the strong contrast in dielectric permittivities of biomolecules has lead to the growing desire in research in scientific field labelled as biosensing. The dielectric response to Radio waves of many polar liquids such as water, ethanol and acetone varies according to the strength of molecular dipoles and the density of dipole moments. The field of sensing and characterization of an unknown sample is an imperative area of biology [39, 40, 41] and non-destructive sensing using RF and microwave frequency is an effective technique. There are different RF sensing techniques available which are categorised under resonant and non-resonant methods [42, 43]. Among the resonant sensors, the characterization of biomolecule can be performed using rectangular waveguides, cavity resonantors or planar resonator sensors [44, 45, 46]. Planar resonators are prefered over cavity resonantors due to its low cost, easy fabrication and integration. Among different planar resonators, IDC [47] are easy to fabricate and provide a higher amount of sensitivity. Fig. 4.1 shows different types of biosensors used. The dielectric property of the biosensor will change on changing the DUT, resulting a capacitance change at the output of IDC. With change in the capacitance, the resonant frequency of the biosensor will vary which will produce a peak shift. This chapter proposes a fully integrated On-Chip CMOS VNA (Vector Network Analyser) designed in 65nm CMOS technology to detect the biomolecule for cell investigation, medical diagnosis and treatment. Additionally, biosensors with CMOS technology have been investigated for effective bio-information analysis since they have the potential to contribute to portable, inexpensive, label-free and minimally invasive medicine [48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58].

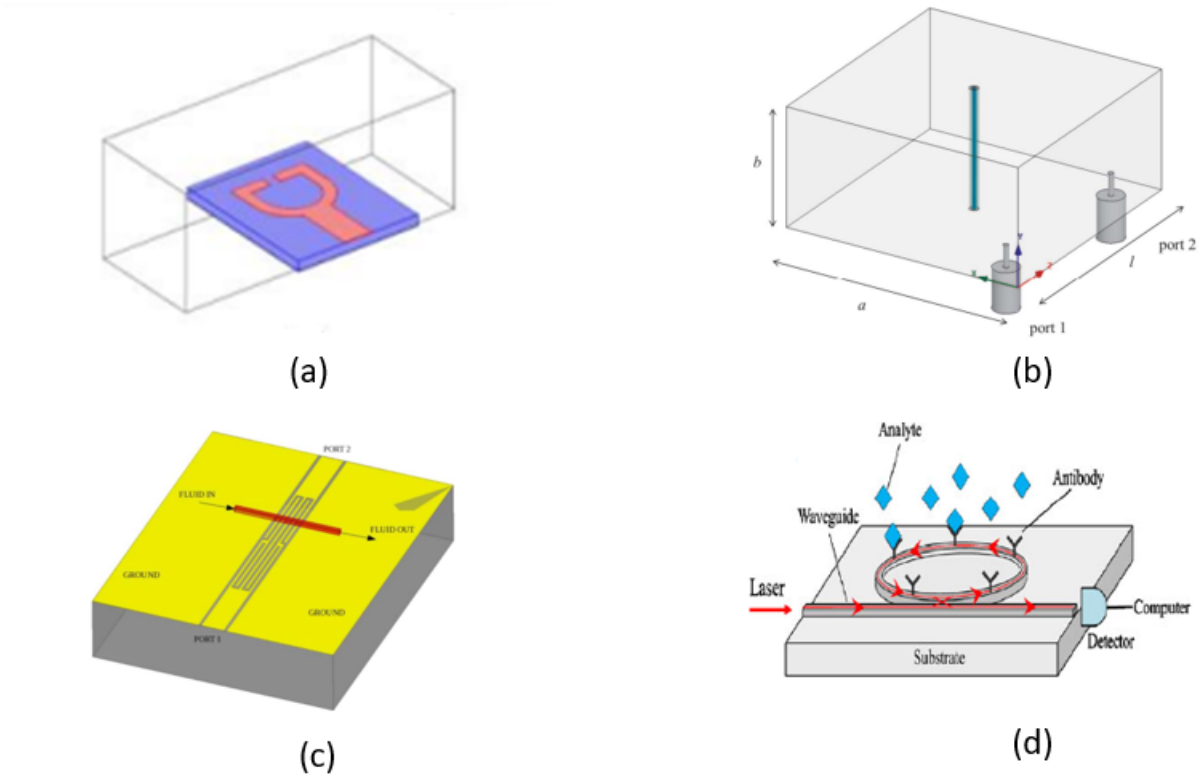


Figure 4.1 (a) CAD of U-shape sensor structure [56] (b) A rectangular waveguide cavity [44] (c) RF coplanar resonator with a microfluid on the top [57] (d) Ring resonantor biosensor using laser [58]

4.2 Working of IDC sensor

Interdigitated Capacitor (IDC) has interdigitated finger-like electrodes as two port of the capacitor as shown in Fig. 4.2. The DUT (Design under Test)/ biomolecule will be placed on this sensor. The sensing mechanism of this biosensor is same as capacitive sensors. The dielectric property of the biosensor will

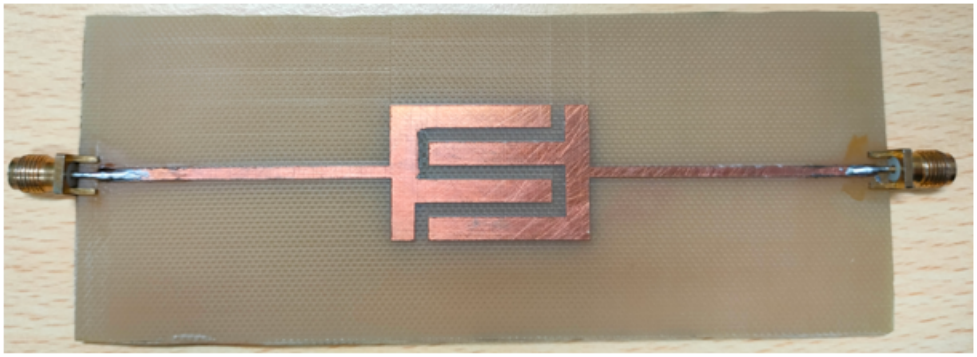


Figure 4.2 Top view of IDC

change on changing the DUT, resulting a capacitance change at the output of IDC. One major reason to choose IDC rather than parallel capacitor is ease of fabrication. It is easier to fabricate an IDC than a parallel capacitor using microelectronics fabrication techniques. Resonators and fingers of IDC are covered with an insulator layer to avoid direct contact of metal and the unknown sample, which may change sample properties or cause corrosion and oxidation of resonator. The inductance of biosensor is beacuse of resonantor length. The resonator can be modelled as an RLC series network whose R_{IDC} and L_{IDC} is fixed and the capacitance varies with variable DUT. From designed value of L_{IDC} and desired resonance frequency ($f_{resonance}$), C_{IDC} can be calculated as

$$f_{resonance} = \frac{1}{2\pi\sqrt{L_{IDC}C_{IDC}}} \tag{4.1}$$

The inductance of the biosensor can be calculated using the expression

$$L_{IDC} = 2 \times 10^{-4} \times l \times (ln(\frac{l}{w+t}) + 1.193 + 0.2235(\frac{w+t}{l})) \tag{4.2}$$

where w is the width and t is the thickness of the resonator. Length of resonator is useful in deciding resonant frequency, whereas width of resonator is used to decide quality factor. For better quality factor, bandwidth of sensor should be minimum for desired resonant frequency. With change in the capacitance as the DUT varies, the resonant frequency of the biosensor will vary.

4.3 Concept of On-Chip VNA

As explained in the previous section, a fully integrated on-chip VNA (Vector Network Analyser) is used for biomolecule detection. The on-chip VNA is used to detect the peak shift of the biosensor

by varying the capacitance of the DUT by using the concept of s-parameter which is explained in the next section. The biosensor might not be practical in medicinal applications because its measurement requires an area-consuming and costly external vector network analyzer (VNA) of signal processing equipment. The VNA is designed to measure vector scattering parameters, i.e., the complex reflection coefficient, of a device under test (DUT) connected at its test port, without disturbing the waves at that port. The On-chip VNA works from a frequency range of 0.5GHz to 2GHz. When an input signal in the frequency range of 0.5GHz to 2GHz is applied, the phase and amplitude of the output signal will vary depending on the DUT's property. This is because dielectrics absorb microwave when a high frequency wave penetrates the target, causing attenuation based on their impedance. In other words, characteristics of the dielectrics can be estimated from the variations in signals flowing through the target. In signal processing, a transmission loss named $|S21|$ can be extracted from amplitudes and phases of output signals on the on-chip VNA using CMOS technology. When an input signal with varying frequency is hitting the biomolecule, at a given time, the frequency of the input signal matches with the resonant frequency of the DUT, there will be ideally no reflections from the DUT hence the $|S21|$ will be at the lowest point giving us the peak at the resonant frequency. In summary, the design can identify the DUT according to the S-parameter $|S21|$ extracted by the on-chip VNA at frequency range of 0.5GHz to 2GHz The block diagram of the proposed design of on-chip VNA is shown in Fig. 4.3.

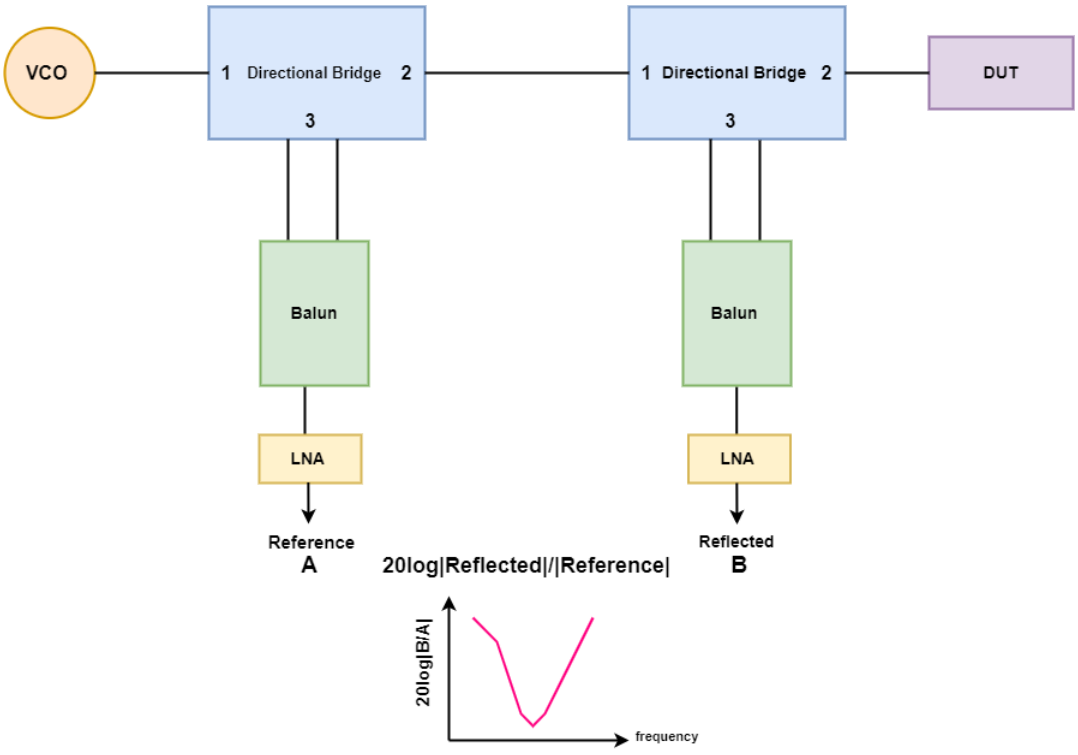


Figure 4.3 Architecture of on-chip VNA

The on-chip VNA comprises of directional bridge for signal separation, voltage controlled oscillator (VCO) for generating varying frequency input signal, and an LNA for amplification of signal. When an input signal with the variable frequency f_{in} is applied to the biosensor circuit, the first directional bridge is configured to distinguish a reference wave flowing to the first LNA from the incident wave. After the incident signal transmits through the first directional bridge, a part of the wave might be reflected from the DUT corresponding to the biomolecule dielectric property. The reflected signal from the second directional bridge flows through the second LNA for amplification. The $|S21|$ of the DUT can be expressed in simple terms as:

$$|S21| = 20log\frac{|Reflected|\angle Reflected}{|Reference|\angle Reference} \tag{4.3}$$

When the input frequency matches with the resonant frequency of the DUT, there are minimal reflections from the DUT and there is attenuation of the reflected signal making $|S21|$ at resonant frequency minimum. Hence, we get a peak at the resonant frequency of DUT. Different DUT's will have peak at different values of frequency and hence from the information of resonant frequency we can identify the biomolecule/DUT used.

4.3.1 Directional Bridge

Directional bridge are used in RF circuits which is used to monitor reflected and transmitted signals. A directional bridge operates by sending a RF signal through the reference arm of the bridge and measuring the resulting voltage and current at the output. The voltage-to-current ratio at the output is compared to the known impedance of the reference arm to calculate the unknown impedance of the device under test. The directional feature of the bridge enables it to differentiate between the forward and reflected waves in a transmission line, which allows it to accurately measure the impedance even in the presence of reflections. There are different types of directional bridges, such as the Slotted Line, Double-Ridged Guide, and Waveguide Bridges, each with its own unique characteristics and uses. Some directional bridges are designed for use at a specific frequency range, while others can be used across a wide range of frequencies. Fig. 4.4 shows the uni-directional bridge with a resistive load R_L at the output. The directional bridge has 3 ports. An input sinusoidal signal is given to PORT 1. The inputs form PORT 1 and node A goes into a black box which has certain gain. The black box works as a differential to single signal converter. The currents going inside the black box should ideally be zero. The output of the black box is PORT 3. Let us assume that $R_S = R_L = R$. Let us consider that an input of V volt amplitude is coming at PORT 1. The total impedance seen from PORT1 is $(R||11R) + 0.1R$ which is approximately 50 Ω. So voltage drop at PORT 1 is V/2. Similarly voltage drop at PORT 2 is:

$$V_{PORT2} = \frac{\frac{V}{2}\frac{11}{12}R}{1.01R} = 0.907V/2 \tag{4.4}$$

Voltage at node A will be approximately 0.49V. The difference of the two signals at PORT1 and node A gets multiplied with some amplification factor. This signal is named as reference signal coming from

PORT 3. Now if we apply an input signal at PORT 2, the voltages at PORT 1 and node A is (10/11)V. So there is no signal at PORT 3 and hence the reflected signal coming from the load gets isolated. The directional bridge proposed in this chapter, consists of two unidirectional bridge as shown in Fig. 4.5. The DUT used in the VNA is a series RLC circuit which is connected as the load. When an input signal form PORT 1 of the first bridge, passes through the DUT, it gets reflected from PORT 1 of second bridge. The reflected signal gets separated from the incident signal as the second bridge is connected in a reverse direction. The PORT 2 of the second bridge acts as the isolation port between the reflected and reference signal. Now, when an input signal having a frequency equal to the resonant frequency of the DUT, hits PORT 1 of the second bridge, there will be ideally zero reflections and the amplitude of reflected signal will be very low. On calculating $20log|Reflected|/|Reference|$, we will get a peak at resonant frequency. On varying the capacitor value, the resonant frequency of the DUT changes which is responsible for peak shift. Fig. 4.6 shows the reference and the reflected wave at resonant frequency of 1GHz for a capacitor value of 25pF. The peak shift with varying capacitors values for an input frequency range of 0.5GHz to 2GHz is shown in Fig. 4.7.

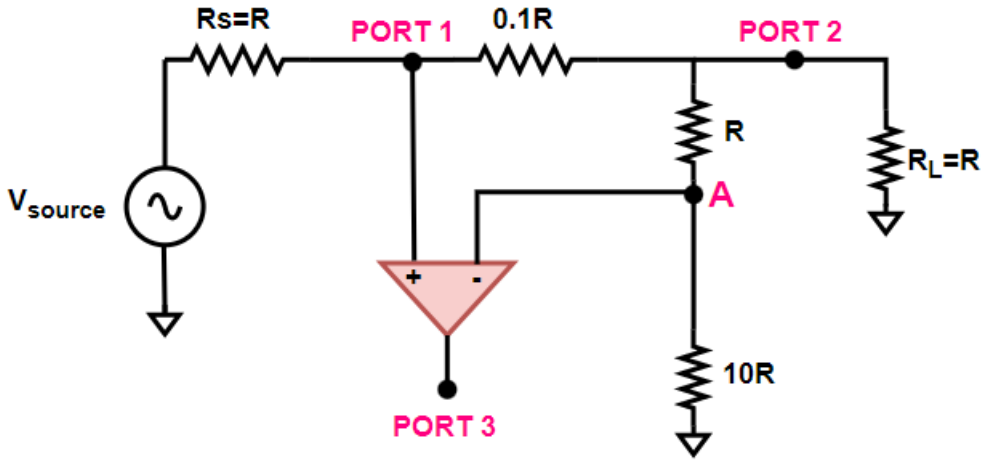


Figure 4.4 Schematic of single stage unidirectional bridge

The challenge of interfacing differential RF circuits to single-ended ones has been in discussion with the RF (and other) design community for many years. The differential to single converter shown in Fig. 4.5 can be replaced with an RF Balun. A balun is a two port transformer used to join a balanced line to an unbalanced line to match or transform the impedance of the network. It is used to subtract two different signals and gives an output of single ended signal. Fig. 4.8 shows a simple balun configuration.

A basic balun is a variation of a specialized RF transformer, and has many similarities to it; some systems have conflicting specifications which can be met with combinations of several baluns along with more complex topologies. A balun does not have an identified ”input” and ”output” port, but can be used either way; i.e the same balun component can be used for single-ended to balanced transformation as

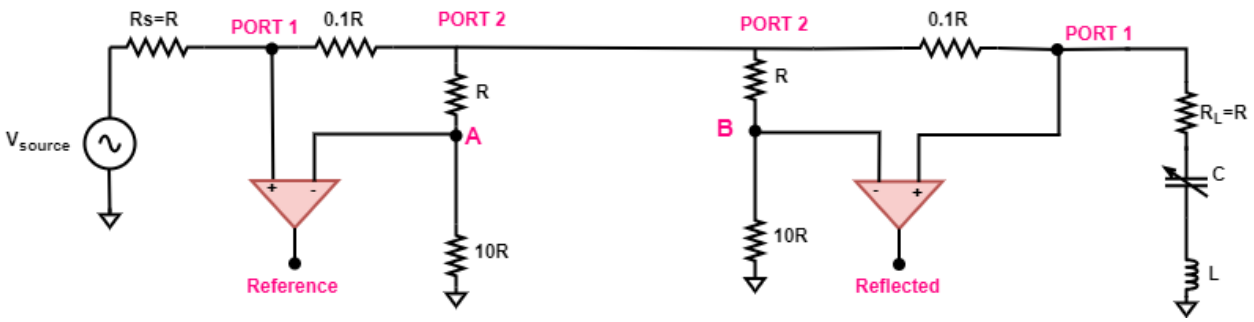


Figure 4.5 Schematic of directional bridge

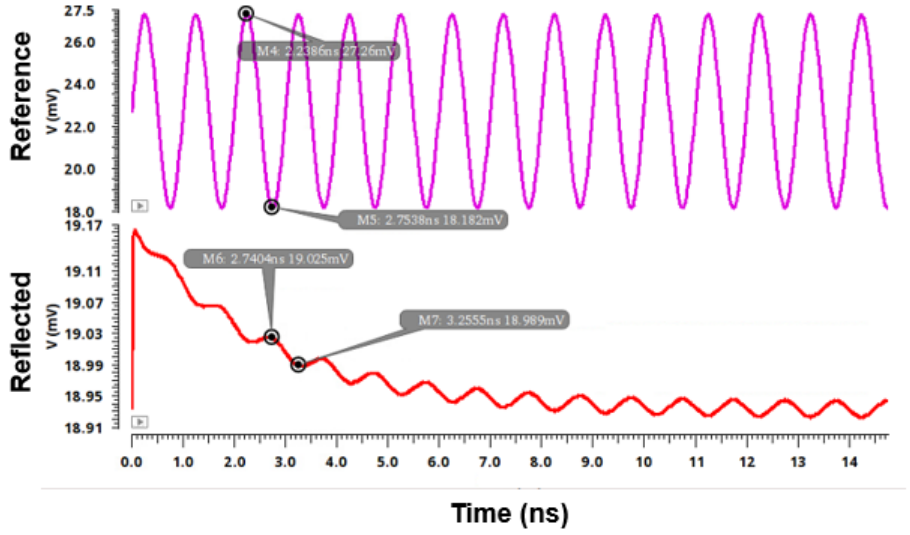


Figure 4.6 Reference and Reflected signals

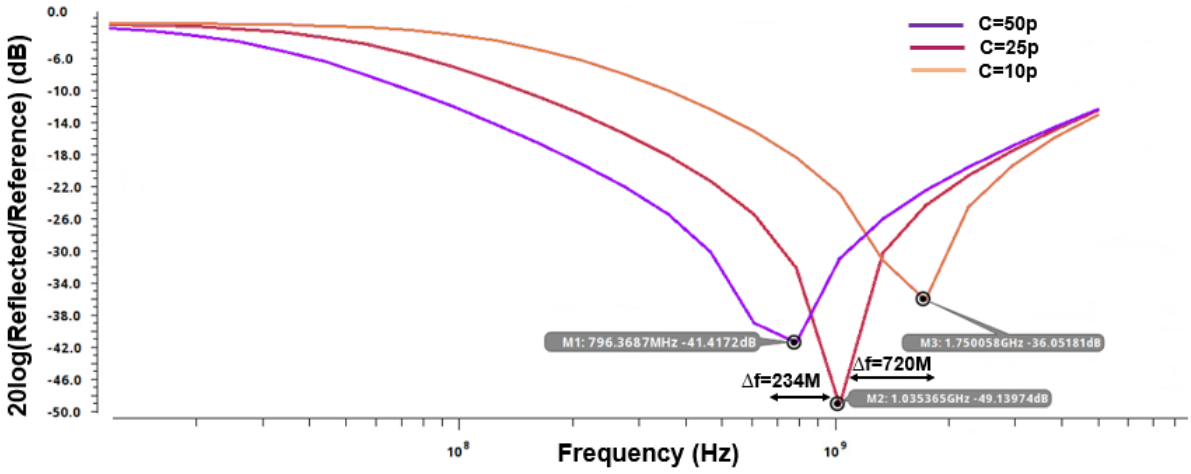


Figure 4.7 Peak shift for different capacitor values

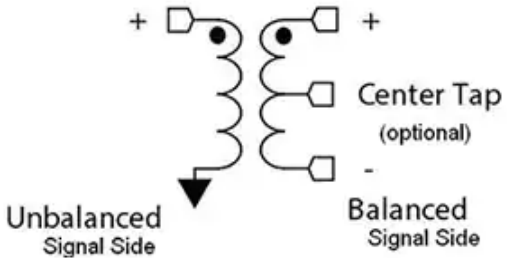


Figure 4.8 A simple balun architecture

well as the reverse. It can also provide resistive source-to-load impedance matching by selection of appropriate primary/secondary turns ratio, using the well-known formula:

$$\frac{Z_{primary}}{Z_{secondary}} = \left(\frac{N_{primary}}{N_{secondary}}\right)^2 \tag{4.5}$$

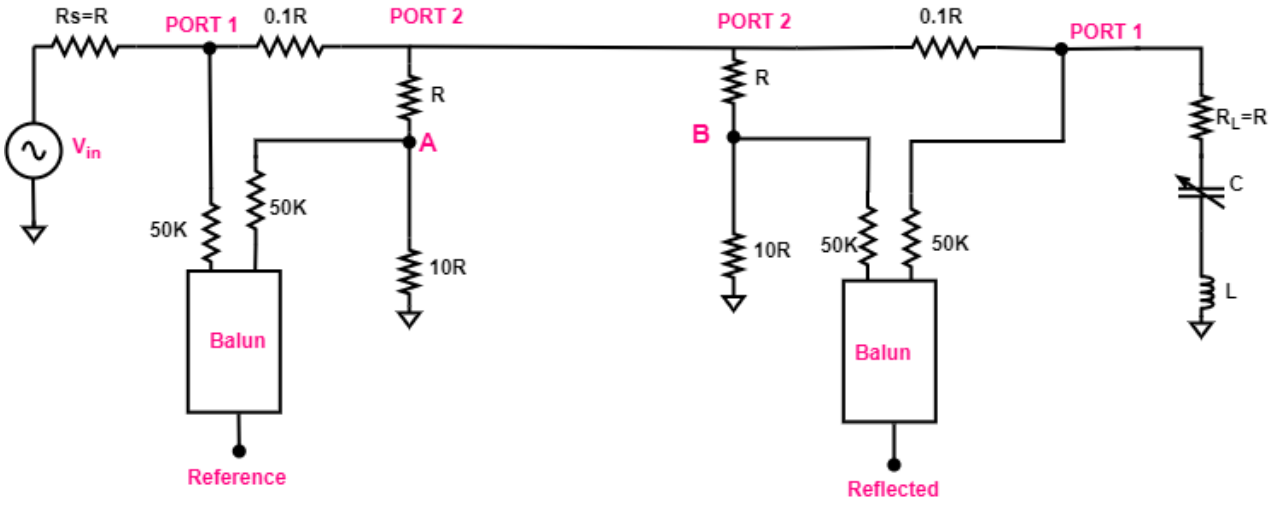


Figure 4.9 Schematic of directional bridge with balun

Fig. 4.9 shows the schematic of the proposed VNA with an RF-Balun. The results with integrating balun with the bridge is shown in Fig. 4.10. Ideally, zero current should flow inside the balun to avoid attenuation at the input ports of the balun. To ensure negligible input current flowing in balun, high resistance is kept at its input node. This prevents any voltage drop across the nodes of the bridge and provides high input impedance to the balun.

4.3.2 Voltage Controlled Oscillator

A current starved voltage controlled oscillator is proposed in the design to generate a input signal with varying frequency range. A current-starved voltage-controlled ring oscillator (CSVCRO) is an os-

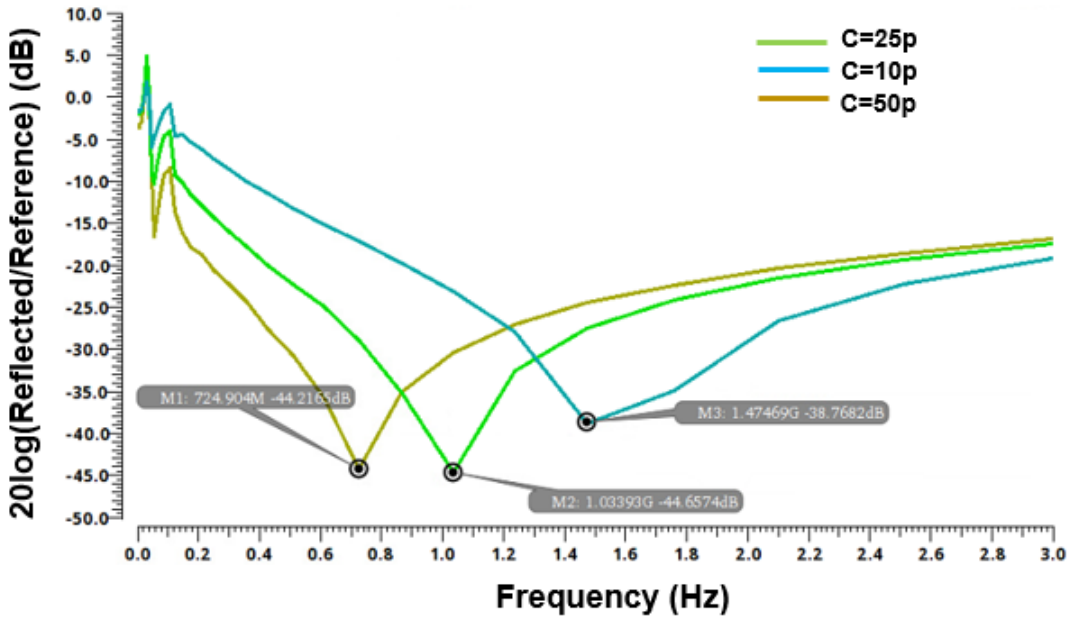


Figure 4.10 Plot of peak shift with different capacitor values on integrating balun

cillator circuit that uses the interaction between a voltage-controlled current source and a ring of inverter stages to generate an oscillating output. The basic structure of a CSVCRO includes a voltage-controlled current source, a number of inverter stages connected in a ring configuration, and a capacitor connected between the input and output of the ring. The voltage-controlled current source generates a current that is fed into the input of the first inverter stage. Each inverter stage in the ring amplifies the incoming current and inverts its phase, resulting in a sinusoidal output waveform that travels around the ring. As the output waveform reaches the input of the voltage-controlled current source, it modulates the current generated by the source, affecting the output of the inverter stages. This interaction between the voltage-controlled current source and the ring of inverters creates a positive feedback loop that sustains the oscillation. The frequency of the oscillation is determined by the load capacitance of the inverter stages and the transconductance of the voltage-controlled current source. The frequency can be adjusted by controlling the voltage applied to the voltage-controlled current source. In a current-starved configuration, the voltage-controlled current source operates in a region where its output current is limited by its internal resistance. This results in a reduction of the overall gain of the oscillator, which reduces the frequency stability and increases the phase noise of the output waveform. However, the current-starved configuration also provides a means of controlling the frequency and power consumption of the oscillator. The major applications of VCOs are optical transmission, clock generation, radio frequency integrated devices (RFID) transponders and data recovery circuits and also in medical domains.

The architecture of the proposed VCO is shown in Fig. 4.11. The current starved ring oscillator consists of 5 stage differential ended inverters. The differential oscillator has efficiency to reject

common-mode noise, power supply noise. The odd number of stages is connected such that the output of last stage is fed back to the input of first stage. In order to have sustained oscillations, it must satisfy necessary conditions i.e. the total phase shift around the loop must be 360° and the loop gain must be equal to unity as stated by Barkhausen. The differential ring oscillators are advantageous as they reject common mode noise and avoid usage of bypass and coupling capacitors together with high gain stability at high frequencies. The output oscillation at node Out of VCO at V_{ctrl} 650mV is shown in Fig. 4.12. The variation of frequency with respect to V_{ctrl} is shown in Fig. 4.13. Fig. 4.14, Fig. 4.15 and Fig. 4.16 demonstrates the output voltage swing at different values of V_{ctrl}.

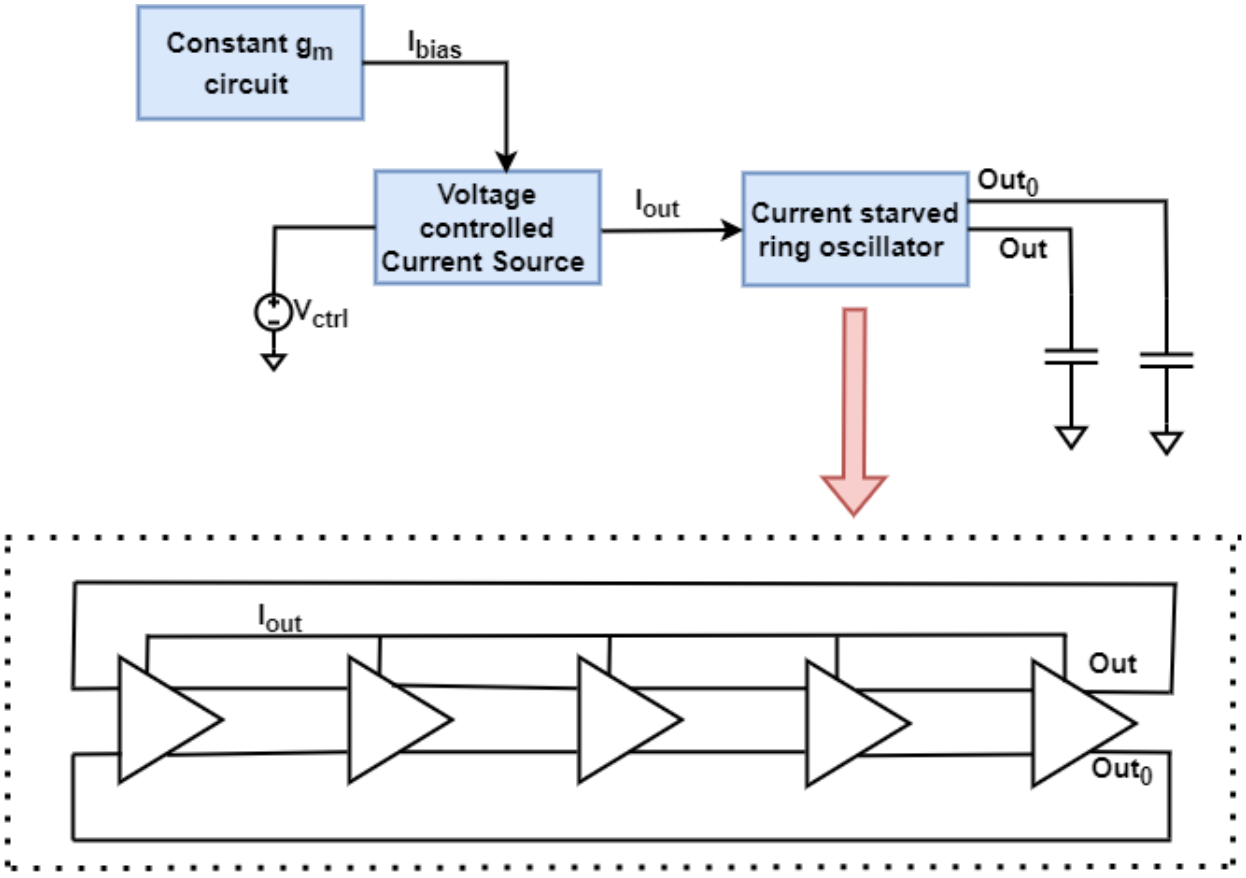


Figure 4.11 Archirecture of voltage controlled oscillator

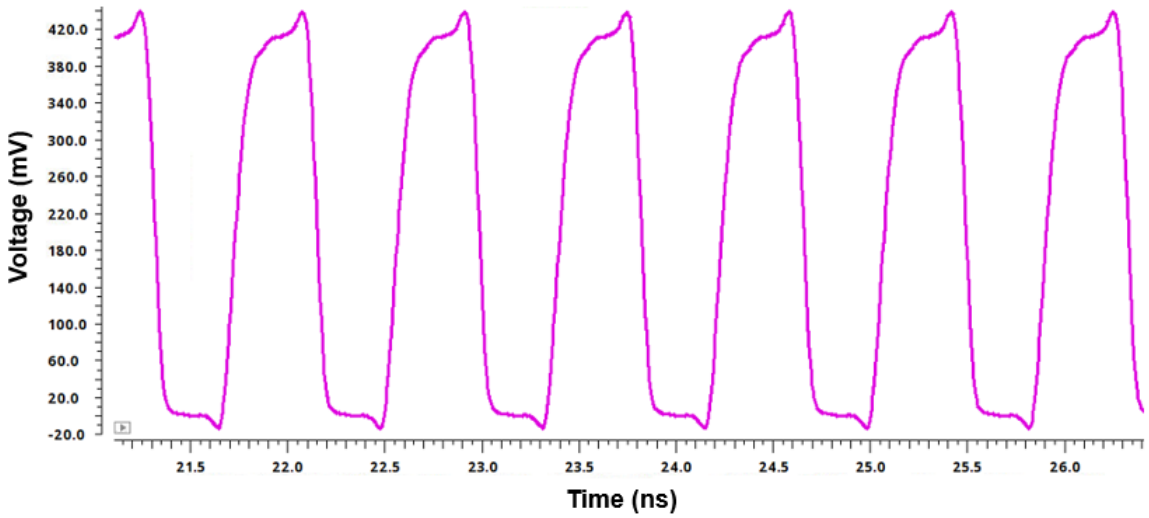


Figure 4.12 Plot of output of VCO at V_{ctrl} 650mV

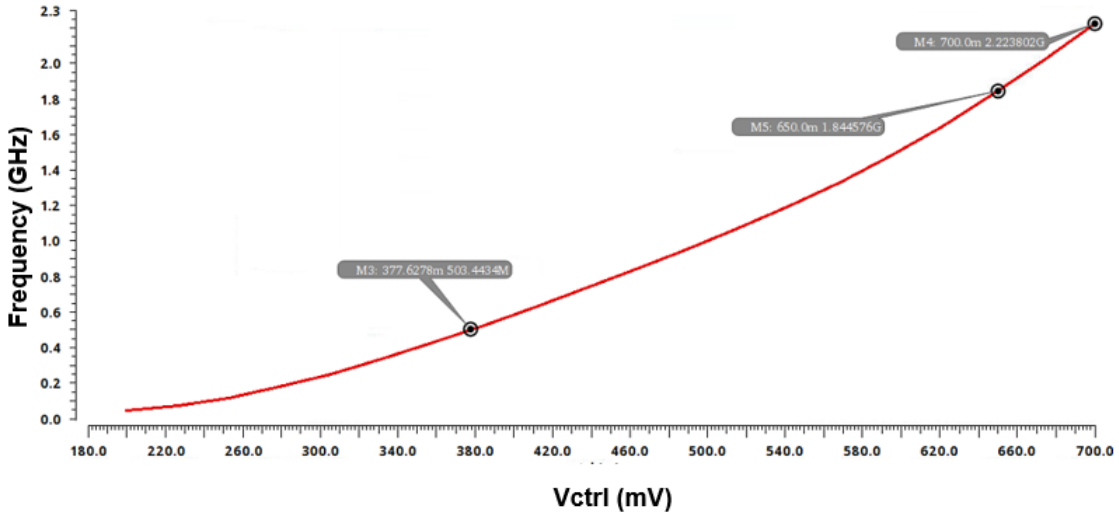


Figure 4.13 Variation of frequency with respect to V_{ctrl}

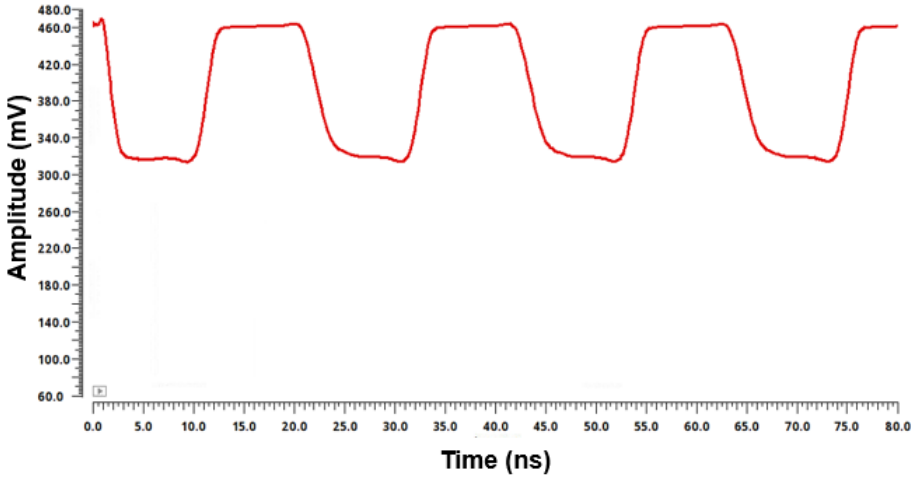


Figure 4.14 Output voltage swing at Vctrl 200m

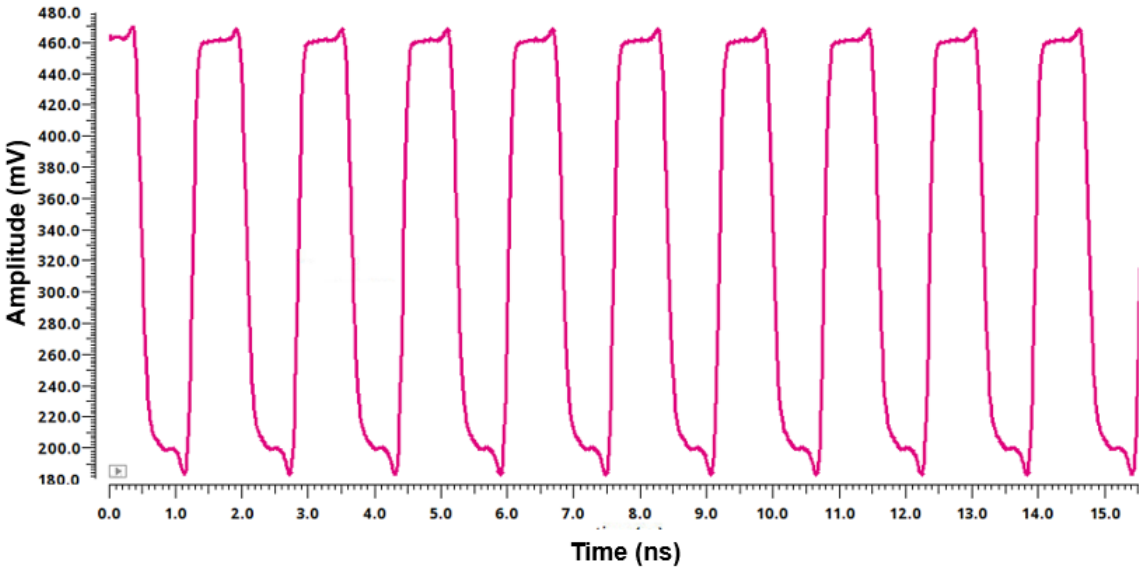


Figure 4.15 Output voltage swing at Vctrl 400m

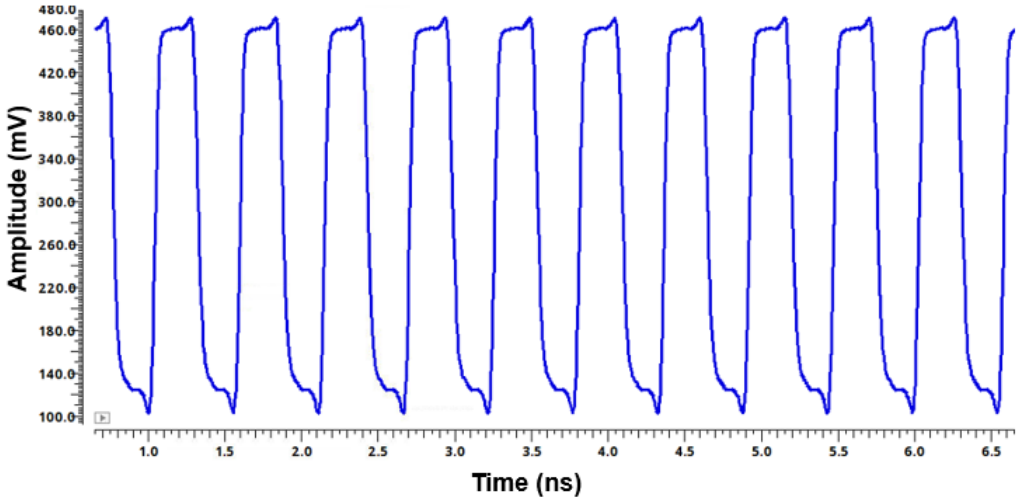


Figure 4.16 Output voltage swing at Vctrl 700m

4.3.3 Design of Wide Band Low Noise Amplifier (LNA)

In order to achieve low noise and high amplitude, Fig. 4.17 shows the wide band LNA which consists of noise cancelling and an output buffer stages using resistive feedback topology [59]. Input-matching, gain, noise figure (NF), linearity, and power consumption are crucial performance metrics that are tightly coupled in a typical low-noise amplifier (LNA). The proposed LNA achieves a minimum NF of 3.1dB and power gain of 15dB over a bandwidth of 0.5GHz to 2GHz while consuming 6 mW from a low supply voltage of 1V. The measures IIP3 point is -13 dBm at 1GHz.

The cascode structure is popularly used in LNA for narrow-band wireless applications. It is a two-stage amplifier consisting of common source and common gate (CS-CG) stages. In Fig. 4.17, R_F is the shunt feedback used for wideband matching. M1, M2 and M5 combine the signal and subtract the noise of M1. To subtract the noise at the drain of M2, the polarities of the signal at the drains of M1 and M2 will be in-phase. The transistor M5 is connected in common gate configuration to subtract the noise at the drain of M1 and M2.

The noise figure of a low-noise amplifier (LNA) is a measure of the amount of additional noise introduced by the amplifier, relative to the noise of the input signal. It is defined as the ratio of the output noise power to the input noise power, where the input noise power is the noise power at the input of the LNA and the output noise power is the noise power at the output of the LNA. The noise figure is usually expressed in decibels (dB) and is given by the equation: NF = 10 log10 (F), where NF is the noise figure and F is the noise factor, which is defined as the ratio of the output noise power to the input noise power, normalized to a reference temperature. A lower noise figure indicates that the LNA is introducing less additional noise, which is desirable for applications where a high signal-to-noise ratio is required. The noise figure of an LNA can be affected by various factors, including the input impedance, the gain of the amplifier, and the operating frequency range. Typically, LNAs have noise figures ranging

from a few tenths of a dB to several dB, depending on the specific design and application requirements. Fig. 4.18 shows the noise figure of the LNA. The noise figure of LNA is 3.1dB in frequency range of 500MHz to 2GHz which is suitable for our application. The power gain of LNA is demonstrated in Fig. 4.19. It can be seen that the LNA provides a gain of 15dB and the variation of gain is almost constant over a frequency range of 500MHz to 2GHz. The power consumption of the LNA at supply 1V is 15mW.

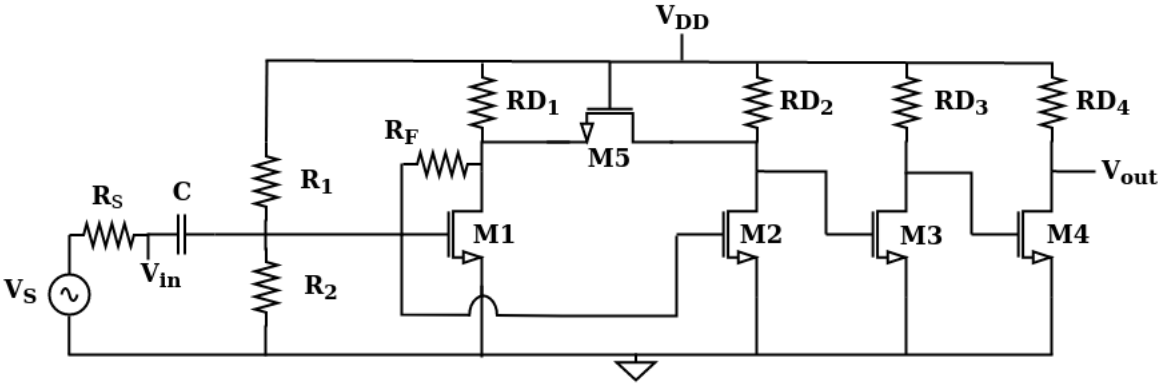


Figure 4.17 Schematic of LNA

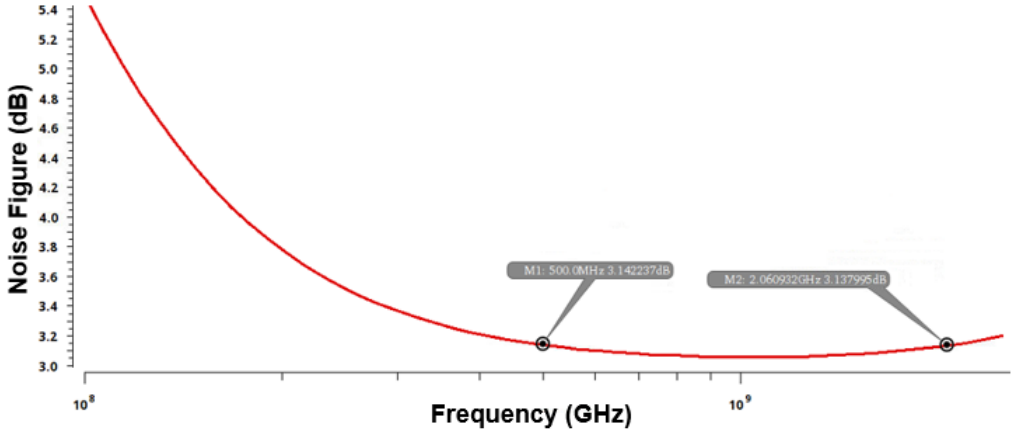


Figure 4.18 Noise Figure of LNA

IIP3 (third order input intercept point) is a measure of the linearity of an electronic component or system, such as a low noise amplifier (LNA). It is defined as the input power level at which the fundamental and third harmonic distortion products have the same power level. The IIP3 is a commonly used parameter to characterize the linearity of an LNA. The third-order intercept point (IIP3) of a low noise amplifier (LNA) is typically measured using two-tone testing, which involves applying two tones to the input of the LNA and measuring the third-order intermodulation products (IM3) at the output.

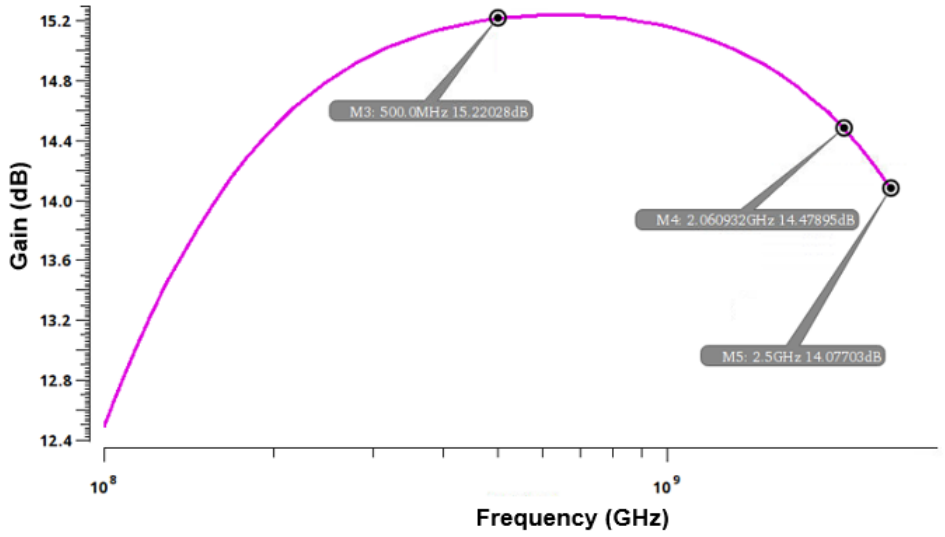


Figure 4.19 Gain of LNA

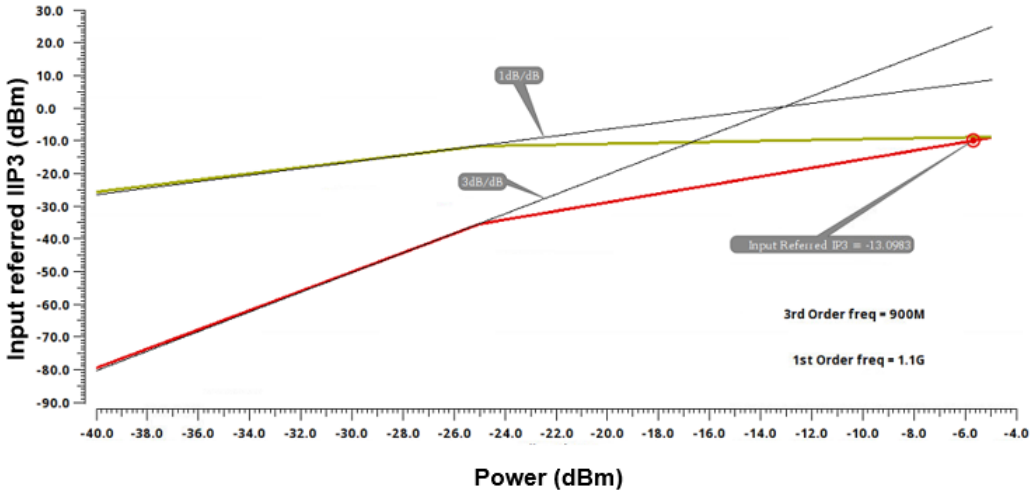


Figure 4.20 Plot of IIP3 of LNA

The input power levels of the two tones are adjusted such that they are close enough to each other to produce significant third-order distortion, but far enough apart that the distortion products can be easily measured. We have taken the first order frequency as 1.1GHz and third order frequency as 900MHz. A high IIP3 value indicates that the LNA is highly linear and can maintain its linearity even at high input signal levels. In other words, an LNA with a high IIP3 will produce less distortion and a more accurate output signal than an LNA with a low IIP3. Linearity is an important characteristic of an LNA because it determines how accurately the LNA can amplify weak input signals without distorting them. If the LNA is highly linear, it will amplify the input signal without introducing any significant distortion, resulting in an accurate output signal. However, if the LNA is not linear, it will introduce distortion to the output signal, which can significantly affect the accuracy of the signal. Fig. 4.20 shows the plot for linearity of LNA which has an IIP3 of -13dB.

4.4 Simulation Results

Fig. 4.21 shows the peak shift when all the blocks are combined together. From Fig. 4.22, the corresponding value of Vctrl vs frequency can be found out. The loading between VCO and directional bridge is achieved by adding a common source stage between them. We have taken water as our reference DUT. On testing water with VNA hardware, it was observed that the resonant frequency of water is at 1GHz. For getting the desired 1GHz frequency, the RLC values of DUT was calculated. Keeping R as 50Ω and 1nH inductor, to get a resonant frequency of 1GHz, the capacitor value was set to 25pF. With respect to 1GHz reference, on changing the capacitance value a shift in the peak is observed. On calculating the shift in the frequency with respect to 1GHz, the type of biomolecule can be identified. The proposed VNA design consumes a power of 45mW.

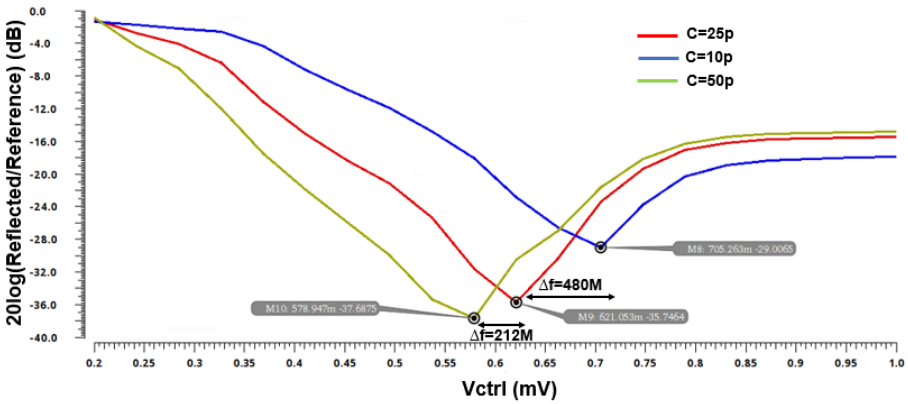


Figure 4.21 Plot of peak shift of complete architecture

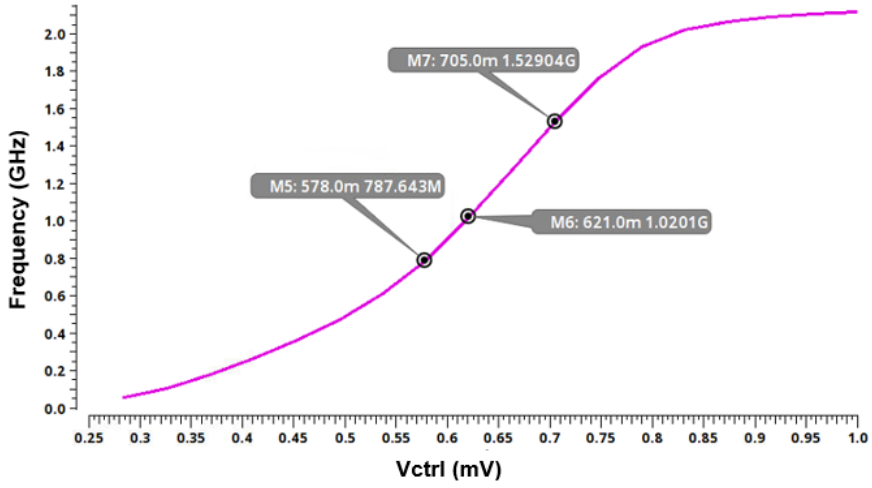


Figure 4.22 Gain of LNA

4.5 Conclusion

In this chapter, RF blocks are designed for detection of permeability and permittivity of an unknown samples. A 0.5GHz to 2GHz tunable fully integrated on-chip VNA design is proposed in CMOS 65nm technology. The on-chip VNA is used to detect any biomolecule/DUT placed on it by exploiting the characteristics of its dielectric properties. The objective of the work was to make an working concept of an on-chip VNA which can detect any change in the biomolecule. The biomolecule is replaced with an on-chip RLC circuit to prove the concept. Shift in the resonant frequency is observed due to capacitance change caused by addition of sample with significant relative permittivity. From the resonant frequency information, the value of permittivity of the sample can be found out. The full-integration architecture with the on-chip VNA and the sensing area is expected to achieve high sensitivity and practicality in clinical applications. The proposed work has a future scope of fabrication of the working model. The results shown so far are simulation results. Also an alternative approach can be used to replace balun with a differential to single converter to save the on-chip area and cost of fabrication. The future work of the proposed design also emphasizes on making the architecture further low power so that RF field of circuits can be used in low power applications.

Chapter 5

Conclusion and Future Work

The following section concludes and summarizes the results from the research work presented and the contributions made to the existing knowledge base related to the field of analog and RF circuits used in biomedical applications. With innovations in circuit design techniques, and with right technical approach complex biomedical applications are now becoming entirely implantable. The electronics of a general biomedical device typically consist of several subsystems that work together to perform the desired functions. Advances in technology have led to the development of new materials, processes, and circuit designs that enable higher performance, lower power consumption, and smaller form factors. These advances are driving the development of new biomedical devices and applications that are more capable, more reliable, and more accessible than ever before. This work presents the design techniques and architectural solutions for low power core analog blocks and RF blocks.

Many researchers have proposed different approaches for low power voltage and current references designs. However, the existing designs may not be able to achieve all the essential parameters of an ideal voltage/current reference. The voltage and current reference design in this thesis tries to provide an alternative approach and meet all the essential requirements of analog blocks that can be used in bioimplantable devices. This work also explores the RF domain used for detection of biomolecule which can be used as an useful clinical equipement. We presented the architecture and concept of on-chip VNA design which uses an RLC circuit as a biomolecule to verify the concept on-chip. Making an on-chip VNA will be a major development in the field of bioimplantable and bioclinical applications.

5.1 Contributions

Current Reference - Low power and low voltage CMOS current reference with a 0.55V supply and is presented. A peaking current source is proposed which cancels out the ratio of the compensated voltage and on-chip resistance by employing a CTAT voltage generator which exploits the threshold voltage dependence on the body to source voltage of the MOSFET, while consuming only 9.5nW of power and generating 5.6nA of reference current. The design enhances the performance of line regulation with the adopted PD-AMP which consumes only 0.62nA of current. The performance of the proposed circuit

makes it suitable for biomedical applications that require low-supply voltage and power consumption. While the viability of the proposed concept has been shown, for future work auto-trimming circuits can be designed for process independent current. As other applications, because of the competitive specifications of temperature coefficient, line sensitivity and power consumption, the proposed work can be used as an elementary circuit block for IoT applications.

Switched Capacitor Voltage Reference - As part of our research, we proposed a low-power SCN-based BGR suitable for biomedical applications. The proposed design demonstrates improved power consumption by employing a low-power novel clock generator circuit and driving the core BGR with slow PTAT clock signals. Biomedical signals has low frequency and voltage attribute, which is satisfied by the proposed work. We also explored the CTAT resistance of MOSFET to generate a PTAT clock signal. This work provides the lowest power consumption and on-chip area among the previous works, thereby contributing towards a new solution for low power and miniaturized wireless sensing systems.

On-chip VNA design for Biomolecule detection - In this chapter, RF blocks are designed for detection of permeability and permittivity of an unknown samples. A 0.5GHz to 2GHz fully integrated wideband on-chip VNA design is proposed in CMOS 65nm technology. The on-chip VNA is used to detect any biomolecule/DUT placed on it by exploiting the characteristics of its dielectric properties. The objective of the work was to make an working concept of an on-chip VNA which can detect any change in the biomolecule. The biomolecule is replaced with an on-chip RLC circuit to prove the concept. Shift in the resonant frequency is observed due to capacitance change caused by addition of sample with significant relative permittivity. From the resonant frequency information, the value of permittivity of the sample can be found out. The full-integration architecture with the on-chip VNA and the sensing area is expected to achieve high sensitivity and practicality in clinical applications. The proposed work has a future scope of fabrication of the working model. The results shown so far are simulation results. Also an alternative approach can be used to replace balun with a differential to single converter to save the on-chip area and cost of fabrication.

Related Publications

5.2 Relevent Publications

1. **Samriddhi Agarwal**; Ashutosh Pathy, Zia Abbas ***"A 9.5nW, 0.55V Supply, CMOS Current Reference for Low Power Biomedical Applications"***, *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS II), vol. 69, no. 9, pp. 3650-3654, Sept. 2022, doi: 10.1109/TCSII.2022.3183146.*, **[Published]**

2. **Samriddhi Agarwal**; Shameer Basha Yerragudi, Naveen Dasarai, Inhee Lee, Zia Abbas ***"An 18.5nW, 62.9dB PSRR, Switched-Capacitor Bandgap Voltage Reference using Low Power Clock Generator Circuit for Biomedical Applications"***, *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2023 **[Accepted: in Proceedings]**

5.3 Other Publications

1. Sahishnavi Bhartipudi, **Samriddhi Agarwal**, Shameer Basha Yerragudi, Naveen Dasari, Zia Abbas ***"Design of fully integrated wideband On-Chip Vector Network Analyzer for biomolecule detection"***, *M*icroelectronics Journal, 2023 **[Submitted]**

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