Design Techniques and Architectural Solutions for RF Circuits and Systems for Portable Sensing Applications

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by

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CERTIFICATE

It is certified that the work contained in this thesis, titled "Design Techniques and Architectural Solutions for RF Circuits and Systems for Portable Sensing Applications" by Adithya Sunil Edakkadan, has been carried out under my supervision and is not submitted elsewhere for a degree.

Date	Advisor: Prof. Abhishek Srivastava

To My Beloved Family and Friends

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Abstract

Advancements in electronics have revolutionized technology by making devices more portable and powerful. Integrated circuit technology has allowed for packing more functionality into compact spaces, leading to the development of portable gadgets that offer convenience and advanced features. Industries like healthcare, aerospace, and automotive have also benefited from miniaturized electronics, enabling remote patient monitoring, enhancing aircraft performance, and advancing smart vehicle technology. Additionally, miniaturization has improved energy efficiency, resulting in wireless and battery-powered devices for remote and off-grid applications. In this thesis, various circuit design techniques have been presented and prototype systems implemented for portable sensing applications.

Magnetometers form a key component of sensing systems used in fields such as geophysical and oceanic exploration and aerospace. Recently, diamond colour defect-based quantum sensing applications such as nitrogen-vacancy (NV) centre magnetometry have emerged in CMOS technology, which uses optically detected magnetic resonance (ODMR) for sensing magnetic field strengths ($|\tilde{\mathrm{B}}|$) from different environmental physical quantities. For ODMR based sensing, CMOS quantum sensors seek an on-chip 2.87 GHz microwave (MW) signal generator. Moreover, in order to sense smaller $|\tilde{\mathrm{B}}|$, these CMOS quantum sensors also require that MW signal should be swept with a sufficiently small step size near 2.87 GHz. It is also required that the PLLs should have low noise and low jitter for high stability and fast settling time. These requirements seek low phase noise voltage-controlled oscillator (VCO) with a small variation in its gain (K_{VCO}) within the desired tuning range. In this thesis, a fractional-N synthesizer based 2.87 GHz MW-generator (MWG) is presented with an extremely small programmable sweep step-size for improved sensitivity of $|\tilde{\mathrm{B}}|$ measurements in CMOS NV magnetometry along with a technique for designing a low-phase noise VCO with low K_{VCO} and small K_{VCO} variation is also presented.

Respiratory diseases contribute to a majority of deaths worldwide every year. Diseases such as asthma, bronchitis and pneumonia also adversely impact a person's social and economic conditions.

They can seriously threaten their health if left undiagnosed and untreated. Techniques such as auscultation are used in the diagnosis of most respiratory diseases. However, using such techniques requires an experienced physician and the diagnosis is subjective. To overcome these challenges, in this thesis, a portable handheld system has also been proposed and a proof of concept implemented to detect and classify respiratory diseases automatically through the use of convolutional neural networks (CNN) running on mobile platforms.

Recent developments in advanced driver assistance systems (ADAS) used in the automotive industry have raised the demands of mmWave radars in 24 GHz and 77 GHz bands. For higher accuracy and precision, frequency modulated continuous wave (FMCW) technique has become very popular for mmWave radars, which requires low phase noise and high bandwidth chirp frequency synthesizers. Such high-frequency band radars require programmable dividers with large divide ratios and fine frequency resolution to obtain high-frequency chirps with sufficiently large bandwidth. In this thesis, the implementation of a low phase noise, transformer tank based mmWave voltage controlled oscillator (VCO) near 20 GHz for multiplier based 77 GHz FMCW chirp synthesizer is presented along with a low-power multi-modulus programmable frequency divider for a frequency synthesizer operating in the 19.25-20.25 GHz frequency band from a reference frequency of 40 MHz. The applications of such radars in road safety and driver assistance is further explored by presenting a novel proof-of-concept that can efficiently classify targets in real-time under multiple classes. Hardware realisation, using a prototype Frequency Modulated Continuous Wave (FMCW) radar system, of the same has also been demonstrated.

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Chapter 1

Introduction

Advancements in electronics have revolutionized the way we interact with technology, making devices smaller, more portable, and incredibly powerful. The rapid progress in miniaturization has paved the way for a new era of convenience and accessibility, transforming various aspects of our lives. One of the remarkable achievements in electronics has been the shrinking of components and circuitry. Through advancements in integrated circuit technology, it has become possible to pack more functionality into smaller spaces. This has led to the development of compact yet powerful devices that fit in our pockets, such as smartphones, tablets, and wearable gadgets. These miniaturized electronics offer an array of features, including high-performance processors, ample storage, and advanced sensors, providing users with unprecedented convenience and functionality.

The reduction in size has not been limited to personal devices alone. Industries such as healthcare, aerospace, and automotive have also witnessed significant advancements. Portable medical devices, for instance, now enable healthcare professionals to monitor patients remotely and provide timely interventions. Similarly, the aerospace industry has benefited from miniaturized electronics in the form of lightweight and highly efficient navigation systems, enhancing aircraft performance and safety. In the automotive sector, compact electronics have contributed to the development of smart vehicles, equipped with advanced driver-assistance systems and enhanced connectivity. The miniaturization of electronics has also given rise to the Internet of Things (IoT) phenomenon, where everyday objects are interconnected, communicating and sharing information seamlessly. This interconnectedness has transformed our homes into smart homes, with devices such as smart thermostats, security systems, and voice-controlled assistants becoming commonplace. The IoT has expanded beyond homes to cities, industries, and infrastructure, enabling intelligent systems for efficient energy management, optimized transportation, and enhanced public services.

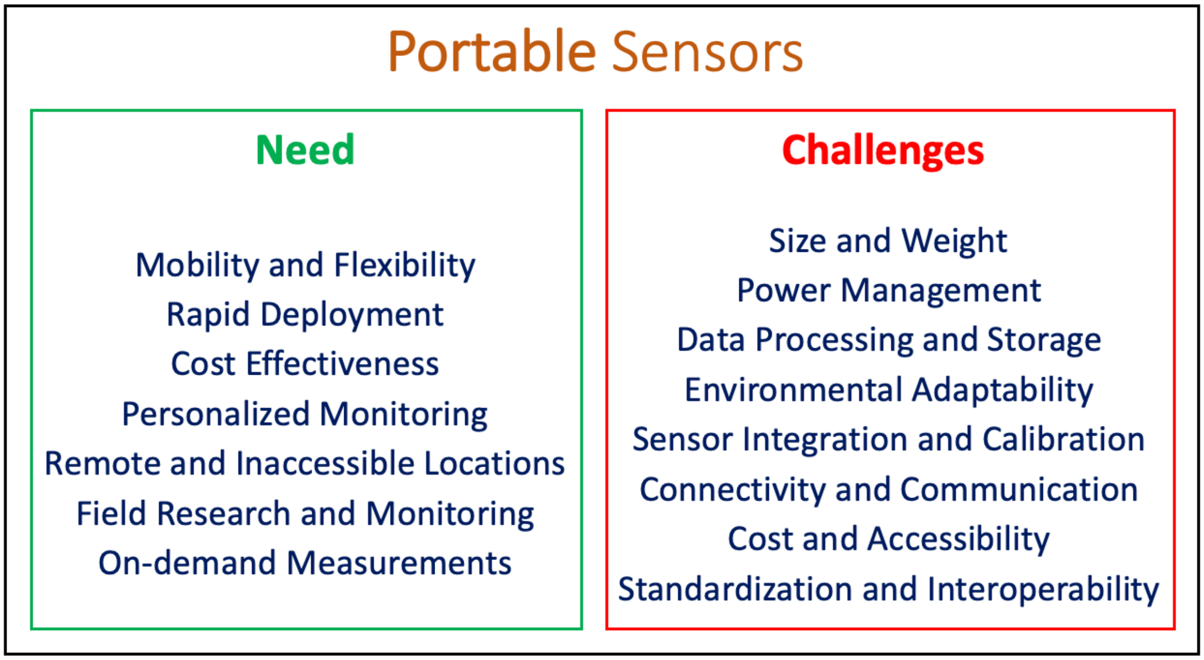


Figure 1.1: Need for portable sensors and the challenges faced

Furthermore, the advancements in miniaturization have brought about significant improvements in energy efficiency. Smaller electronic components consume less power, enabling devices to operate for extended periods on smaller batteries or even harvest energy from the environment. This has led to the proliferation of wireless and battery-powered devices, eliminating the need for cumbersome power cables and opening up possibilities for remote and off-grid applications. Fig. 1.1 summarizes the need for portable sensors and lists the challenges currently being faced when developing portable sensors.

1.1 Need for portable sensors

The integration of sensors into portable or field deployable systems plays a vital role in enabling a diverse range of applications.

Portable sensors play a crucial role in meeting the demands of various applications and addressing specific needs. Here are some key reasons why portable sensors are essential:

1. Mobility and Flexibility: Portable sensors provide the ability to collect data in real-time from different locations, including remote or challenging environments. They enable researchers, scientists, and professionals to gather information on the go, without being restricted to fixed monitor-

ing stations or laboratories. This flexibility is particularly valuable in fields such as environmental monitoring, healthcare, agriculture, and industrial settings.

2. Rapid Deployment: Portable sensors offer the advantage of quick and easy deployment. They can be readily carried and installed in different locations as needed, allowing for efficient data collection and analysis. This is especially beneficial in time-sensitive situations or emergency response scenarios, where immediate data acquisition is crucial for decision-making and problem-solving.

3. Cost-Effectiveness: Portable sensors often provide a cost-effective solution compared to larger, fixed monitoring systems. They eliminate the need for extensive infrastructure and can be easily repositioned or reutilized for various applications. This versatility and affordability make portable sensors accessible to a wider range of users and enable data collection on a larger scale.

4. Personalized Monitoring: Portable sensors enable individuals to monitor their own health, wellness, and environmental conditions. Wearable sensors, for example, can track vital signs, physical activity, sleep patterns, and environmental exposures. This personalized monitoring empowers individuals to make informed decisions about their well-being and take preventive measures when necessary.

5. Remote and Inaccessible Locations: Portable sensors are invaluable for gathering data in remote or hard-to-reach areas where installing permanent monitoring systems may be impractical or impossible. They enable data collection in wilderness areas, underground environments, oceans, and outer space, expanding our understanding of these regions and supporting scientific research and exploration.

6. Field Research and Monitoring: Researchers often require portable sensors for field studies and monitoring projects. These sensors allow for on-site data collection, measurements, and analysis in real-world conditions. Whether studying wildlife, ecological systems, or geological phenomena, portable sensors provide the necessary tools to gather accurate and relevant data directly from the field.

7. On-demand Measurements: Portable sensors enable users to obtain measurements whenever and wherever needed. This is particularly beneficial in quality control, industrial processes, and safety

inspections. Portable sensors can quickly assess parameters such as temperature, humidity, gas concentrations, or chemical properties, ensuring compliance with standards and identifying potential hazards in a timely manner.

1.2 Challenges

Making sensing systems portable presents several challenges that need to be addressed. Here are some key challenges:

1. Size and Weight: Shrinking the size and weight of sensing systems while maintaining their functionality is a significant challenge. Miniaturizing components, integrating multiple sensors, and optimizing power consumption are crucial factors to consider. Balancing compactness with performance can be a complex engineering task.

2. Power Management: Portable sensing systems typically rely on batteries or energy harvesting methods. Maximizing battery life and optimizing power consumption are essential to ensure longer operation and minimize the need for frequent recharging or replacement. Efficient power management techniques and low-power design strategies are critical in addressing this challenge.

3. Data Processing and Storage: Portable sensing systems generate vast amounts of data, requiring efficient processing and storage solutions. The limited computational resources and storage capacity of portable devices pose challenges in handling and analyzing large datasets. Developing algorithms for real-time data processing and implementing data compression techniques become necessary.

4. Environmental Adaptability: Portable sensing systems may encounter a wide range of environmental conditions, including temperature variations, humidity, dust, and vibrations. Ensuring robustness and reliability in different environments is crucial. Designs must account for protection against external factors, such as rugged casings, waterproofing, and resistance to temperature extremes.

5. Sensor Integration and Calibration: Integrating multiple sensors into a portable system and ensuring their accurate calibration can be challenging. Different sensors may have varying charac-

teristics, response times, and calibration requirements. Ensuring seamless integration, calibration accuracy, and sensor reliability are essential for precise and consistent measurements.

6. Connectivity and Communication: Portable sensing systems often require communication capabilities to transmit data to external devices or networks for further analysis or remote monitoring. Reliable wireless communication protocols and connectivity options need to be implemented, considering factors such as range, power efficiency, and data security.

7. Cost and Accessibility: Developing portable sensing systems that are affordable and accessible is important for widespread adoption. Cost-effective manufacturing processes, component selection, and scalability considerations are crucial to make these systems affordable without compromising quality and performance. Additionally, ensuring user-friendly interfaces and intuitive operation enhances accessibility and usability.

8. Standardization and Interoperability: Standardizing communication protocols, data formats, and interfaces among portable sensing systems is essential to enable interoperability and seamless integration with other devices or networks. Ensuring compatibility and ease of integration between different sensing systems can enhance collaboration, data sharing, and system interoperability.

Chapter 2 introduces the concepts involved in NV magnetometry and Fractional-N PLL design while Chapter 3 details the design, implementation and performance of the 2.75-2.94 GHz voltage controlled oscillator with low gain variation followed by Chapter 4 which details the design, implementation and performance of the 2.87 GHz Frequency Synthesizer with Programmable Sweep. Chapter 5 introduces the need for portable respiratory sound classification systems and details the implementation and results of the proposed system. Chapter 6 introduces the need for mmWave radars and the concepts involved in their design and usage. Chapter 7 details the design, implementation and simulation results of the voltage-controlled oscillator and multi-modulus divider for FMCW chirp synthesizer while Chapter 8 details the implementation of the radar-based object classification system. Chapter 9 finally concludes the thesis and mentions the scope of improvement for this work.

Chapter 2

Oscillators, PLLs and NV Magnetometry

Oscillators are vital components in modern electronics, serving a critical role in various applications. Their necessity stems from their ability to generate continuous and stable waveforms with precise frequencies. Frequency synthesis is a critical application of oscillators. By combining oscillators with frequency dividers, phase-locked loops, and other circuitry, complex frequency synthesis circuits can generate a wide range of frequencies with high accuracy and stability. Frequency synthesizers find extensive use in telecommunications, radar systems, test equipment, and many other applications that require precise frequency generation.

Most applications make use of oscillators with tunable output frequencies. As shown in Eq. 2.1, the output frequency of an ideal voltage-controlled oscillator (VCO) is a function of the input control voltage.

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont} \tag{2.1}$$

ω_0 is the output frequency when the control input is 0 and K_{VCO} is the gain of the VCO. [1]

2.1 VCO Performance

The performance of a VCO is measured in terms of the following parameters:

1. Center Frequency

2. Tuning Range

3. Tuning Linearity

4. Output Amplitude

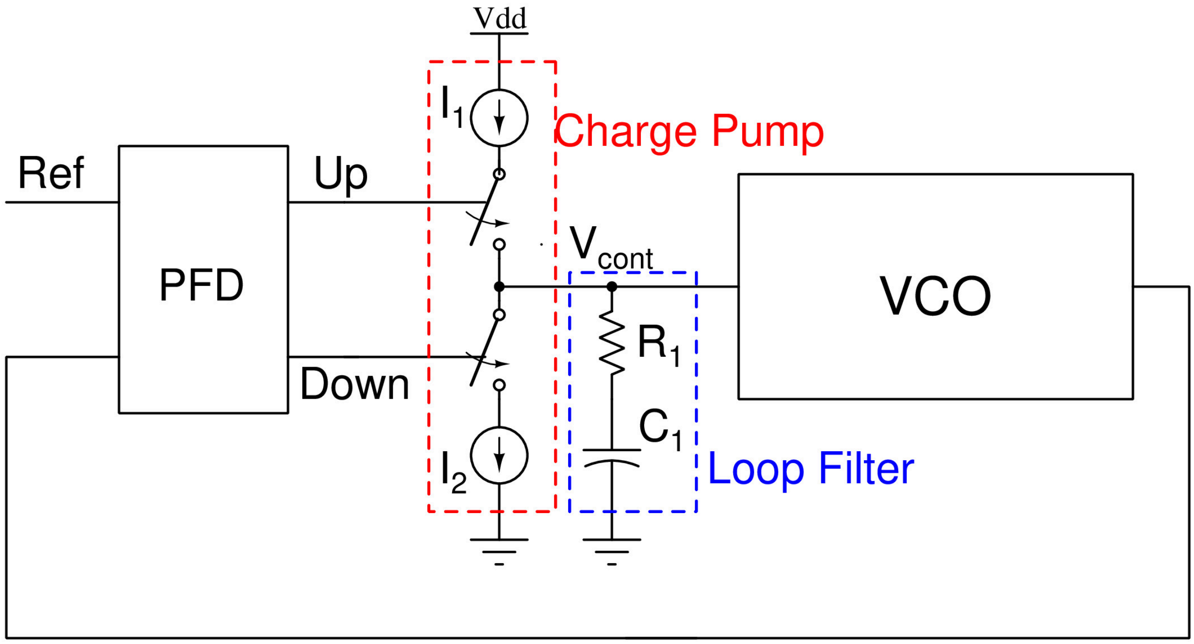


Figure 2.1: Charge-pump PLL

5. Power Dissipation

6. Supply and Common-Mode Rejection

7. Output signal Purity

2.2 PLLs

Phase-Locked Loops (PLLs) are widely used in diverse electronic applications due to their versatile functionality and ability to synchronize signals. PLLs find extensive use in communication systems, frequency synthesis, clock recovery, data synchronization, and many other areas. Fig. 2.1 depicts the block diagram of a basic charge pump PLL.

In communication systems, PLLs are employed for carrier recovery and synchronization. They help extract the carrier signal from the received modulated signal and maintain synchronization with the transmitter's carrier frequency and phase. PLLs play a vital role in achieving reliable and accurate data transmission in wireless communication, satellite communication, and digital broadcasting. PLLs also play a significant role in clock recovery and synchronization. They are used to extract timing information from incoming signals, recovering the clock signal and maintaining synchronization with the data stream. Clock recovery PLLs are utilized in data communication systems, high-speed digital interfaces, and storage devices to ensure accurate data transfer and synchronization.

Furthermore, PLLs are used for data synchronization in various applications. They help align the timing of incoming data streams, allowing for proper data sampling and processing. This is crucial in applications such as digital audio/video processing, digital data acquisition systems, and synchronization of data in network protocols. Frequency synthesis is another crucial application of PLLs. By employing PLLs with voltage-controlled oscillators (VCOs), desired frequencies can be generated with exceptional accuracy and stability. Frequency synthesizers based on PLLs are widely used in radio transceivers, cellular networks, and other communication systems where precise frequency generation is essential.

2.3 PLL Stability

The stability of a Phase-Locked Loop (PLL) is influenced by several factors that can impact its performance. These factors include:

1. Loop Filter Design: The design of the loop filter, which consists of passive components such as resistors, capacitors, and sometimes active components, plays a critical role in determining the stability of the PLL. The filter characteristics, such as its bandwidth and damping factor, need to be carefully chosen to ensure stability.

2. Loop Bandwidth: The loop bandwidth determines how fast the PLL can track and lock onto the input signal. A wide loop bandwidth can result in faster response but may also introduce instability if not properly controlled. The loop bandwidth should be selected based on the system requirements and the characteristics of the input signal.

3. Phase Detector Characteristics: The phase detector is responsible for comparing the phase of the input signal with the output signal of the Voltage-Controlled Oscillator (VCO). The type of phase detector used and its characteristics, such as linearity and dead zone, can affect the stability of the PLL. A well-designed phase detector is essential for stable operation.

4. Noise and Disturbances: Noise and disturbances present in the system can affect the stability of the PLL. Sources of noise can include power supply variations, thermal effects, electromagnetic

interference, and other external factors. Proper filtering and shielding techniques are necessary to minimize the impact of noise and disturbances on the PLL's stability.

5. Component Variations: Variations in component values, such as resistors, capacitors, and VCO characteristics, can affect the stability of the PLL. Manufacturing tolerances and temperature variations can introduce deviations in the expected behaviour of the components, leading to stability issues. Careful component selection and calibration are important to ensure stability.

6. Operating Conditions: The operating conditions of the PLL, such as temperature, voltage, and load variations, can influence its stability. PLLs should be designed to operate reliably within the specified operating conditions to maintain stability.

7. Feedback and Loop Gain: The loop gain, which is the gain around the feedback loop, should be properly controlled to avoid instability. Excessive loop gain can lead to oscillations, while insufficient loop gain can result in poor tracking and locking performance. Proper adjustment of the loop gain is crucial for stability.

2.4 NV Defect

The nitrogen vacancy (NV) defect in diamonds is a fascinating phenomenon that has attracted significant interest in the field of quantum science and technology. It refers to a specific atomic defect in the crystal lattice of diamond where a nitrogen atom replaces a carbon atom, and an adjacent carbon atom is missing.

The NV defect possesses unique properties that make it highly desirable for various applications. One of its key features is its ability to exhibit quantum properties at room temperature, which is uncommon for most quantum systems. Moreover, the NV defect in diamonds is extremely sensitive to external influences, such as magnetic fields and temperature changes. This sensitivity has made it a valuable tool for high-resolution sensing and imaging applications. It can be used as a nanoscale sensor to detect and measure magnetic fields with exceptional precision, enabling advancements in fields like biomagnetism, material science, and magnetic resonance imaging (MRI).

The energy levels of the NV defect play a crucial role in its quantum behavior and applications. The defect consists of a ground state, excited states, and a long-lived spin-triplet metastable state. The ground state is a spin triplet state with three sublevels, while the excited state is a spin singlet state. The spin-triplet metastable state has a longer lifetime and is particularly important for quantum information storage and manipulation. The energy levels can be controlled and manipulated through external factors such as optical excitation or microwave radiation. This allows researchers to initialize, manipulate, and read out the quantum state of the defect, enabling coherent quantum operations and information processing.

2.5 ODMR

Optically Detected Magnetic Resonance (ODMR) is a powerful technique that combines the principles of magnetic resonance spectroscopy with optical detection methods. It enables the study and characterization of spin-dependent processes in a variety of materials, ranging from solid-state systems to molecular complexes. ODMR relies on the interaction between electron spins and external magnetic fields. When subjected to a static magnetic field, the electron spins undergo a phenomenon known as resonance, where they absorb or emit electromagnetic radiation at specific frequencies. This resonance behavior provides valuable insights into the structure, dynamics, and environment of the electron spins within the material.

In ODMR, the resonance is typically detected using optical techniques. A laser beam is used to optically excite or probe the sample, and the resulting fluorescence or absorption signals are analyzed to extract information about the spin states and their dynamics. By varying the applied magnetic field and monitoring the optical response, ODMR can precisely determine the g-factors, spin relaxation times, and other spin-related parameters of the system under investigation.

ODMR has found widespread applications in various scientific fields. In material science, it is used to investigate defects, impurities, and dopants in crystals and semiconductors, providing valuable information about their electronic properties and spin dynamics. In the field of spintronics, ODMR helps in understanding and controlling spin-dependent transport phenomena in magnetic materials and spin-based devices. Furthermore, ODMR is also employed in studies related to molecular magnets, quantum information processing, and biological systems.

The advantages of ODMR lie in its non-destructive and highly sensitive nature. It allows for the characterization of spin-dependent processes at low temperatures and even at room temperature, making it suitable for a wide range of experimental setups. Additionally, ODMR can be combined with other spec-

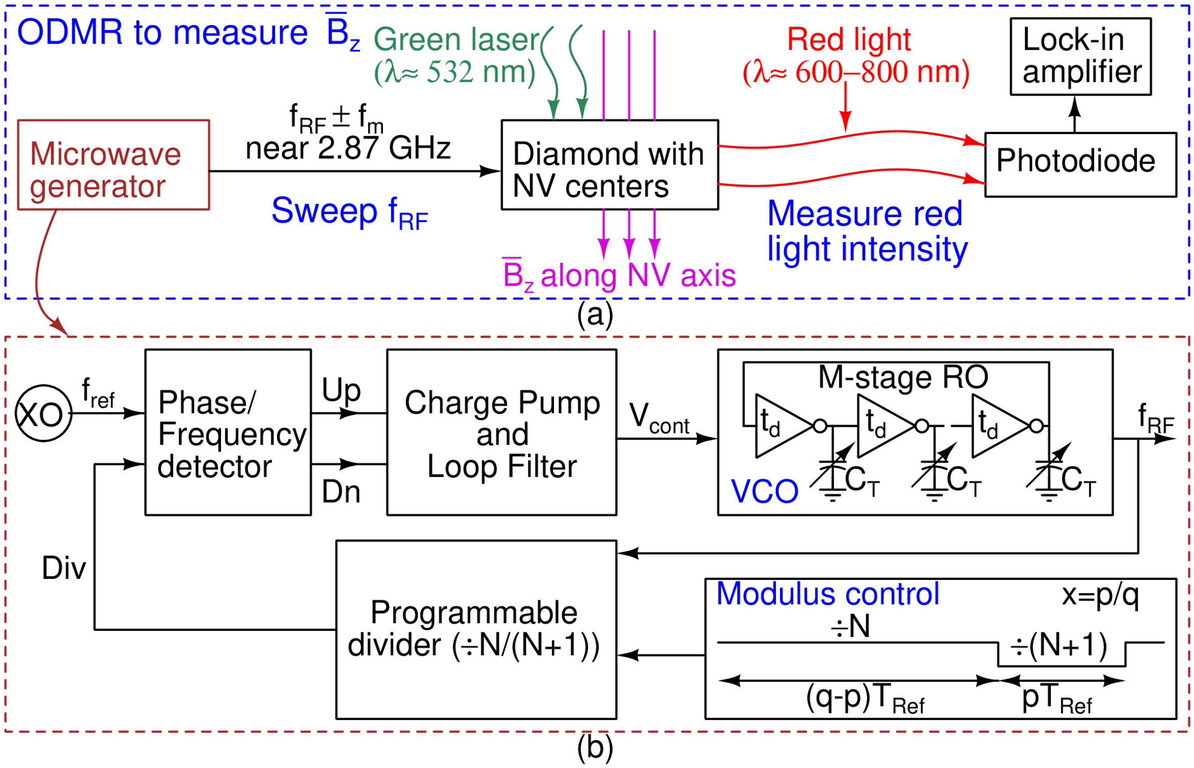


Figure 2.2: (a) Depiction of NV-ODMR to measure magnetic field strength ($|\vec{B_z}|$) and (b) Fractional-N synthesizer as microwave signal generator

troscopic techniques, such as electron paramagnetic resonance (EPR) and optical spectroscopy, to provide complementary information and a more comprehensive understanding of the underlying physics.

2.6 NV Magnetometry

Nitrogen-Vacancy (NV) centre in diamond behaves as an isolated electronic spin system that can be used in quantum sensors [2]. When a vacancy replaces the adjacent carbon pair in a diamond lattice, the nitrogen atom and the vacancy form an NV centre. The NV defect has its ground level in a spin triplet state whose sub-levels are split in energy into a singlet ($m_s = 0$) and a doublet of degenerate levels ($m_s = \pm 1$) separated by 2.87 GHz [3]. When an external magnetic field is applied on the NV ground state spin triplet, a Zeeman shift of energy $\gamma_e B_z$ is induced, where B_z represents the magnetic field component along the NV symmetry axis. As shown in Fig. 2.2(a), optically detected magnetic resonance (ODMR) technique can be used in NV-based sensing to measure static or slow varying $|\vec{B_z}|$ [2], [3]. In ODMR, NV electron spin transitions are excited by a microwave signal (f_{RF}) near 2.87 GHz and diamond is irradiated with a green light, which produces a red light proportional to $|\vec{B_z}|$ and having photon frequency Δf_p given in Eq. (2.2) [2], which is detected using a photo-diode.

$$\Delta f_p = f_+ - f_- = 2\gamma_e|\vec{B_z}| \tag{2.2}$$

In Eq.(2.2), γ_e is gyromagnetic ratio (28 GHz/T) and f_+ and f_- are the transition frequencies from the singlet level to the doublet levels. Usually, NV-ODMR is detected with lock-in technique for which f_{RF} is frequency modulated (f_m) while using an external source [2], [3]-[13]. The sensitivity of measured $|\vec{B_z}|$ can be improved with reduced f_m, which results into lower Δf_p as given in Eq. (2.2). Moreover, overall power can also be reduced by having on-chip frequency sweep than using the external frequency modulator.

Chapter 3

A 2.75-2.94 GHz Voltage Controlled Oscillator with Low Gain Variation for Quantum Sensing Applications

3.1 Introduction

Phase Locked Loops (PLL) are commonly used for high frequency carrier synthesis in wired and wireless transceivers. Recently, quantum sensing applications have also emerged that demand low noise PLLs with high stability and small settling time for microwave frequency generation. For example, nitrogen vacancy based magnetometry applications seek low noise, narrow bandwidth microwave generators near 2.87 GHz with very fine frequency resolution [2]. These low noise PLLs seek voltage controlled oscillators (VCO) with low gain (K_{VCO}) and small variation in its gain [3]. Therefore, there is a need to develop VCOs with low variation in K_{VCO} for quantum sensing applications. In this chapter, I present - 1) a technique with detailed analysis to reduce the variation in K_{VCO} of LC oscillators, 2) design and implementation of an LC VCO with low K_{VCO} variation in 180 nm CMOS technology and 3) post-layout simulation results to validate the proposed technique for LC VCO design of low K_{VCO} with reduced K_{VCO} variation.

The chapter is organized as follows: section 3.2 presents the background of this work and review of prior related works. In section 3.3 architecture of the VCO and detailed analysis of the proposed low K_{VCO} variation technique is presented. The circuit implementation and simulation results are discussed in section 3.4 and the conclusion is presented in section 3.5.

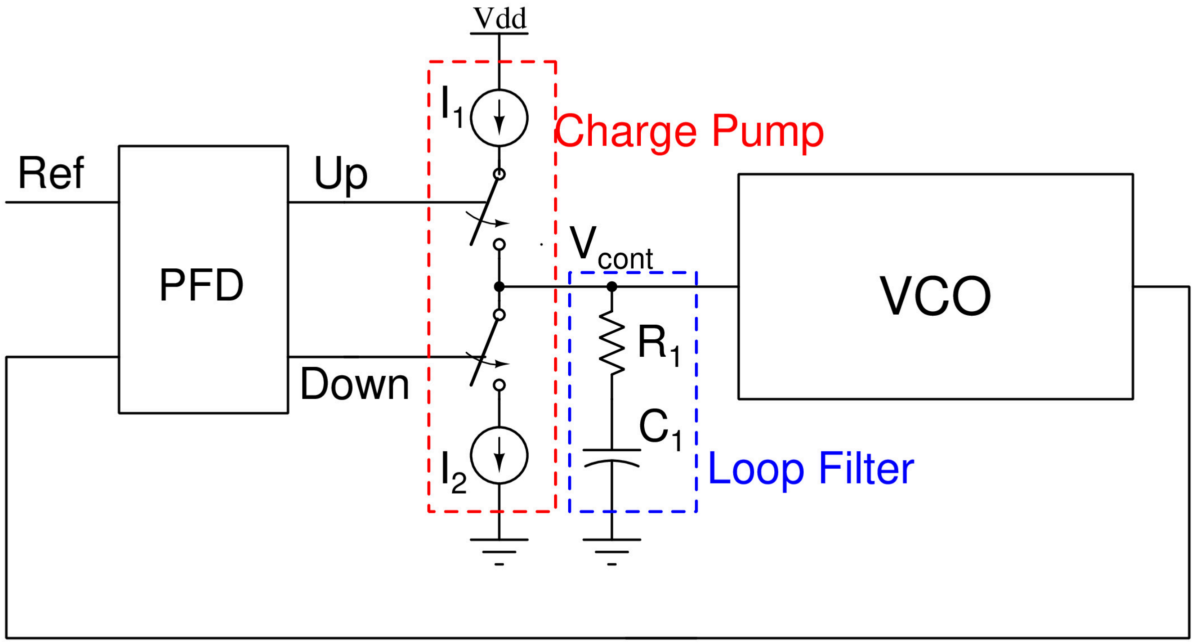


Figure 3.1: Charge-pump PLL

3.2 Background and Prior Works

3.2.1 Background

Fig. 3.1 depicts the block diagram of a PLL, which contains a phase frequency detector (PFD) followed by a charge pump, a loop filter and a voltage controlled oscillators (VCO) [1]. Eq. (3.1) shows the closed loop transfer function of the PLL [1].

$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_p}{2\pi} K_{VCO} R_1 s + \frac{I_p}{2\pi C_1} K_{VCO}} \tag{3.1}$$

In Eq. (3.1), the denominator is of the form $s^2 + 2\zeta w_n s + w_n^2$ and the damping factor (ζ) and natural frequency (ω_n) are represented by equations (3.2) and (3.3), respectively, where I_p is the charge pump current, C_1 is loop filter capacitance and R_1 is loop filter resistance.

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi}} \tag{3.2}$$

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}} \tag{3.3}$$

ζ and ω_n determine the stability of the PLL as well as the phase noise performance [4]. For the loop to remain stable, the value of ζ should be near unity [4]. The settling speed can be measured using the quantity represented in Eq. (3.4).

$$\frac{1}{\zeta\omega_n} = \frac{4\pi}{R_1 I_p K_{VCO}} \tag{3.4}$$

Important characteristics of the PLL such as phase noise performance and loop characteristics are determined by its VCO. The VCO phase noise ($\overline{\phi_{out}^2}$) shaped by the PLL is given by Eq. (3.5) [4].

$$\overline{\phi_{out}^2} = \frac{\omega^4}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2\omega_n^2\omega^2}\left(\frac{\alpha}{\omega^3} + \frac{\beta}{\omega^2}\right) \tag{3.5}$$

where α and β are factors which contain information about the noise injected and the Q value, respectively. For a PLL in operation, values of I_p, C_1 and R_1 are fixed and the only scope for large variations is in K_{VCO}. From equations (3.2) - (3.5), it can be inferred that for given I_p, C_1 and R_1, large variations in K_{VCO} will degrade the PLL stability, settling time and the phase noise performance. In order to ensure operation of the PLL in its desired dynamics, variations in K_{VCO} should be minimized. There have been several techniques proposed in the past to reduce the K_{VCO} variation [5]-[10], which are discussed in the following subsection.

3.2.2 Literature review

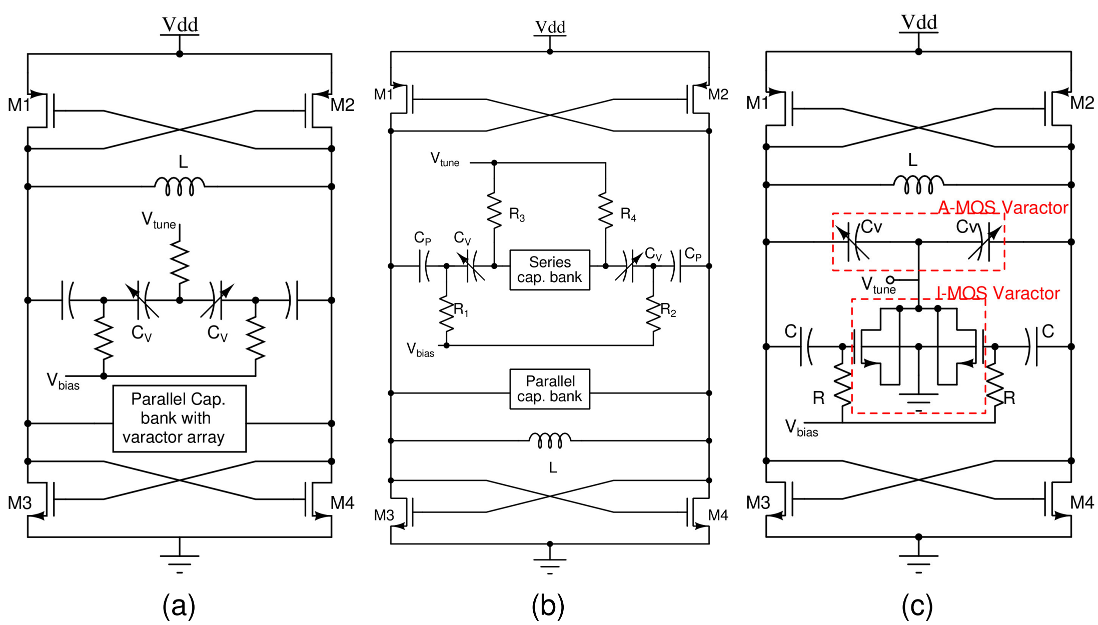


Figure 3.2: Schematic of related works: (a) [5] (b) [6] and [7] (c) [8]

As shown in Fig. 3.2(a), [5] uses a switched varactor array connected in parallel with a capacitor bank (C_{bank}) that is used to compensate the variation in K_{VCO} when there is change in value of C_{bank}.

When a C_{bank} structure is connected in series with the varactor, it has higher value of K_{VCO} at higher value of C_{bank} and when C_{bank} structure is connected in parallel with the varactor, it has a lower value of K_{VCO} at higher value of C_{bank}. Therefore, as shown in Fig. 3.2(b), [6] and [7] propose the use of the series and parallel C_{bank} structure such that their opposite impact on value of K_{VCO} minimizes it's variation. As shown in Fig. 3.2(c), [8] proposes the use of bias shifted inversion mode MOS varactor connected in parallel with conventional accumulation mode MOS Varactor. For reduced gain variation in ring oscillators, [9] proposed a cross-coupled pair with capacitive degeneration and [10] proposed using peak inductors.

In this work, we present a technique to control C_{bank} and V_{bias} simultaneously for reduced K_{VCO} variation in an LC oscillator. The proposed VCO architecture and its detailed analysis is presented in the following subsection.

3.3 Proposed Architecture and Detailed Analysis

3.3.1 Architecture of the Proposed LC VCO With Low K_{VCO} Variation

Fig. 3.3(a) shows the block diagram of the proposed LC VCO. It consists of an NMOS cross coupled pair with a tail current source, a main tank, an auxiliary tank and a digital to analog converter (DAC). As shown in Fig. 3.3(a), the main tank is comprised of an inductor (L) and switched capacitor bank in parallel. As shown in Fig. 3.3(a), C_{bank} structure is controlled by an N-bit digital control signal, which is used for the coarse tuning of the oscillator. Same N-bit signal controls the DAC, which generate the desired bias voltage for varactor capacitance change in the auxiliary tank. As shown in Fig. 3.3(b), the auxiliary tank consists of MOS varactors, where the voltages at the drain/source and gate terminals of the varactor are denoted by V_{bias} and V_{tune}, respectively. The capacitors C_b in Fig. 3.3(b) behave as blocking capacitors to ensure stable biasing of the varactors. MOS varactors have been utilized for the fine tuning of the oscillation frequency in the proposed VCO. This is achieved by changing varactor capacitance with its gate-source voltage (V_{gs}).

3.3.2 Detailed Analysis for K_{VCO} and its variation

3.3.2.0.1 Consideration for low K_{VCO} Frequency of the proposed LC VCO topology shown Fig. 3.3(a) can be given by Eq. (3.6) given below

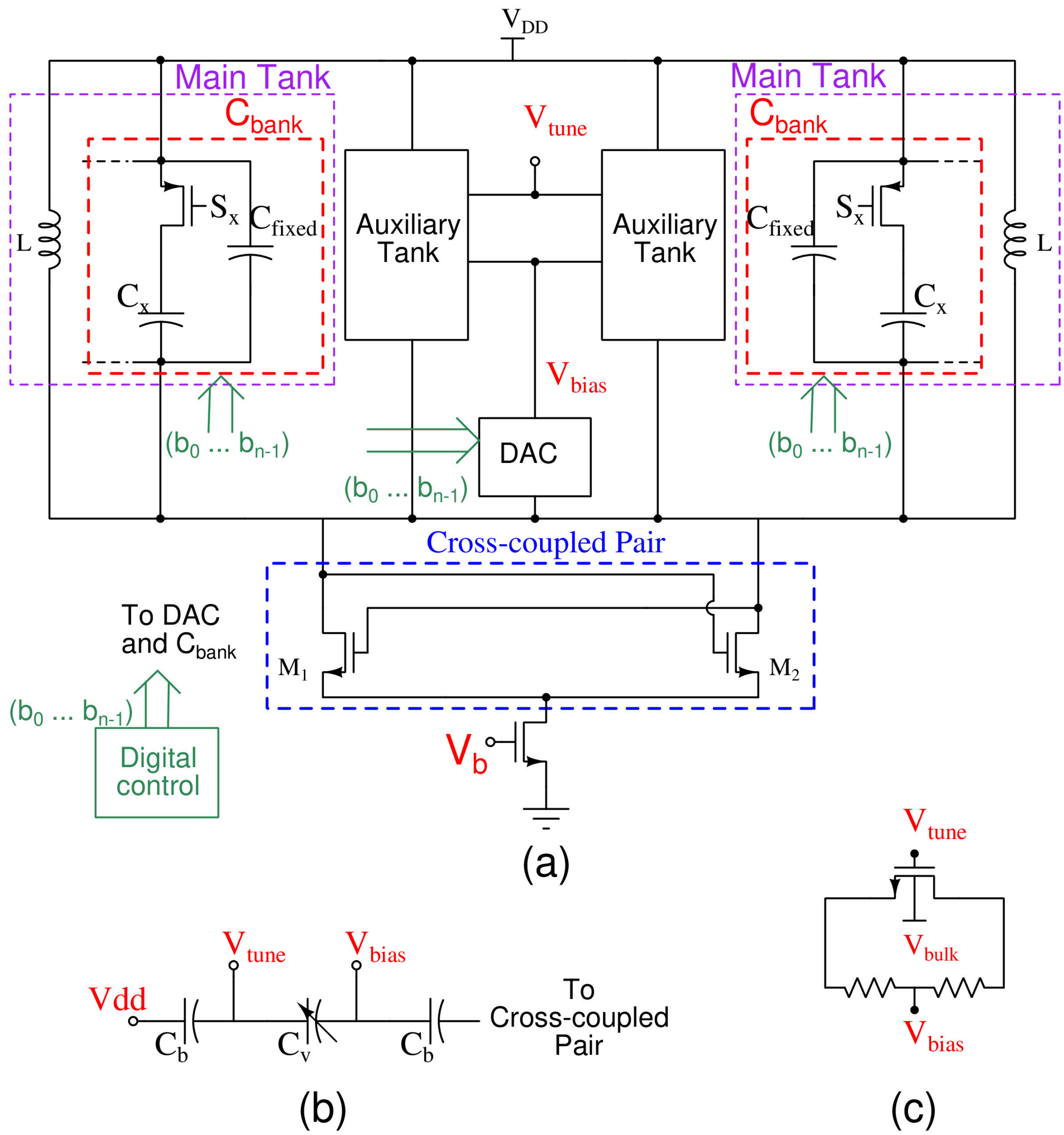


Figure 3.3: (a) Proposed LC Oscillator Topology (b) auxiliary tank structure and (c) structure of MOS varactor

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{3.6}$$

where, L is the total inductance of the circuit, and C represents the total capacitance of the circuit. In Eq. (3.7), C_{bank} and C_v represents the capacitance of the capacitor bank and capacitance of the MOS varactor, respectively.

$$C = C_{bank} + C_v \tag{3.7}$$

K_{VCO} can be reduced by reducing the change in oscillation frequency with respect to the control voltage of VCO, which requires a corresponding small change in MOS varactor capacitance. Since, C_v is proportional to its area, varactors with minimum area should be used for lower values of K_{VCO}. Moreover, size of cross-coupled pair should be large enough to give sufficiently high capacitance such that change in overall capacitance due to change in C_v is further minimized.

3.3.2.0.2 Analysis for K_{VCO} Variation This sub-section presents the complete theoretical analysis of reduced K_{VCO} variations in narrow tuning range with constant C_{bank} values as well as for wide tuning range with varying values of C_{bank}. For constant C_{bank}, change in frequency is affected only by change in capacitance of MOS varactor with the change in tuning voltage. The K_{VCO} of the circuit can be obtained by partially differentiating f_{res} with respect to control voltage, V_{tune}, to obtain the expression given in Eq. (3.8).

$$K_{VCO} = \frac{\partial f_{res}}{\partial V_{tune}} = -\frac{1}{4\pi\sqrt{L}(C_{bank} + C_v)^{1.5}} \times \frac{\partial C_v}{\partial V_{tune}} \tag{3.8}$$

Consider the MOS varactor in Fig. 3.3(c), which is similar in design to the MOS varactor used in the proposed LC VCO topology. The capacitance of the varactor is given by Eq. (3.9)

$$C_v = \frac{1}{\sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_{gs} - V_{fb})}{qN_a\epsilon_s}}} \tag{3.9}$$

where, V_{fb} is the flat band voltage of the device and V_{gs} is the gate to source voltage of the varactor, which is given by Eq. (3.10).

$$V_{gs} = V_{tune} - V_{bias} \tag{3.10}$$

For mathematical simplicity, the source voltage of this MOS varactor in Eq. (3.10) is assumed to be equal to V_{bias}, which is the mean value of source voltage. For further analysis, we define V_z as shown in Eq. (3.11).

$$V_z = V_{bias} + V_{fb} \tag{3.11}$$

Thus, the capacitance of varactor in Fig. 3.3(c) is obtained by substituting Eq. (3.10) and Eq. (3.11) in Eq. (3.9) to obtain the expression given in Eq. (3.12).

$$C_v = \frac{1}{\sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_{tune}-V_z)}{qN_a\epsilon_s}}} \tag{3.12}$$

where parameters C_{fb}, C_{ox} and V_{tune} represents the flat band voltage of the varactor, oxide capacitance per unit area of the varactor and tuning voltage respectively.

The partial differential of capacitance of MOS varactor with respect to the tuning voltage is obtained in Eq. (3.13).

$$\frac{\partial C_v}{\partial V_{tune}} = -\frac{1}{qN_a\epsilon_s} \times \frac{1}{(\frac{1}{C_{ox}^2} + \frac{2(V_{tune}-V_z)}{qN_a\epsilon_s})^{1.5}} \tag{3.13}$$

If the points where the difference between V_{tune} and V_z is high, Eq. (3.13) implies that the change in capacitance of MOS varactor with respect to change in tuning voltage is low, which decreases the K_{VCO} variation, but these points will have low K_{VCO}, resulting in very low tuning range. There is a clear tradeoff between tuning range and K_{VCO} variation. Tuning range is more preferred in this short frequency range and therefore, the selected operating points are chosen where the difference between V_{tune} and V_z is low, which will achieve significant tuning range with bearable K_{VCO} variation.

The proposed design methodology attains moderate K_{VCO} variation in a short frequency range, but as larger tuning ranges are required in most applications involving PLLs to ensure locking and reasonable settling times, the VCO makes use of a variable C_{bank} whose values can be switched to obtain outputs in different frequency bands. For an operating point which has a low value of output oscillation frequency, the value of C_{bank} should be high. Eq. (3.8) shows that the value of K_{VCO} is low at these operating points. Likewise, for an operating point with a high value of oscillation frequency, the K_{VCO} value will be high. By substituting Eq. (3.13) in Eq. (3.8), the expression of K_{VCO} is obtained as given by Eq. (3.14).

$$\begin{aligned} K_{VCO} = \frac{1}{4\pi \times N_a\epsilon_s\sqrt{L}} \times \frac{1}{(\frac{1}{C_{ox}^2} + \frac{2(V_{tune}-V_z)}{qN_a\epsilon_s})^{1.5}} \\ \times \frac{1}{(C_{bank} + C_v)^{1.5}} \end{aligned} \tag{3.14}$$

We define the term $Var_{K_{VCO}}$ as given by Eq. (3.15), which is derived from Eq. (3.14) by removing all constants and some simplifications.

$$Var_{K_{VCO}} = (C_{bank} + C_v) \times \left(\frac{1}{C_{ox}^2} + \frac{2(V_{tune} - V_z)}{qN_a\epsilon_s} \right) \tag{3.15}$$

Eq. (3.15) gives important insight on reducing K_{VCO} variation. As it can be seen from Eq. (3.15), if all the parameters are constant except C_{bank}, $Var_{K_{VCO}}$ will have large variation throughout the tuning range, i.e., K_{VCO} variation will be pretty high, i.e., for a low value of C_{bank}, value of K_{VCO} will be high and for a high value of C_{bank}, value of K_{VCO} will be low. The proposed methodology is to change the value of V_{bias} with change in C_{bank} such that the term $Var_{K_{VCO}}$ is constant, i.e., K_{VCO} has reduced variation. For example, if we have an operating point where the oscillator has a high value of C_{bank}, a high value of V_{bias} is used, i.e., low value of $V_{tune} - V_z$, resulting in a high K_{VCO} value. Similarly, for an operating point with a low value of C_{bank}, low value of V_{bias} is used to achieve low K_{VCO}. We propose to control C_{bank} and V_{bias} simultaneously to reduce K_{VCO} variation.

3.4 Design Implementation and Simulation Results

3.4.1 VCO Implementation

Fig. 3.4(a) shows the complete schematic of the proposed LC VCO with low K_{VCO} variation, which has been implemented in 0.18μm 6-metal layer CMOS technology. Fig. 3.4(b) shows the layout of the VCO, which occupies an area of 421.52 μm x 346.34 μm. As shown in the Fig. 3.4(a), oscillator core is implemented with a cross-coupled pair and the tank has been realized with capacitor bank containing total 16 unit capacitance (C_x), inductor (L), MOS varactors (C_V) and blocking capacitances (C_b). The capacitor banks (C_{bank}) are placed parallel to the inductors (L) to get shifts in the output frequency and produce a wide band of overall output frequencies. The fixed capacitance has been realized using a MIM capacitor (C_{fixed}) and has a value of 1.09 pF, while each unit capacitance was realized using a combination of MIM capacitors and has an effective value of 20 fF. A 16-bit digital control signal is used to control this operation and the switches used in the capacitor bank are PMOS switches. C_b is taken to be of the order pF while C_v is of the order 10 fF. The blocking capacitors (C_b) are MIM capacitors of value 1.15 pF used to provide stable bias voltage to the varactor. The resistances (R) are current limiting resistors of 1 kΩ used to limit the current from the control sources. The MOS varactors

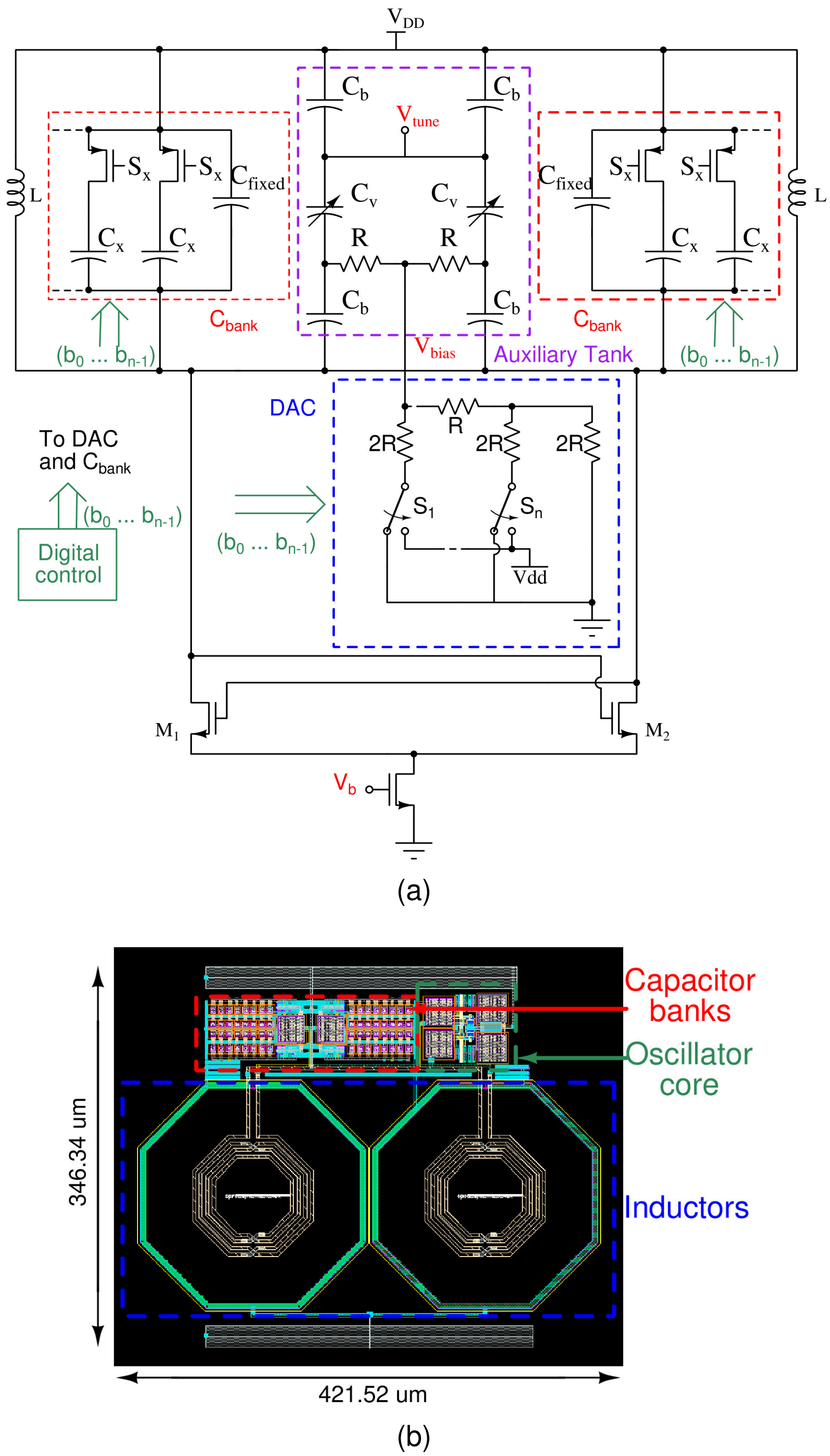


Figure 3.4: (a) Schematic and (b) layout of the proposed LC VCO with low K_{VCO} variation

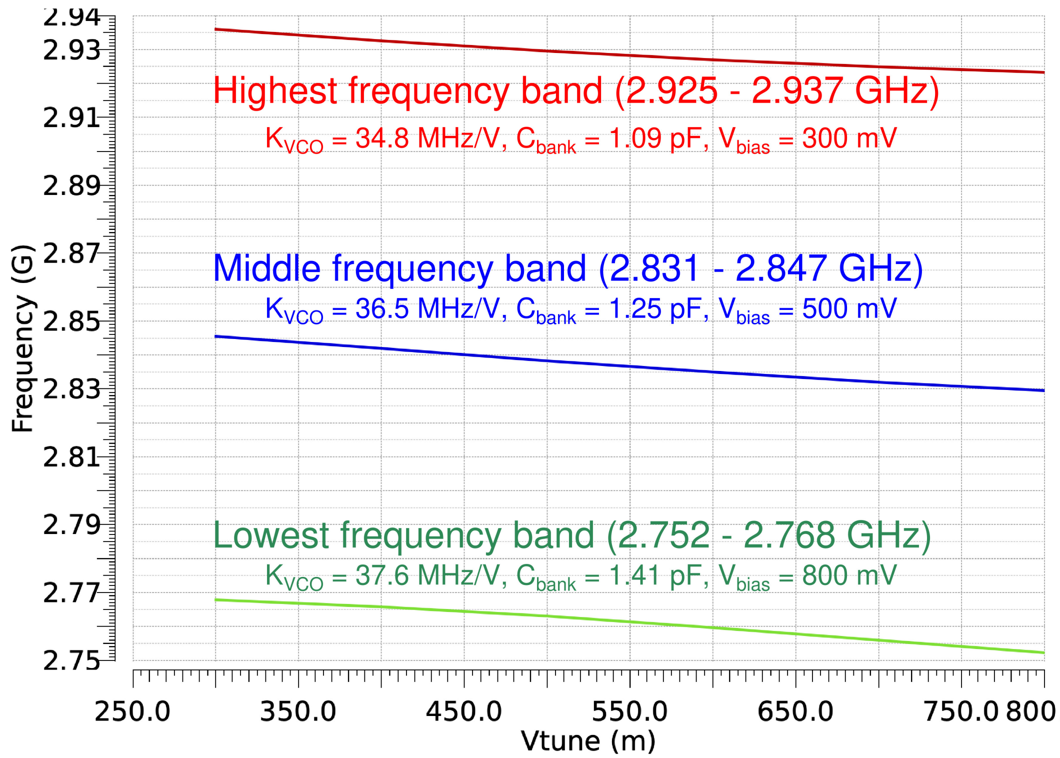


Figure 3.5: Variation of VCO output frequency and peak K_{VCO} values with V_{tune} for a lowest, highest and middle band

used are minimum sized for attaining low K_{VCO} and have a variable capacitance value in the range 21.87 fF - 61.88 fF. The inductors used are symmetric spiral inductors with a quality factor of 5.59.

V_{bias} is controlled by using DAC [11] whose input is the same 16-bit digital control signal controlling the C_{bank}. These two components are used in conjecture to minimize the variations in K_{VCO}, where V_{bias} changes according to the change in C_{bank} values.

3.4.2 Simulation Results

This subsection presents the post-layout simulation results of the proposed design shown in Fig 3.4(a), which has been implemented in 180nm CMOS process. The proposed VCO consumes 5 mA current from a 1.8 V supply. V_{tune} is swept from 300 mV to 800 mV and the output is taken at one of the cross coupled pair gates. Fig. 3.5 shows the variation of VCO frequency for the lowest (near 2.75 GHz), highest (near 2.94 GHz) and center (near 2.83 GHz) frequency bands. Simulation results shown in Fig. 3.5 depicts that the VCO tuning range is 190 MHz (2.75 - 2.94 GHz) around 2.87 GHz center frequency with K_{VCO} variation in each band is $<$ 20 MHz/V. We also observed a decrease in the tuning

$\mathbf{C_{bank}}$ **(pF)**	$\mathbf{V_{bias}}$ **(V)**	**Tuning Range (GHz)**	**Peak** $\mathbf{K_{VCO}}$ **(MHz/V)**	$\mathbf{K_{VCO}}$ **at 550mV** $\mathbf{V_{tune}}$ **(MHz/V)**
1.09	0.3	2.925 - 2.937	34.842	26.229
1.11	0.3	2.912 - 2.925	35.106	26.259
1.13	0.3	2.898 - 2.911	35.375	25.960
1.15	0.4	2.887 - 2.902	36.304	30.720
1.17	0.4	2.877 - 2.892	36.406	30.679
1.19	0.4	2.864 - 2.878	36.482	30.594
1.21	0.5	2.853 - 2.869	36.647	34.162
1.23	0.5	2.841 - 2.857	36.466	34.513
1.25	0.5	2.831 - 2.847	36.526	34.557
1.27	0.6	2.819 - 2.836	36.527	36.351
1.29	0.6	2.807 - 2.824	36.671	36.499
1.31	0.6	2.796 - 2.813	36.752	36.639
1.33	0.7	2.788 - 2.805	36.939	36.301
1.35	0.7	2.777 - 2.794	37.194	36.491
1.37	0.7	2.766 - 2.783	37.357	36.635
1.39	0.8	2.761 - 2.776	37.452	32.973
1.41	0.8	2.752 - 2.768	37.613	32.955

.

Table 3.1: VCO tuning ranges and corresponding K_{VCO} values

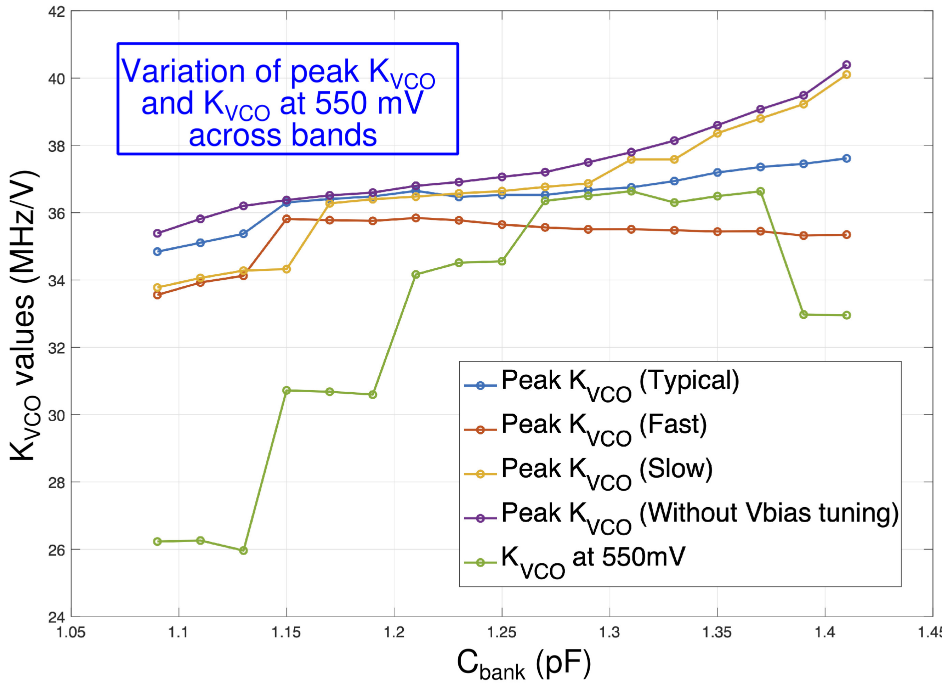
range from 2.85 GHz - 3.12 GHz from schematic simulation to 2.75 GHz - 2.94 GHz in post-layout simulations. Table 3.1 presents the VCO frequency bands with varying C_{bank} and corresponding V_{bias} values along with the peak K_{VCO} and K_{VCO} at tuning voltage of 550 mV where the peak K_{VCO} is the highest K_{VCO} value seen for a particular combination of C_{bank} and V_{bias}. K_{VCO} variation shown in Table 3.1 is also plotted in Fig. 3.6(a), which shows that variation in K_{VCO} of 3.82%. Fig. 3.6(a) also depicts the degradation of the K_{VCO} variation to 6.57% without a significant increase in tuning range when V_{bias} tuning is disabled and the K_{VCO} variation across process corners with the slow process corner variation of 8.57%. This is a significant improvement in K_{VCO} variation reduction as compared to other related works, which demonstrate a variation in the range of 40 MHz/V - 600 MHz/V [5] - [10]. Fig. 3.6(b) shows the variation in phase noise at 1 MHz offset with the change in C_{bank} values.

Minimum phase noise of -118.638 dBc/Hz is obtained for 1.1 pF value of C_{bank}, which corresponds to the highest frequency range (near 2.94 GHz). As shown in Fig. 3.6(b), phase noise degrades as the capacitance is increased, which is expected due to the increased losses in C_{bank} switches. Fig. 3.7 shows the variation in phase noise performance considering all the active and passive components across the different process corners for minimum C_{bank} value. As shown in the figure, phase noise at 1 MHz offset at 2.94 GHz center frequency is < -117 dBc/Hz across the corners.

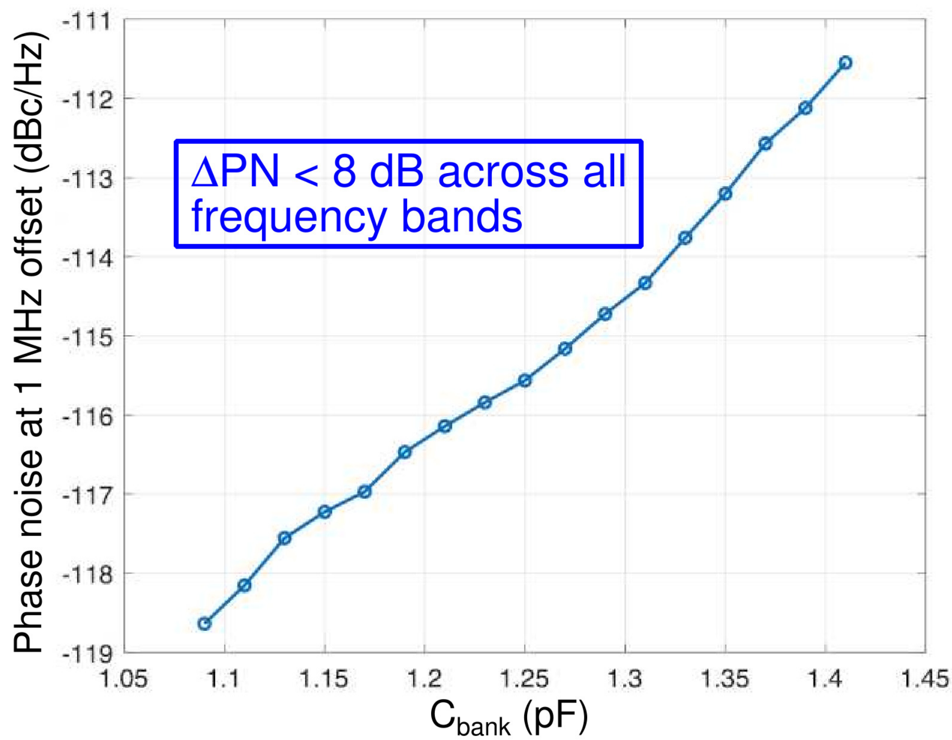
Table 3.2 presents the performance summary and comparison of the proposed design with other recently reported work. As shown in the table, K_{VCO} variation is minimum in the proposed VCO as compared to the other works. Moreover, phase noise is also better as compared to the other works. Our design has a low tuning range compared to others as our proposed architecture is aimed at low K_{VCO} design specific for NV magnetometry, where reduced tuning range is desirable. There is a clear trade-off between the tuning range, K_{VCO} value and power consumption. For lower K_{VCO}, the tuning range decreases. However, the overall tuning range of the VCO can be increased by using a bigger capacitor bank with more unit capacitance as per the requirement, which will consume more power. For a fair comparison of VCO performance considering the K_{VCO} variations (ΔK_{VCO} in %), we propose a new figure-of-merit (FoM), which is shown in Eq. (3.16).

$$FoM = \frac{\left(\frac{f_0}{\Delta f}\right)^2}{P_{DC} \times PN \times \Delta K_{VCO}(\%)} \tag{3.16}$$

As shown in table 3.2, FoM of the proposed design is significantly higher than the other designs except [8] which has higher FoM owing to its exceptionally low power consumption at lower technology node.



(a)



(b)

Figure 3.6: (a) K_{VCO} variation across frequency bands (b) Phase noise variation across frequency bands

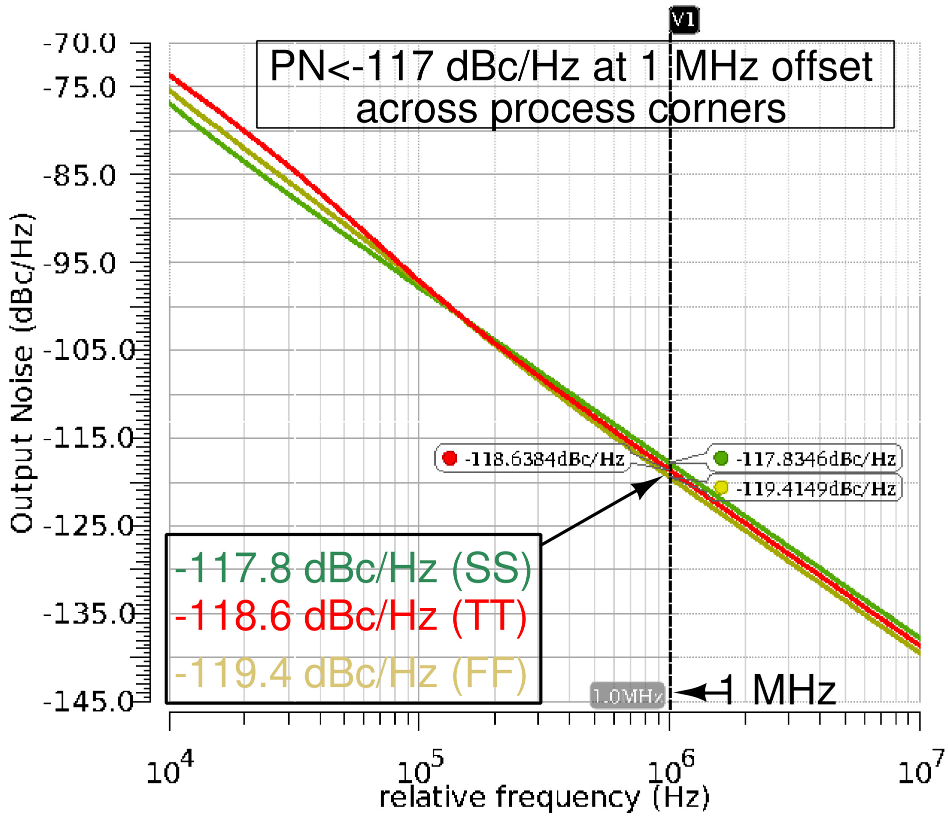


Figure 3.7: Phase noise variation across process corners

Ref.	[5]	[6]	[7]	[8]	[9]	[10]	Our Work
Technology	90 nm CMOS	180 nm CMOS	65 nm CMOS	110 nm CMOS	180 nm CMOS	130 nm CMOS	180 nm CMOS
VCO Type	LC VCO	LC VCO	LC VCO	LC VCO	Ring VCO	Ring VCO	LC VCO
Freq. (GHz)	24.1-28.2	4.39-5.26	1.51-3.01	1.73-2.56	1.78-2.53	0.36-11.9	2.75 - 2.94
K_{VCO} Variation (%)	±16	±9.56	±49.5	±8.60	±2.81 (TR†= 580 MHz) ±7.01 (TR†= 750 MHz)	±61.64	±3.82
Phase Noise (dBc/Hz @ 1MHz)	-103	-113.7	-115.1	-116.4	-92.68	-103.3	-118.64
Power (mW)	26	9.7	1.02	0.76	28	37.5	9
FoM (dBc/Hz)‡	165.81	168.45	167.64	176.41	141.78	151.17	172.44

†Tuning range, ‡Proposed FoM (Eq. (3.16)) to include effect of K_{VCO} variation on VCO performance.

Table 3.2: Performance summary and comparison with similar works

3.5 Summary

This chapter presented a technique to design an LC VCO with low gain and reduced gain variation, which are often needed in highly sensitive quantum sensing applications. A new FoM has been also defined in this work to capture the effect of K_{VCO} variations on VCO performance. The proposed LC VCO is designed in 180 nm CMOS technology. Post layout simulation results show that it consumes 5 mA current from 1.8 V supply and exhibits a phase noise and FoM of -118.64 dBc/Hz and 172.44 dBc/Hz, respectively at 1 MHz offset at center frequency of 2.94 GHz. The proposed LC VCO achieves a tuning range of 2.75 - 2.94 GHz and exhibits low K_{VCO} (< 38 MHz/V) with low K_{VCO} variation (< 20 MHz/V) of 3.82%, which are much better than the other previously reported works.

Chapter 4

Design of 2.87 GHz Frequency Synthesizer with Programmable Sweep for Diamond Color Defect based CMOS Quantum Sensing Applications

4.1 Introduction

Quantum sensing has a wide array of applications in material science, mesoscopic physics and life science. Nitrogen-Vacancy (NV) centre in diamond behaves as an isolated electronic spin system that can be used in quantum sensors [2]. When a vacancy replaces the adjacent carbon pair in a diamond lattice, the nitrogen atom and the vacancy form an NV centre. The NV defect has its ground level in a spin triplet state whose sub-levels are split in energy into a singlet ($m_s = 0$) and a doublet of degenerate levels ($m_s = \pm 1$) separated by 2.87 GHz [3]. When an external magnetic field is applied on the NV ground state spin triplet, a Zeeman shift of energy $\gamma_e B_z$ is induced, where B_z represents the magnetic field component along the NV symmetry axis. As shown in Fig. 4.1(a), optically detected magnetic resonance (ODMR) technique can be used in NV-based sensing to measure static or slow varying $|\vec{B_z}|$ [2], [3]. In ODMR, NV electron spin transitions are excited by a microwave signal (f_{RF}) near 2.87 GHz and diamond is irradiated with a green light, which produces a red light proportional to $|\vec{B_z}|$ and having photon frequency Δf_p given in Eq. (4.1) [2], which is detected using a photo-diode.

$$\Delta f_p = f_+ - f_- = 2\gamma_e |\vec{B_z}| \tag{4.1}$$

In Eq.(4.1), γ_e is gyromagnetic ratio (28 GHz/T) and f_+ and f_- are the transition frequencies from the singlet level to the doublet levels. Usually, NV-ODMR is detected with lock-in technique for which f_{RF} is frequency modulated (f_m) while using an external source [2], [3]-[13]. The sensitivity of measured $|\vec{B_z}|$ can be improved with reduced f_m, which results into lower Δf_p as given in Eq. (4.1). Moreover,

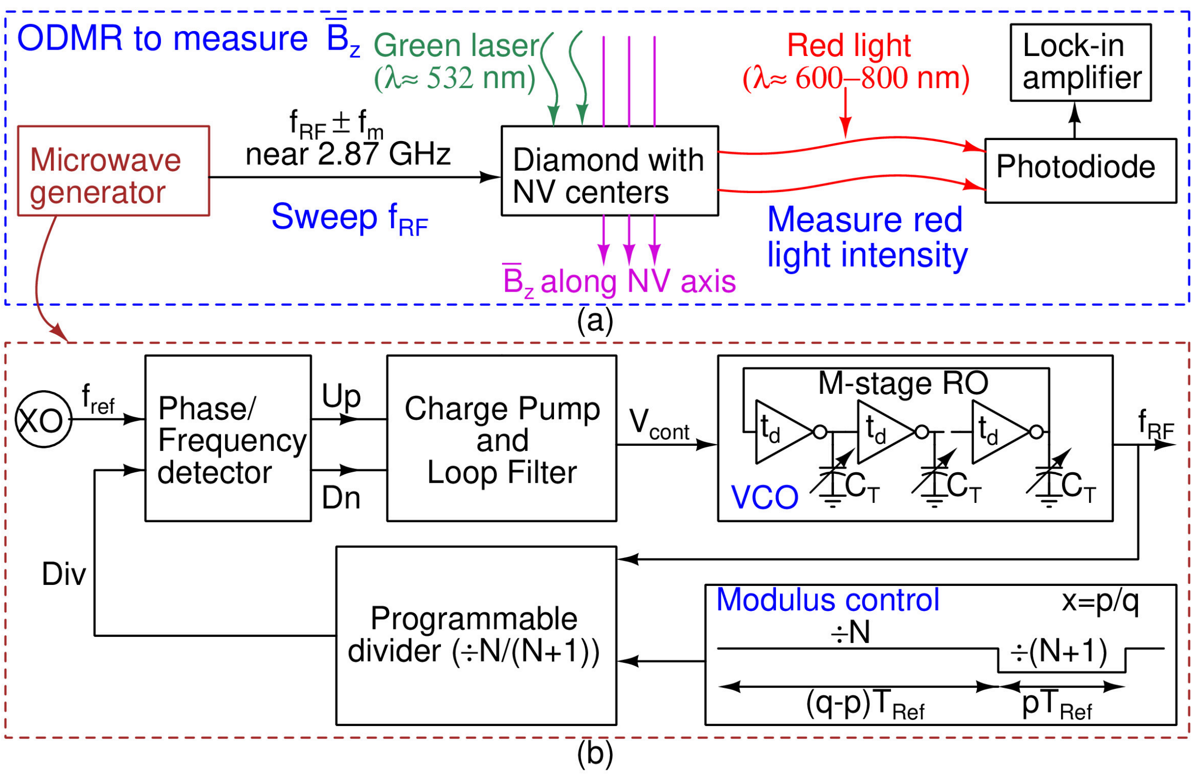


Figure 4.1: (a) Depiction of NV-ODMR to measure magnetic field strength ($|\vec{B}_z|$) and (b) Fractional-N synthesizer as microwave signal generator

overall power can also be reduced by having on-chip frequency sweep than using the external frequency modulator.

Towards achieving the goal of the improved sensitivity for $|\vec{B_z}| < 1\ \mu$T measurement in NV-based quantum sensing applications with reduced power consumption, in this chapter, I present - 1) design of a 2.87 GHz MWG with a programmable sweep-step size of 50 kHz, 2) it's implementation in 180 nm CMOS technology and 3) post-layout simulation results to validate the MWG design. As compared to the previous works [2]-[13], this research presents MWG with on-chip programmable frequency sweep for NV-ODMR for the first time, which not only helps in improving $|\vec{B_z}|$ sensitivity but also aids in generating and delivering a homogeneous magnetic field in CMOS quantum sensors by removing the signal loss and reflections at interface, which are otherwise inevitable in conventional off-chip source solutions. The chapter is organized as follows: Sections 4.2 and 4.3 present the architecture overview and detailed design of the proposed MWG, respectively. Section 4.4 presents post-layout simulation results followed by the conclusion in Section 4.6.

4.2 Architecture Overview and Design Considerations

4.2.1 Architecture overview

From Eq. (4.1), to detect $|\vec{B_z}| < 1\ \mu$T, Δf_p of 56 kHz is needed, which requires that MWG signal should be varied near 2.87 GHz with a resolution <56 kHz. For this, as shown in Fig. 4.1(b), a phase-locked loop (PLL) based fractional-N frequency synthesizer has been presented in this work, which contains a crystal oscillator (XO) to generate reference signal (f_{ref}), phase/frequency detector (PFD), a charge pump (CP), a loop filter (LPF), a voltage controlled oscillator (VCO) and a programmable divider. Important considerations of MWG design are discussed in the following subsection.

4.2.2 Design considerations

4.2.2.0.1 Low gain VCO For $< 1\ \mu$T sensitivity, VCO shown in Fig. 4.1(b) should be able to achieve frequency resolution (Δf) of 50 kHz with low phase noise while providing a sufficiently wide tuning range. For low frequency resolution, the gain of the VCO (K_{VCO}) can be estimated by Eq. (4.2)

$$\Delta f = K_{VCO} \times \Delta V_{cont} \tag{4.2}$$

where, ΔV_{cont} is the change in control voltage at VCO input. Very small values (few 100's μV) of ΔV_{cont} are more prone to noise, whereas larger values (10's of mV) will require extremely low K_{VCO}. Considering this, a value of 1 mV is considered for ΔV_{cont}, which requires a VCO with $K_{VCO} =$ 50 MHz/V at $f_{RF} =$ 2.87 GHz. To achieve this low K_{VCO} requirement, there are two choices for the VCO realization - 1) LC VCO or 2) ring VCO with CMOS inverters. LC VCO choice results in increased chip area and possibility of degradation of field homogeneity in the sensing area [2] due to the magnetic coupling between on-chip inductor and $|\vec{B_z}|$. Therefore, as shown in Fig. 4.1(b), an M-stage ring oscillator (RO) topology is chosen in the proposed work, for which, oscillation frequency (f_{RF}) can be given by Eq. (4.3).

$$f_{RF} = \frac{1}{2Mt_d} \tag{4.3}$$

In Eq. (4.3), t_d ($\propto C_T$) is the delay of each stage, where C_T is the total capacitance at each node. Gain of the ring VCO can be expressed by Eq. (4.4) given below.

$$|K_{VCO}| = \frac{\partial f_{RF}}{\partial V_{cont}} = \frac{1}{2Mt_d^2}\frac{\partial t_d}{\partial V_{cont}} = 2Mf_{RF}^2\frac{\partial t_d}{\partial V_{cont}} \tag{4.4}$$

Eq. (4.4) gives important insights about designing low gain ring VCO - 1) by minimizing M and 2) by making C_T a weaker function of V_{cont} to reduce $\frac{\partial t_d}{\partial V_{cont}}$.

4.2.2.0.2 Programmable divider In order to obtain a resolution of Δf near f_{RF}, the divider must divide by $(N+1)$ for a fraction x of the cycles of reference signal having frequency f_{ref} and divide by N for the remaining cycles, which are related as shown in Eq. (4.5) [4].

$$f_{RF} + \Delta f = (N + x)f_{ref} \tag{4.5}$$

Using Eq. (4.5), under locked condition ($f_{RF} = N \times f_{ref}$), $x = \frac{\Delta f}{f_{ref}}$. As depicted in Fig. 4.1(b), a modulus control signal is generated by considering $x = \frac{p}{q}$, where p and q are the number of total reference cycles and number cycles for which the modulus signal is low, respectively. This modulus control signal programs the divider for fractional-N operation and switches the center frequency of the VCO. Very low f_{ref} will require high N resulting into more area and dynamic power consumption, whereas very high f_{ref} will make x too small, which will require more number of reference cycles for fractional-N operation. Considering these points, we chose $f_{ref} \approx$ 90 MHz, which gives N=32.

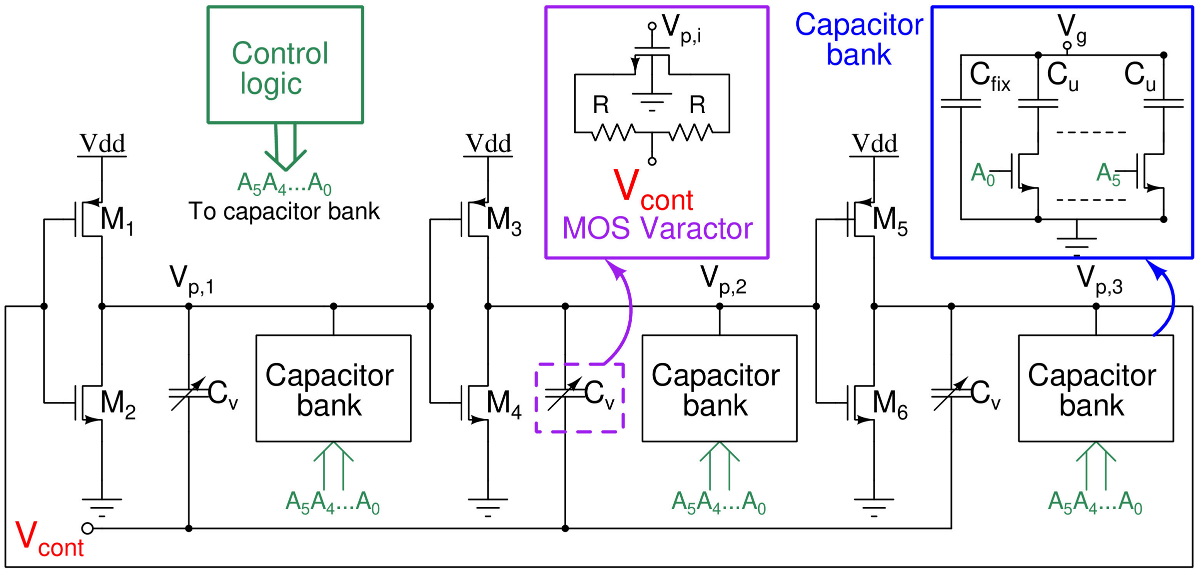


Figure 4.2: VCO schematic for the proposed MWG

4.3 Design Implementation

This section of the paper elucidates the design details of different modules of the proposed MWG.

4.3.1 Low gain ring VCO design

Fig. 4.2 depicts the proposed ring VCO. As suggested in section-4.2, the proposed VCO uses the minimum number (M=3) of CMOS inverter stages with varactor and a capacitor bank at each node. As shown in the figure, each capacitor bank contains a fix capacitance (C_{fix}) and parallel combination of 6 unit capacitance (C_u), which are realized using MIM capacitors. C_u is used for the coarse tuning of the VCO and is controlled by a 6-bit signal ($A_5 \ldots A_0$), which is generated by the control logic shown in the figure. MOS varactors are controlled by V_{cont} and facilitate the finer tuning of f_{RF} [14]. Varactors with minimum size have been used for having the least value of $\frac{\partial t_d}{\partial V_{cont}}$ for low K_{VCO} as shown in Eq. (4.4). In the proposed VCO design, A_0 is connected to supply, A_2, A_3, A_4 and A_5 are connected to ground while A_1 is connected to the modulus control signal. The capacitor bank MIM capacitors sizes are selected such that two bands are centered at 2.87 GHz and 2.87+f_{ref} GHz and the other bands are such that the overall tuning range is maximized near 2.87 GHz.

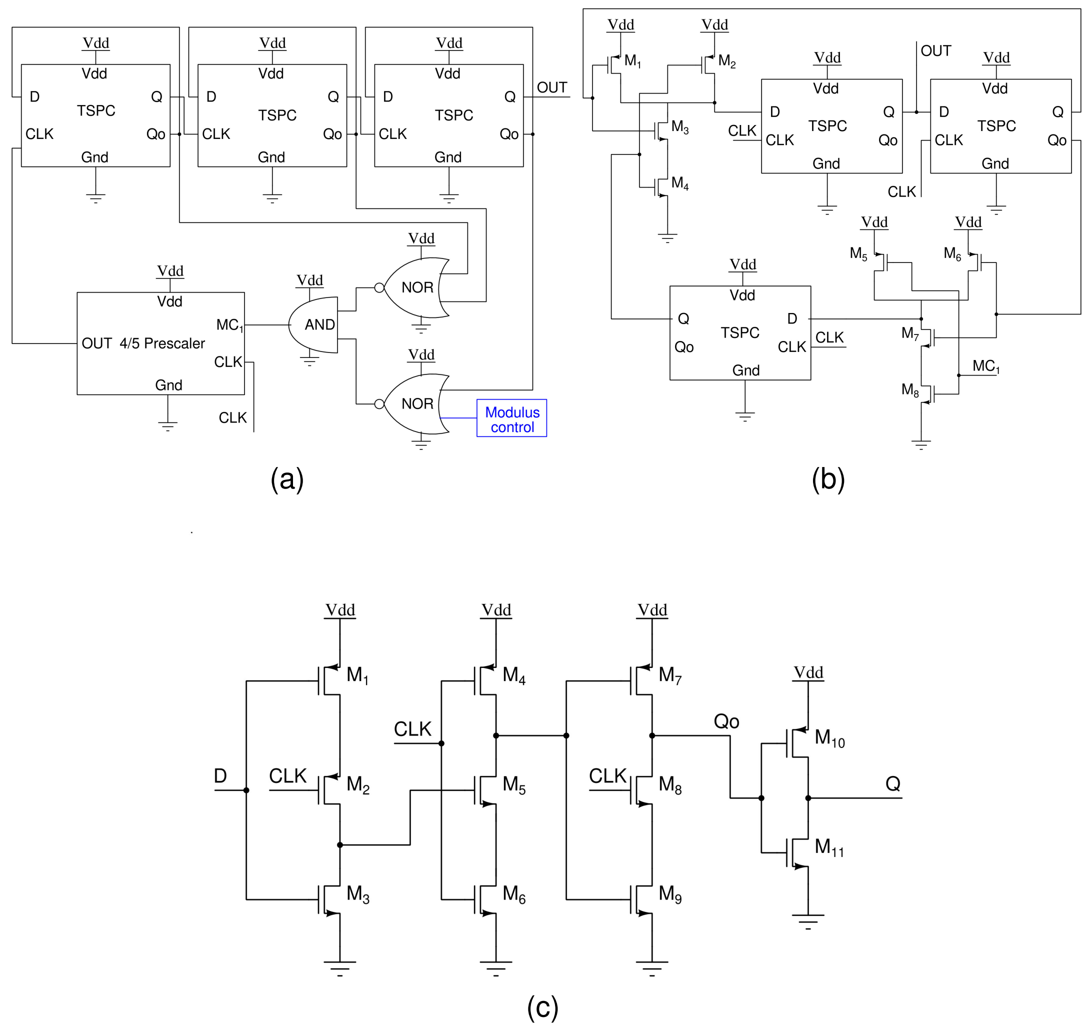


Figure 4.3: Schematic of the (a) programmable divider for the proposed MWG, (b) 4/5 prescaler used in the divider and (c) TSPC D flip flop (divide by 2 unit)

4.3.2 Frequency Divider

As shown in Fig. 4.3(a), the programmable divider of the proposed MWG consists of three True Single-Phase Clock (TSPC) D flip-flops and a 4/5 prescaler that clocks the TSPC stages controlled by MC_1 which is NOR of the input of each of the TSPC stages and the modulus control signal[15]. Each TSPC stage acts as divide by 2 unit. The 4/5 prescaler shown in Fig. 4.3(b) consists of TSPC stages and the required NAND logic to switch between divide by 4 and 5 based on MC_1. Fig. 4.3(c) shows the schematic of the TSPC logic based D flip flops used in Fig. 4.3(a) and Fig. 4.3(b) [16].

Control Signal	Tuning Range (GHz)	$\mathrm{K_{VCO}}$ (MHz/V)
000000	2.994 - 3.069	51.666
000001	2.916 - 2.987	49.177
000011	2.842 - 2.909	46.769
000111	2.744 - 2.807	43.760
001111	2.659 - 2.718	41.172
011111	2.584 - 2.640	38.943
111111	2.515 - 2.568	36.927

The K_{VCO} values mentioned are the maximum values.

Table 4.1: VCO tuning ranges and corresponding K_{VCO} values form post-layout simulations

4.3.3 PFD/CP/LPF/XO

Fig. 4.4(a) shows the block diagram of the PFD, which consists of two D-flip-flops and an AND gate [17]. The two flip-flops shown in Fig. 4.4(a) have their inputs connected to supply and clocked by the reference signal (f_{ref}) and divider output (Div), respectively. They generate the Up and Down pulses for driving the charge pump (CP) according to the phase difference in the reference and divider output signals [4]. Fig. 4.4(b) shows the topology used to realize CP based on the dynamic current-matching technique, which minimizes current mismatches by using additional feedback transistors that compensate for the channel length modulation [18]. As shown in figure, the loop filter comprised of R_1, C_1 and C_2 [17]. Fig. 4.4(c) shows the pierce oscillator topology, which is used to realize the crystal oscillator to generate external reference in the proposed MWG [19].

4.4 Post Layout Simulation Results

Fig. 4.5 shows the layout of the proposed MWG in 180 nm CMOS technology, which occupies about 273μm $\times$ 152μm. Table 4.1 shows the values of post-layout simulated tuning ranges and K_{VCO} of the proposed ring VCO for different control signals. As shown in the table, the proposed VCO achieves an overall tuning range of 2.515 - 3.069 GHz and attains K_{VCO} <50 MHz/V near 2.87 GHz, which also facilitates the fractional-N operation for fine frequency sweeping.

As shown in Fig 4.6(a), the proposed VCO also achieves significantly low K_{VCO} <52 MHz/V across all tuning ranges shown in table 4.1. Moreover, as shown in the figure, variation in K_{VCO} values across the bands is also very small (<16 MHz/V). Fig. 4.6(b) shows that the VCO phase noise at a 1 MHz offset near 2.87 GHz frequency $<$ -90.6 dBc/Hz across the process corners. Fig. 4.7(a) shows

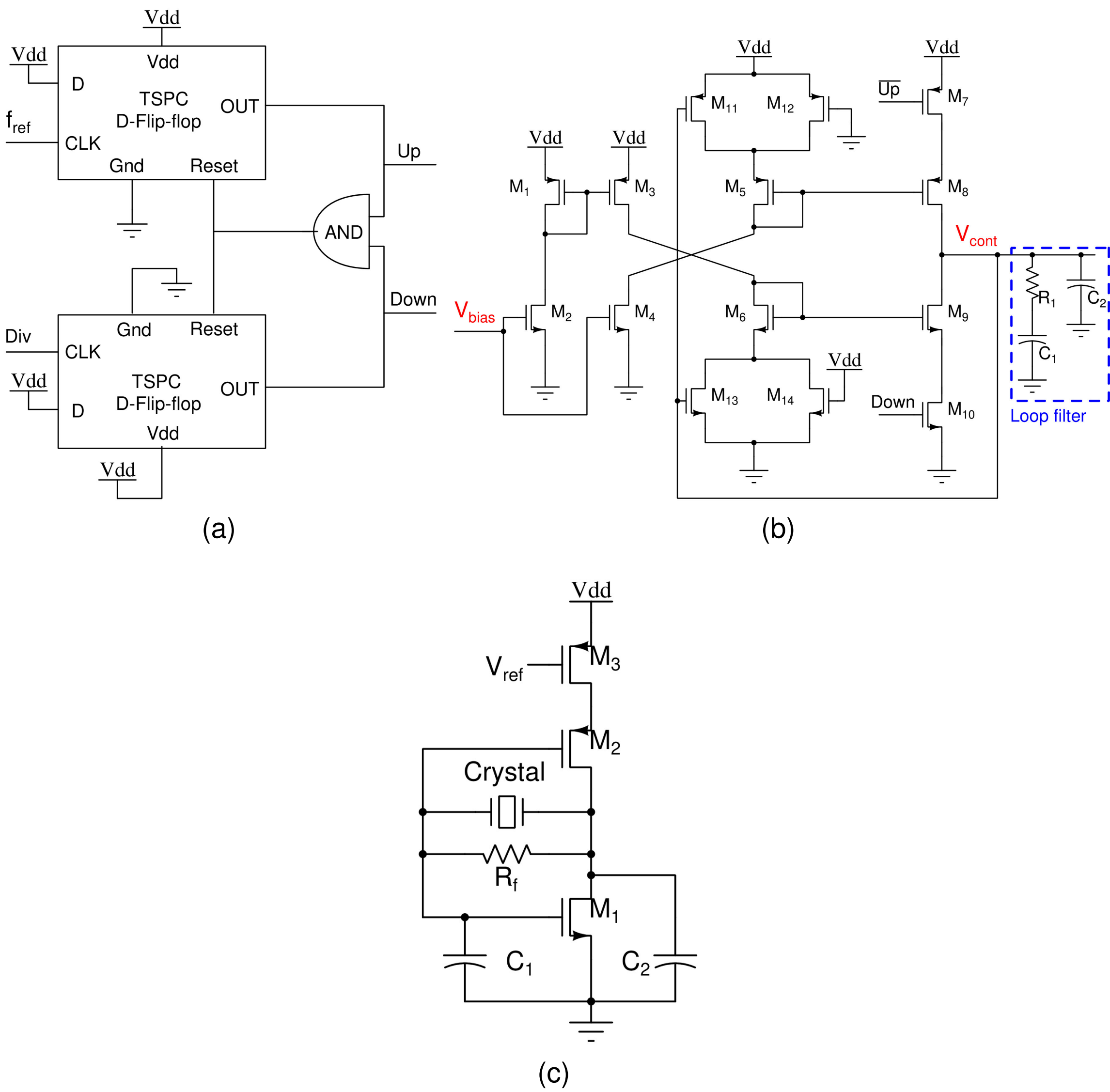


Figure 4.4: Schematic of (a) PFD, (b) current matching CP [18] and (c) XO

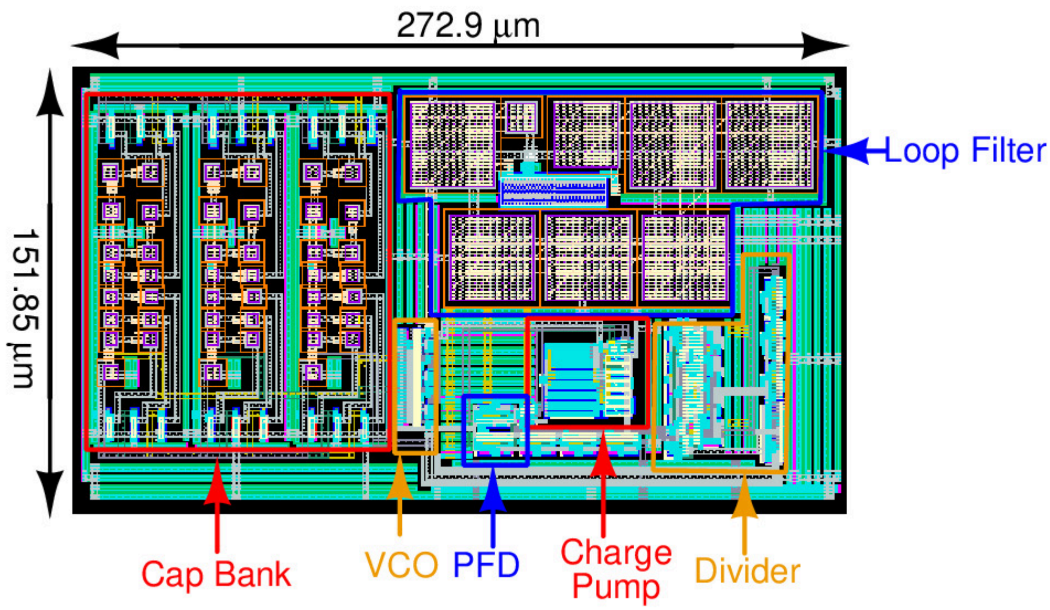


Figure 4.5: Layout of the proposed MWG in 180 nm CMOS technology

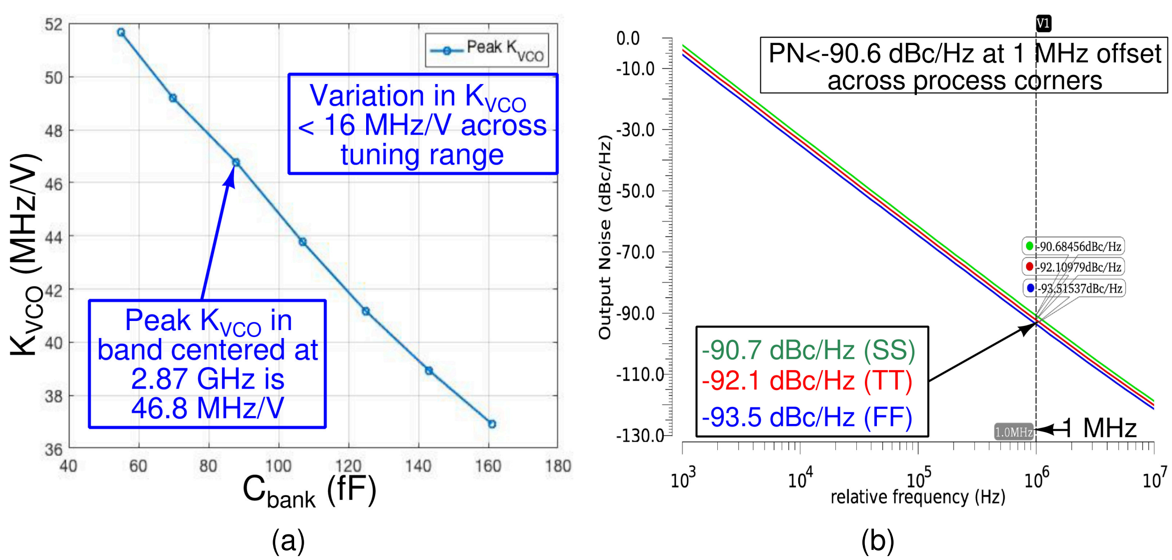


Figure 4.6: Post-layout simulation results showing (a) variation of K_{VCO} across entire tuning range of VCO and (b) VCO phase noise across process corners

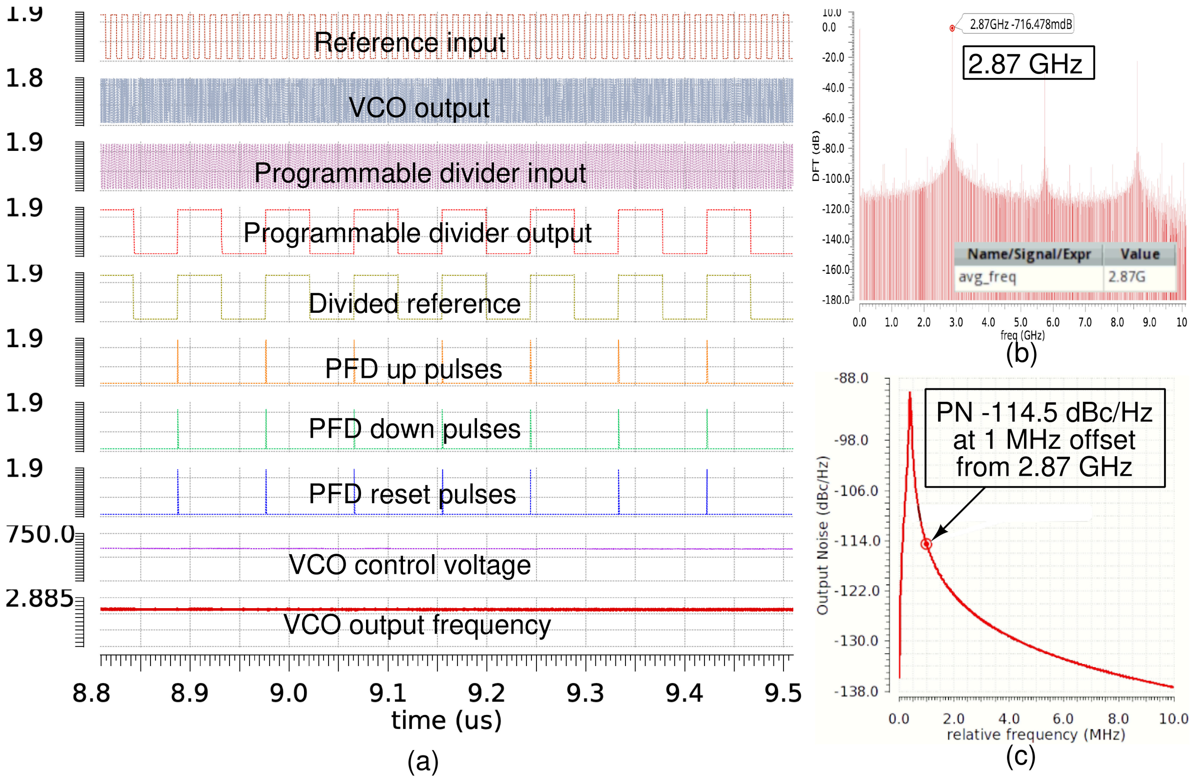


Figure 4.7: Post-layout simulation results showing (a) PLL signals in locked state (b) DFT of PLL output locked at 2.87 GHz and (c) PLL phase noise plot

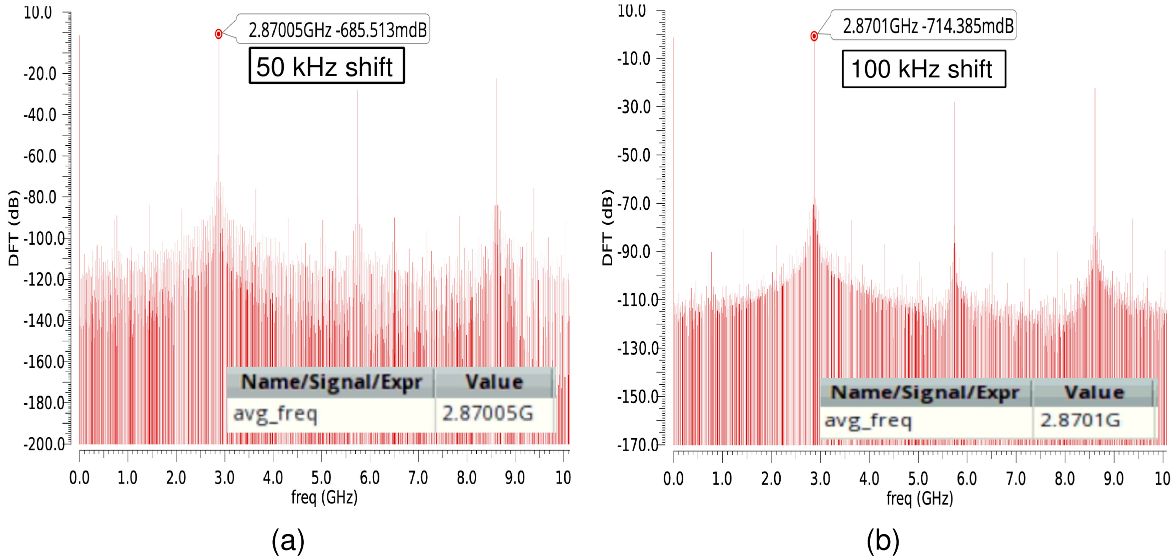


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Figure 4.8: Post-layout simulation results showing DFT plots for (a) 50 kHz shift and (b) 100 kHz shift from 2.87 GHz

the transient response of the proposed MWG in phase locked state. Fig. 4.7(b) presents the DFT plot showing $f_{RF} = 2.87$ GHz is synthesized by the proposed MWG. Fig. 4.7(c) shows that the phase noise of the 2.87 GHz MWG signal is -114.5 dBc/Hz at an offset of 1 MHz. The proposed MWG consumes about 11.14 mW of power from a 1.8 V supply.

To get a frequency shift of 50 kHz in $f_{RF} = 2.87$ GHz, modulus control of the divider is programmed for $x = \frac{4}{7175}$. Value of x implies that the programmable divider must divide by 33 for 4 cycles every 7175 cycles and divide by 32 for the remaining 7171 cycles. Similarly, $x = \frac{8}{7175}$ for 100 kHz shift. The time period (T) of the 89.6875 MHz crystal oscillator is 11.1498 ns, which gives timing information for the divide by 33 (N+1) control as $4\times$T and divide 32 (N) control as $7171\times$T. Similarly, for 100 kHz shift timing for divide by 33 and 32 control signals are $8\times$T and $7167\times$T, respectively. Fig. 4.8(a) and 4.8(b) show DFT plots for 50 kHz and 100 kHz shifts in $f_{RF} = 2.87$ GHz obtained using the corresponding modulus control signals, respectively. Table 4.2 presents the performance summary and comparison of the proposed design with other works. As shown in the table, proposed MWG achieves lower K_{VCO} and frequency resolution as compared to the other works while providing significant improvement in the magnetic field sensitivity.

Parameters	[2]	[3]	[12]	[13]	[20]	[21]	This Work
Simulated/Measured	Measured	Measured	Measured	Measured	Measured	Measured	Simulated
Technology	65 nm	65 nm	65 nm	65 nm	45 nm	45 nm	180 nm
Area (μm $\times$ μm)	80 $\times$ 300	50 $\times$ 50	80 $\times$ 300	800 $\times$ 500	320 $\times$ 300	300 $\times$ 100	273 $\times$ 152
PLL Type	Integer-N	Integer-N	Integer-N	Integer-N	Fractional-N	Fractional-N	Fractional-N
VCO Type	Ring with varactors	Ring with MOSCAP	Ring with MOSCAP	Ring with MOSCAP	Ring with varactors	Ring with varactors	Ring with varactors
Freq. Range (GHz)	2.87*	2.6 - 3.1	2.87*	2.6 - 3.1	2.31 - 3.05	2.3 - 2.6	2.5 - 3.1
Freq. Resolution (kHz)	1200$_\diamond$	100$_\diamond$	1200$_\diamond$	180$_\diamond$	740$_\diamond$	300$_\diamond$	50
Magnetic Field Sensitivity (μT)	13.42 $_\ddagger$	1243.23 $_\ddagger$	13.42 $_\ddagger$	2827.28 $_\ddagger$	6.77	5.36	0.89
Noise Bandwidth (kHz)	3	1.5	3	1.5	-	-	-
Ref. Freq. (MHz)	$\sim$90	$\sim$120	$\sim$100	$\sim$100	22.6	22.6	$\sim$90
K_{VCO} (MHz/V)	1200	100$_\dagger$	1200	180	740$_\dagger$	300$_\dagger$	50
Phase Noise (dBc/Hz)	-88 @ 3kHz	-90 @ 1.5kHz	-88 @ 3kHz	-90 @ 1.5kHz	-104 @ 1MHz	-109 @ 1MHz	-114 @ 1MHz
Supply Voltage (V)	2.5	2.5	2.5	2.5	1	1	1.8
Power (mW)	>12.5**	>12.5**	>12.5**	>12.5**	10	6.4	11.14

* Frequency range is not given so the given center frequency is mentioned. $_\diamond$ Calculated using the K_{VCO} value assuming 1mV steps in V_{cont}. $_\ddagger$ Reported 245 nT/$\sqrt{Hz}$, 32 μT/$\sqrt{Hz}$, 245 nT/$\sqrt{Hz}$ and 73 μT/$\sqrt{Hz}$ in the given noise bandwidth. $_\dagger$ The K_{VCO} values are calculated using the tuning range and control voltage range. ** Estimated using charge pump current and supply voltage values given.

Table 4.2: Performance summary of the proposed MWG and comparison with other works

4.5 Tapeout in SKY130

The SkyWater 130nm technology is a combined effort by Google and SkyWater. It is an open source PDK in its experimental preview phase with MPW mode fabrication. Fig. 4.9 summarises the technology node process and the pad frame/harness being used for the MPW shuttle program.

4.5.1 Area and Floorplan

Fig. 4.10 shows the area of the harness as well the dedicated user project ares. It also shows the proposed floor plan for the project.

4.5.2 Tapeout

Fig. 4.11 shows the schematic and layout representations of the individual modules included in the tapeout. Fig. 4.12 shows the layout of the complete MWG included in the tapeout. Fig. 4.13 shows the final floorplan and complete die layout for the tapeout. The submission was made in April 2022 to the 5th iteration of the Efabless Open MPW Shuttle Program and the packaged dies are yet to be delivered.

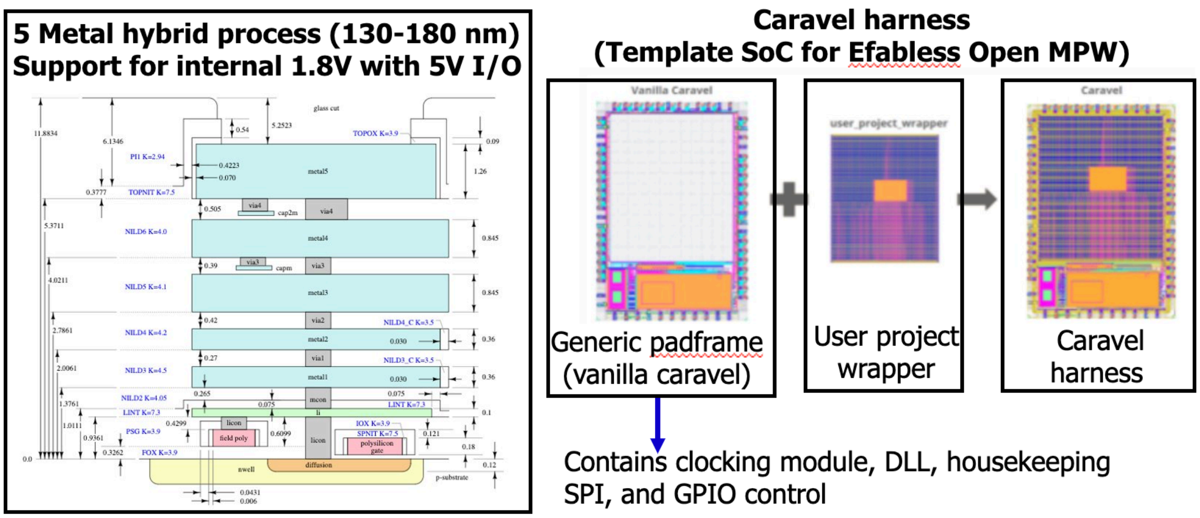


Figure 4.9: Diagrams showing the layers in the process and structure of caravel harness

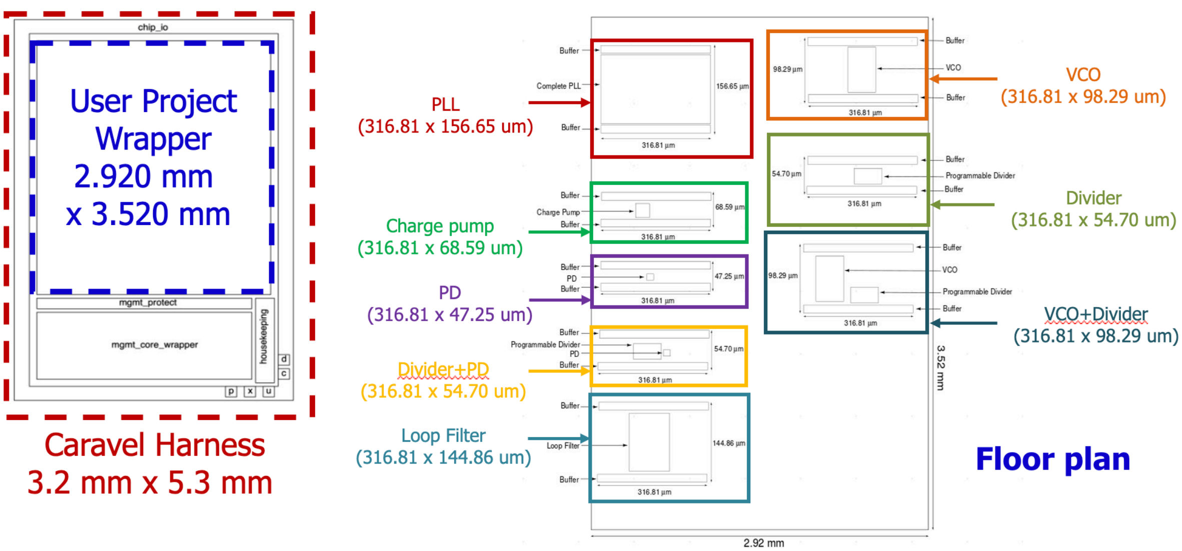


Figure 4.10: Area of the harness and user project along with floor plan for project

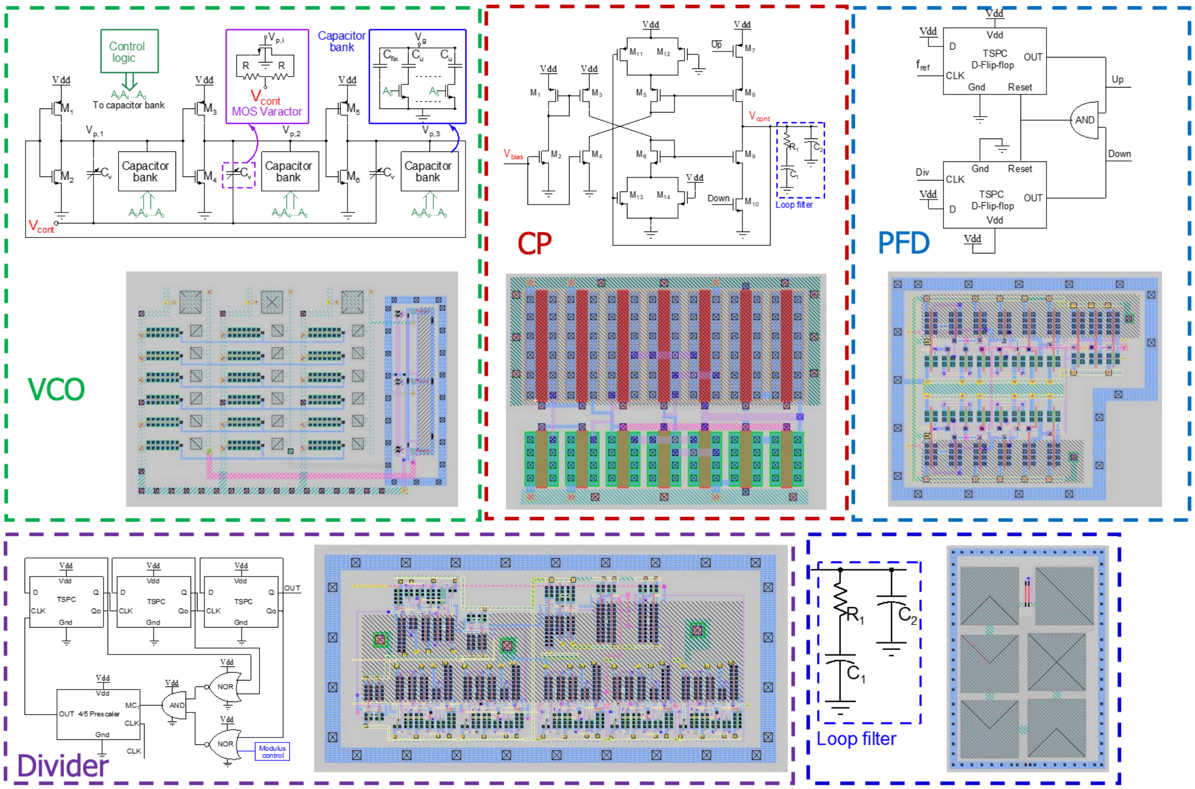


Figure 4.11: Schematic and layout of individual modules for tapeout

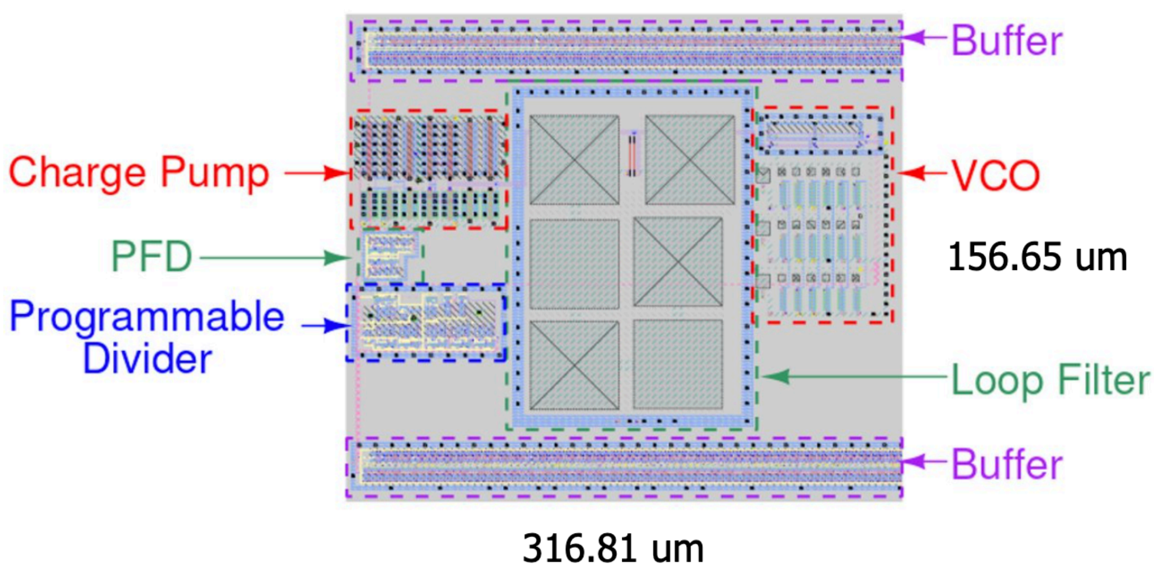


Figure 4.12: Schematic and layout of MWG for tapeout

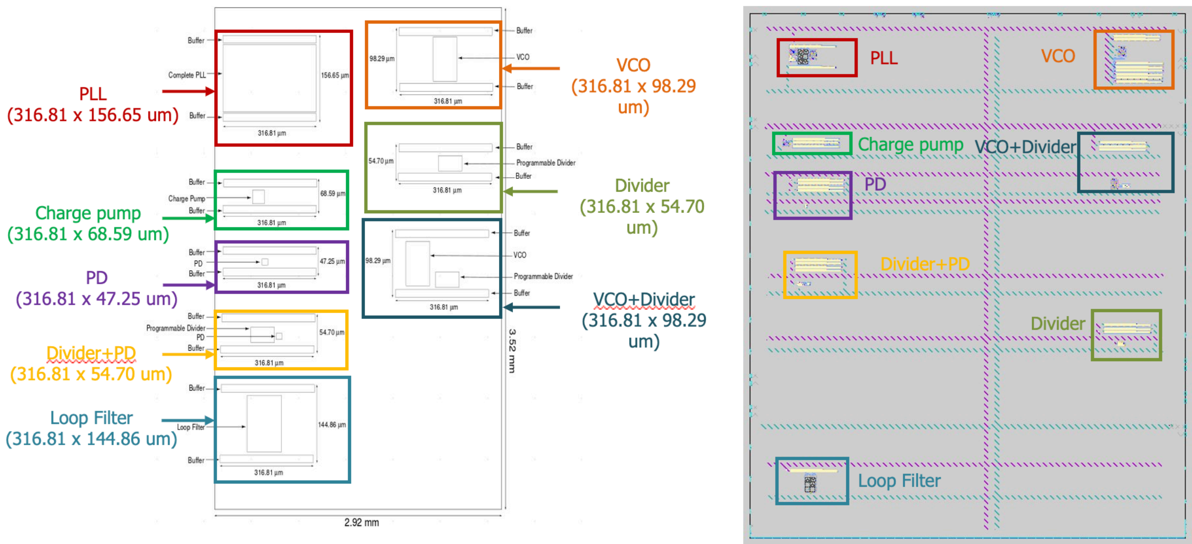


Figure 4.13: Floorplan and layout of complete die for tapeout

4.6 Summary

In this chapter, a 2.87 GHz microwave signal generator (MWG) with a minimum sweep-step size of 50 kHz has been presented for NV-ODMR based CMOS quantum sensing applications to detect $< 1\ \mu$T magnetic field strengths ($|\vec{B}|$). Conventionally, for ODMR, the 2.87 GHz signal is frequency modulated using an external source, which drastically increases power consumption and system complexity. This work presented MWG with on-chip programmable sweep capability to generate microwave signals close to 2.87 GHz for improved sensitivity of $|\vec{B}|$ measurement in NV-ODMR. The proposed MWG has been implemented in 180 nm CMOS technology and its operation is validated by post-layout simulations, which show that it achieves a phase noise of -114.5 dBc/Hz at an offset of 1 MHz near 2.87 GHz frequency, while consuming 11.14 mW from 1.8 V supply. Post-layout simulations also show that the proposed MWG has a tuning range of 2.515 to 3.069 GHz with a low gain VCO that exhibits $K_{VCO} <$ 51.67 MHz/V and can be used to sense $|\vec{B}| < 0.9\ \mu$T, which is much lower as compared to the other existing works.

Chapter 5

Deep Learning Based Portable Respiratory Sound Classification System

5.1 Introduction

Respiratory diseases are among the leading causes of death with lung infections, lung cancer and chronic obstructive pulmonary disease (COPD) accounting for nearly one-sixth of the deaths worldwide. According to the Global Burden of Disease (GBD) study, infections in the lower respiratory tract are among the leading causes of death [22]. A delay in the diagnosis of such diseases can lead to serious irreversible health complications. These diseases also have an adverse impact on the social and economic conditions of a person. Access to diagnostic modalities such as lung ultrasounds is required in order to perform accurate diagnoses. However, under resource-limited situations where physicians do not have access to such infrastructure and equipment, auscultation which involves the analysis of respiratory sounds by a trained physician still serves as a prominent tool for preliminary diagnosis[23]. Respiratory sounds are generated by the movement of air within the respiratory system. These sounds vary depending on the state of the respiratory system and the health of the individual. Different respiratory disorders are characterized by a specific set of respiratory sounds which can serve as indicators of the particular disorder. Table 5.1 shows some of the common respiratory diseases and their respective respiratory sound indicators [24].

In this work, a portable system has been proposed and implemented to classify respiratory sounds through the use of audio processing and convolutional neural networks (CNN) in order to aid the auscultation process and allow for faster and more accurate diagnoses even in the absence of trained medical professionals and advanced diagnosis equipment.

This work has made use of HF_Lung_V1 dataset which is a combination of a database used in a datathon in Taiwan Smart Emergency and Critical Care (TSECC), 2020, under the license of Creative

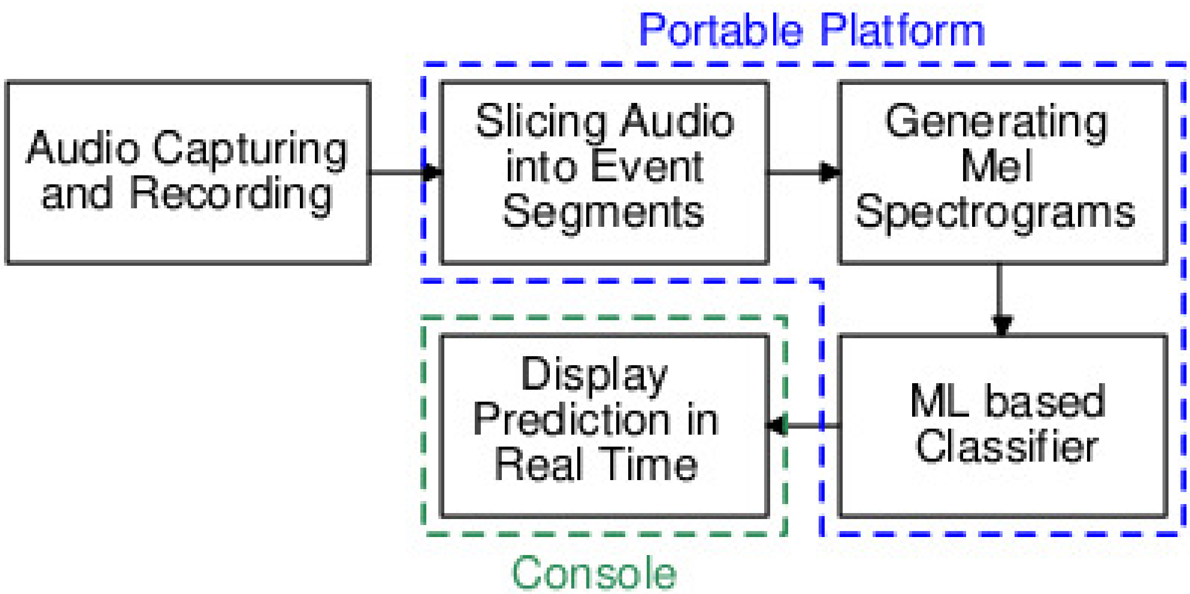


Figure 5.1: Overview of proposed system

Disease	**Rhonchi**	**Wheeze**	**Stridor**	**Crackling**
Bronchitis	X	X		X
COPD	X	X		X
Pneumonia		X		X
Epiglottitis		X	X	
Laryngomalacia			X	
Cystic fibrosis				X
Heart disease		X		X

Table 5.1: Respiratory diseases and respective lung sounds

Commons Attribution 4.0 (CC BY 4.0), provided by the Taiwan Society of Emergency and Critical Care Medicine (TSECCM) and sound recordings acquired from 18 residents of a respiratory care ward (RCW) or a respiratory care center (RCC) in Northern Taiwan [25]. This system is aimed at performing multi-class classification of normal, rhonchi, wheeze, stridor and crackles. This paper is organized as follows: Section 5.2 presents the background of this work and a review of related works. Section 5.3 elaborates the various signal processing techniques used to process the respiratory audio signals and extract features for classification and presents the deep learning model architecture used for classification. Section 5.4 summarizes the results obtained and Section 5.5 provides the conclusion.

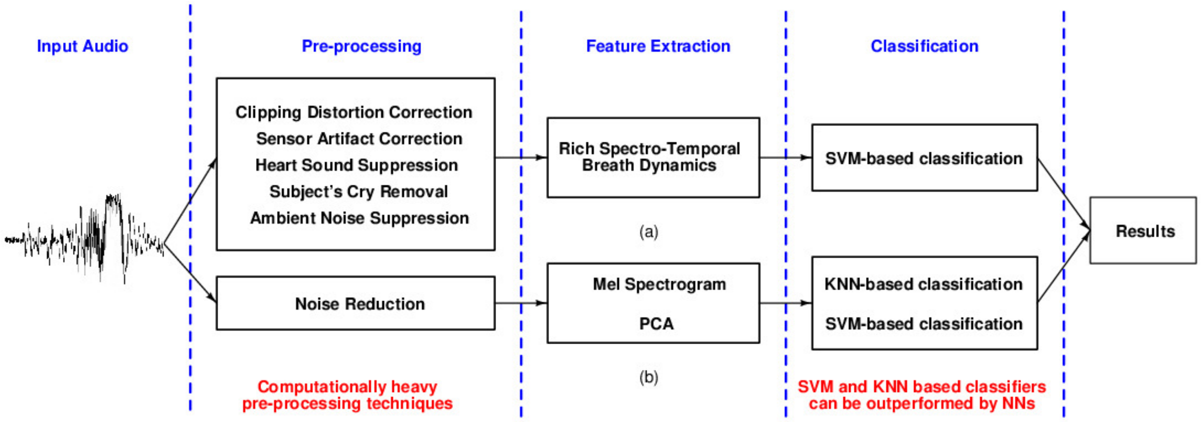


Figure 5.2: Respiratory sound classification methods in related works: (a)[26] and (b)[27]

5.2 Background and Prior Works

Various efforts have been made towards automated lung auscultation for diagnostic applications. [26] proposes a computer-aided approach to classify respiratory sounds even in noisy environments using noise suppression schemes, spectrotemporal features and support vector machines. The framework is shown to be effective in noise suppression suitable for auscultation and explores the use of rich biomimetic feature mappings yielding notable improvement in classifying adventitious respiratory events. Fig. 5.2(a) shows the pipeline with a variety of pre-processing techniques and feature extraction and classification methods. The fallback is that complex and computationally heavy algorithms have been used which necessitate the use of computing systems capable of handling the load and poses a challenge to making the system function in real-time. [27] proposes an ML-based approach to classify respiratory sounds based on Mel Spectrograms and develops a comparison between performance obtained using different algorithms. PCA is applied to the Mel spectrograms to extract audio signature features which are fed to the classifier models. Fig. 5.2(b) shows the flow of data through the noise reduction stage followed by Mel spectrogram generation, PCA and the classifier. [28] explores the possibility of using smartphones to record respiratory audio for the development of portable solutions. It is concluded that lung auscultation with smartphone built-in microphones is feasible in a clinical context but with heavy limitations on the accuracy of diagnosis. These works have solely focused on the design and implementation of computerized lung auscultation software and are heavily dependent on complex processing algorithms or handicapped due to the lack of sufficiently robust algorithms. There have been no efforts towards making this system completely portable to function outside the clinical environment and in real-time. In this work, we focus on developing a system capable of performing real-time lung auscultation on a portable platform.

5.3 Respiratory Sound Processing and Classification

5.3.1 Respiratory Sound Processing

The HF_Lung dataset contains 9765 15-second audio files with 8,457 wheeze labels, 686 stridor labels, 4,740 rhonchi labels and 15,606 discontinuous adventitious sound labels. Various respiratory events are characterised by sounds of distinctive properties. Ronchi is a low-pitched snoring-like sound with a frequency range of less than 200 Hz while wheeze is a high pitched whistling like sound with a frequency range greater than 400 Hz. Stridor is a high-pitched musical sound with a frequency range greater than 500 Hz while coarse and fine crackles are explosive sounds with frequencies ranging near 350 Hz and 650 Hz respectively [29].

Discerning different respiratory sounds is very difficult from an audio signal due to the presence of noise and lack of visible frequency information. The feeble nature of respiratory audio makes the task of classification more challenging. This brings us to the requirement of more robust representations of the audio signals such as spectrograms in order to aid the task of classification. Spectrograms are an ideal choice for representing respiratory audio signals as they are much more suited for the classification task as compared to audio signals as they contain frequency spectrum information variation with time [30, 31]. With the advances in computer vision oriented machine learning models, the feature extraction and classification of image data such as spectrogram images are more effective and efficient as compared to audio signals.

5.3.2 Mel Spectrogram

Spectrograms visually represent the signal strength of a signal at various frequencies over time. Spectrograms can be plotted over the raw magnitude or over a logarithmic scale. However, linear or logarithmic spectrograms may prove to be insufficient to obtain sufficiently differentiable spectrogram representations for respiratory signals as the frequency bands formed in spectrograms will not be discrete enough to discern. The Mel scale allows for better differentiation between lower frequencies as compared to higher frequencies which are ideal for respiratory sounds as they fall in the 50 Hz to 2500 Hz range and is used in such instances for improved detection and classification [29]. Eq. 5.1 gives the

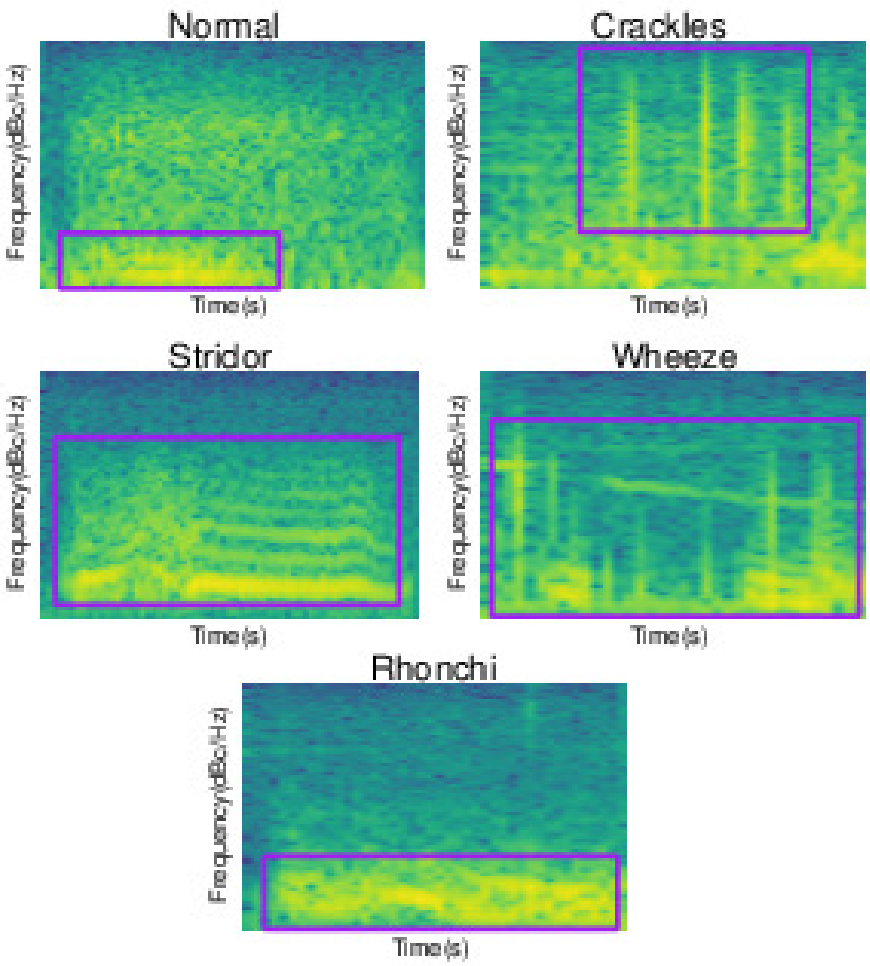


Figure 5.3: Mel spectrograms for different respiratory sounds in HF_Lung

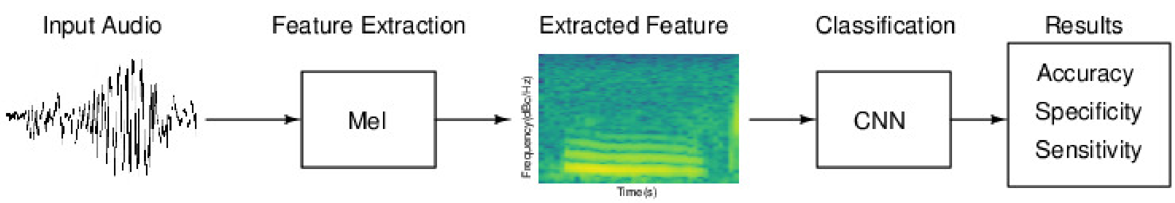


Figure 5.4: Respiratory sound classification pipeline

Mel scale value, m, for a frequency of f in Hz.

$$m = 2595 \cdot log_{10}\left(1 + \frac{f}{700}\right) \tag{5.1}$$

The spectrogram parameters need to be adjusted in order to ensure that the spectrograms generated are best representative of the data and have sufficient resolution. The size of the FFT, N, defines the frequency resolution of the spectrogram. $\frac{SR}{N}$ gives the frequency resolution, res, of the generated spectrogram with respect to the sampling rate, SR, and N. There is an increase in frequency resolution with the increase in N. Hence, the N value selected must be sufficiently high in order to ensure sufficient frequency resolution in the generated spectrogram. Another parameter to be aware of is the window size since a smaller window size implies not enough information is present in each window to give sensible spectral information while a larger window size implies there will be excess leakage of information leading to a lack of resolution. The type of window is also a determining factor as rectangular windows are very poor choices as they have very minimal side lobe attenuation i.e., their side lobes in the frequency domain have significant magnitude with respect to the main lobe. Hamming and Hanning windows are a far better choice of windows as their side lobes are of negligibly lower magnitude as compared to the main lobe. The magnitude of the first side lobe of the Hamming window is lower than the first side lobe of the Hanning which would make it a better choice for eliminating the contribution of those side lobe frequencies but the distant side lobes of the Hanning are far more attenuated than the Hamming making Hanning a better choice for signals with larger bandwidths i.e., energy spread across a wider frequency range.

Fig. 5.3 shows the Mel spectrograms generated for various respiratory sounds with 1024 point FFT with Hanning window of length of 128 and hop length of 64. The distinction between different sounds is clearly visible in their respective spectrograms.

5.3.3 Deep Learning Classifier

Deep learning is used across various machine learning and artificial intelligence (AI) applications to obtain best possible results by imitating human learning abilities. CNNs are a class of artificial neural networks widely used for image classification applications due to their ability to abstract image data to feature maps [32] -[34]. The Mel spectrograms generated can be processed as images. Mobilenet_V2 is the chosen CNN architecture due to its drastically lower parameter count and memory and processing requirements allowing for use on mobile platforms [35]. In this work, we make use of a transfer learning-

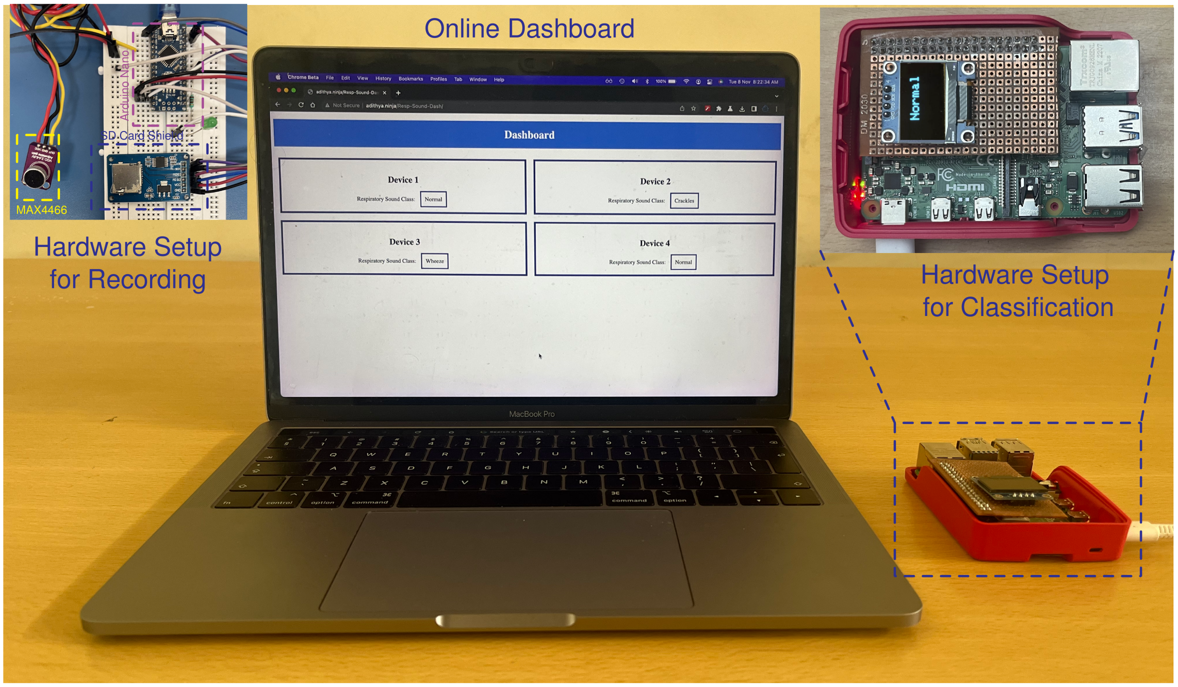


Figure 5.5: Portable Respiratory sound classification system with recording system

based approach. The available MobileNet_V2 model is trained on the ImageNet dataset which implies that the convolution layers are heavily trained for multi-class feature extraction. These pre-trained convolutional layers are used in conjunction with classifier layers trained on the application-specific dataset to allow for state-of-the-art feature extraction and classification.

5.4 Results and Discussions

Fig. 5.4 shows the complete pipeline used in this work. The classifier is trained on the dataset on a multi-GPU system and testing is performed on a Raspberry Pi 4B with 8 GB of RAM in order to verify complete functionality on a portable platform. Raspberry Pi offers sufficient resources for the use of CNN-based classifiers while maintaining a small form factor making it an ideal choice for a portable system. Fig. 5.5 shows the Raspberry Pi-based portable respiratory sound classification system. Since the Raspberry Pi only has a CPU and no GPUs, the model is reconfigured to run on CPU alone. The system implementation is able to perform the tasks of multiclass classification of normal, rhonchi, wheeze, stridor and crackle sound events from respiratory audio data obtained in real-time. The HF_Lung dataset is split in an 80:20 ratio into training and testing data. Fig. 5.6 shows the

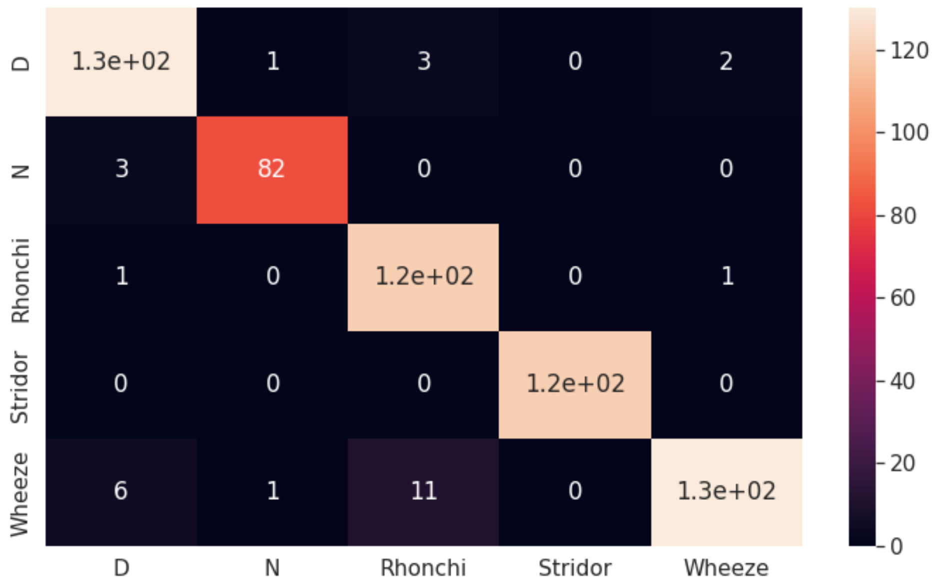


Figure 5.6: Confusion matrix obtained for test split of HF_Lung dataset

Ref.	**[26]**	**[27]**	**[29]***	**This work**
Accuracy (%)	86.67	64.45	64.90	80.55
Sensitivity (%)	86.82	-	51.93	95.65
Specificity (%)	86.55	-	77.88	98.80

* Performance on Task 1-2 in the mentioned work which is most comparable to this work

Table 5.2: Performance summary and comparison with similar works

confusion matrix obtained on the test dataset. It is observed that the model is able to classify each of the adventitious sounds with high accuracy. The model achieves an accuracy of 80.55% with a sensitivity of 95.65% and a specificity of 98.80% on the testing dataset. Table 5.2 shows the performance summary and compares it with that of related works. It is clearly visible that this work ensures improved sensitivity and specificity while maintaining high accuracy. The accuracy obtained in this work is also comparable to [26] which makes use of complex and computationally heavy pre-processing algorithms.

Fig. 5.5 also shows the recording system consisting of Arduino Nano and MAX4466 which can capture audio in real time for use with the classification system. The results of classification from the system are pushed to an IoT cloud service like ThingSpeak through MQTT. This allows for the data

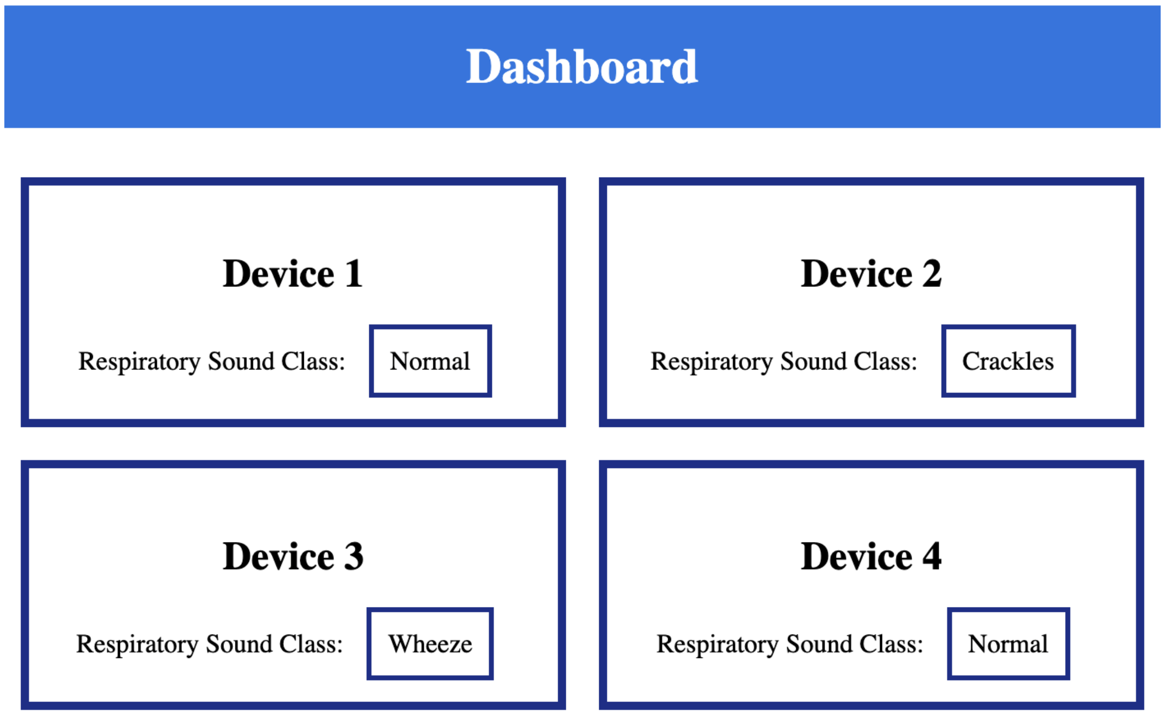


Figure 5.7: Online dashboard layout

to be accessed remotely through a web dashboard which has been set up to centrally monitor all the portable devices. Fig. 5.7 shows the developed online dashboard,

5.5 Summary

Respiratory diseases pose a major threat to our well-being. Methods of diagnosis of such diseases are often complex and require extensive training and experience to perform. Delay in diagnosis can be fatal and such methods are also seen to be less effective in minors. In this work, an automated system has been proposed and a proof of concept implemented to classify respiratory sounds to help recognise anomalies which may be the sign/symptom of respiratory diseases. The respiratory audio recordings obtained from the recording system are converted into spectrograms and fed to CNNs for classification. The system designed and implemented in this work achieves an accuracy of 80.55% with a sensitivity of 95.65% and a specificity of 98.80% on the HF_Lung dataset on the tasks of multiclass classification of normal, rhonchi, wheeze, stridor and crackle respiratory sound events.

Chapter 6

FMCW Radars

6.1 Working of FMCW Radars

Frequency Modulated Continuous Wave (FMCW) radar is a type of radar system that operates by continuously transmitting a signal with a frequency that is modulated or varied over time. FMCW radars are commonly used for various applications, including distance and speed measurements, object detection, and tracking.

The basic principle of FMCW radar involves transmitting a continuous wave signal with a linearly increasing or decreasing frequency. This signal is often referred to as the ”chirp.” The chirp signal is emitted by the radar antenna and travels through space until it encounters objects in its path. When the chirp signal reflects off an object, such as a target or obstacle, a portion of the signal is reflected back to the radar antenna. This reflected signal, also known as the ”echo,” carries information about the distance and velocity of the object. The FMCW radar system simultaneously transmits and receives signals, allowing it to compare the transmitted chirp signal with the received echo signal. By analyzing the frequency difference between the transmitted and received signals, the radar can determine the range or distance to the target. The frequency difference, also known as the beat frequency, is directly proportional to the round-trip distance traveled by the radar signal. By measuring the beat frequency, the FMCW radar can accurately calculate the distance to the target.

Moreover, FMCW radar can also provide velocity information. Since the transmitted frequency is continuously changing over time, any change in the frequency of the received signal can be attributed to the relative velocity between the radar and the target. By analyzing the frequency shift, the radar can determine the speed or velocity of the target. FMCW radars are particularly advantageous for their ability to provide range and velocity measurements simultaneously, along with their high range resolution and accuracy. They are commonly used in applications such as automotive collision avoidance systems, traffic monitoring, weather radar, and industrial sensing.

6.2 Advantages

FMCW (Frequency Modulated Continuous Wave) radars offer several advantages that make them well-suited for various applications. Here are some of the key advantages:

1. Range Resolution: FMCW radars provide excellent range resolution, allowing them to detect and distinguish between multiple targets that are closely spaced. This high range resolution enables precise localization and tracking of objects, making FMCW radars suitable for applications that require accurate distance measurements.

2. Simultaneous Range and Velocity Measurement: FMCW radars can measure both the range (distance) and velocity of targets simultaneously. This capability is particularly useful in applications such as automotive radar systems, where knowledge of both the distance and speed of surrounding objects is crucial for collision avoidance and adaptive cruise control.

3. Frequency Modulation: The use of frequency modulation in FMCW radars provides robustness against interference and noise. By employing specific modulation techniques, FMCW radars can distinguish between the transmitted signal and unwanted signals or clutter, resulting in improved target detection and reduced false alarms.

4. Continuous Waveform: FMCW radars transmit a continuous waveform, allowing for continuous monitoring of the surrounding environment. Unlike pulsed radar systems that have gaps between transmitted pulses, FMCW radars provide continuous coverage, enabling real-time tracking and surveillance.

5. Lower Peak Power: FMCW radars typically operate at lower peak power levels compared to pulsed radars. This lower power requirement simplifies the design and reduces the complexity and cost of the radar system. It also makes FMCW radars suitable for applications where power consumption and electromagnetic compatibility are important considerations.

6. Reduced Interference: FMCW radars are less susceptible to interference from other radar systems or electromagnetic sources operating at different frequencies. The frequency modulation used in

FMCW radars allows them to operate concurrently with other radar systems without significant interference, making them suitable for crowded electromagnetic environments.

7. Compact and Lightweight Design: FMCW radars can be implemented using compact and lightweight hardware components. The continuous waveform and lower power requirements enable the use of smaller antennas and more efficient signal processing algorithms. This compact design makes FMCW radars suitable for applications where size, weight, and power constraints are important, such as in portable devices or unmanned aerial vehicles (UAVs).

6.3 Challenges

While FMCW (Frequency Modulated Continuous Wave) radars offer several advantages, they also come with certain challenges and disadvantages. Here are some of the key considerations:

1. Doppler Ambiguity: FMCW radars suffer from Doppler ambiguity, which means they cannot accurately determine the velocity of a target if it exceeds the maximum measurable velocity range. This limitation arises due to the finite frequency sweep range of the radar signal. Special techniques, such as multiple frequency ramps or complex signal processing algorithms, may be required to mitigate this issue.

2. Range-Doppler Coupling: FMCW radars exhibit range-Doppler coupling, which means that changes in target distance can affect the measured velocity and vice versa. This coupling can introduce errors in target tracking and velocity estimation, especially when dealing with dynamic or rapidly changing scenarios.

3. Frequency Nonlinearity: The frequency modulation in FMCW radars relies on the assumption of linear frequency sweep. However, in practice, there can be non-linearities in the frequency response of the radar system, which can distort the received signal and affect the accuracy of range and velocity measurements. Calibration and compensation techniques may be necessary to address these non-linearities.

4. Interference and Clutter: FMCW radars can be susceptible to interference and clutter from other radar systems, sources of electromagnetic radiation, or environmental factors. These unwanted signals can degrade the radar's performance, leading to false detections or reduced sensitivity.

Advanced signal processing techniques, such as adaptive filtering or interference rejection algorithms, are employed to mitigate these effects.

5. Limited Range and Penetration: FMCW radars may have limitations in terms of maximum range and penetration capability. The range is typically limited by the power and sensitivity of the radar system, as well as environmental factors such as atmospheric absorption. Additionally, FMCW radars may struggle to penetrate certain materials, such as dense foliage or walls, which can limit their effectiveness in certain applications.

6. Cost and Complexity: Implementing FMCW radar systems with high-performance capabilities can be complex and costly. Sophisticated hardware components, precise frequency modulation schemes, and advanced signal processing algorithms are required to achieve accurate and reliable measurements. This complexity can increase the overall system cost and require expertise in radar design and implementation.

Chapter 7

Circuits for Frequency Modulated Continuous Wave Chirp Synthesizers in mmWave Radars

7.1 Introduction

The frequency modulated continuous wave (FMCW) technique has gained significant popularity in recent years, particularly in the 76-81 GHz band mmWave radar applications. It is highly regarded for its ability to deliver precise, accurate, and wide bandwidth performance for various applications such as autopilot and advanced driver assistance systems (ADAS)[36]. In ADAS applications, an FMCW-based mmWave radar, as depicted in Fig. 7.1, utilizes frequency chirps generated by a chirp synthesizer. These chirps, known as TX chirps, are transmitted towards the target object. The radar then receives the reflected signals, referred to as RX chirps, after a time delay. By mixing the RX chirps with the TX chirps, an intermediate frequency (IF) signal is produced. This IF signal is further processed using digital signal processing (DSP) techniques to estimate crucial parameters like object range, velocity, and angle of arrival.

In the FMCW technique, as illustrated in Fig. 7.2, a chirp is created by continuously varying the transmitted frequency from the radar. The chirp bandwidth (BW_{ch}) represents the difference between the maximum (f_{max}) and minimum (f_{min}) radiated frequencies, while the chirp period (T_m) signifies the duration required to generate the desired BW_{ch}. For ADAS applications, a vital component called the chirp synthesizer is employed in FMCW radars. This block is responsible for generating low-noise chirps with a high BW_{ch} (up to 4 GHz) in a short chirp period (T_m) of less than 100 microseconds. Additionally, it is crucial for the frequency sweep (f_{min} to f_{max}) to exhibit high linearity to ensure improved spectral purity and reduced communication errors[37].

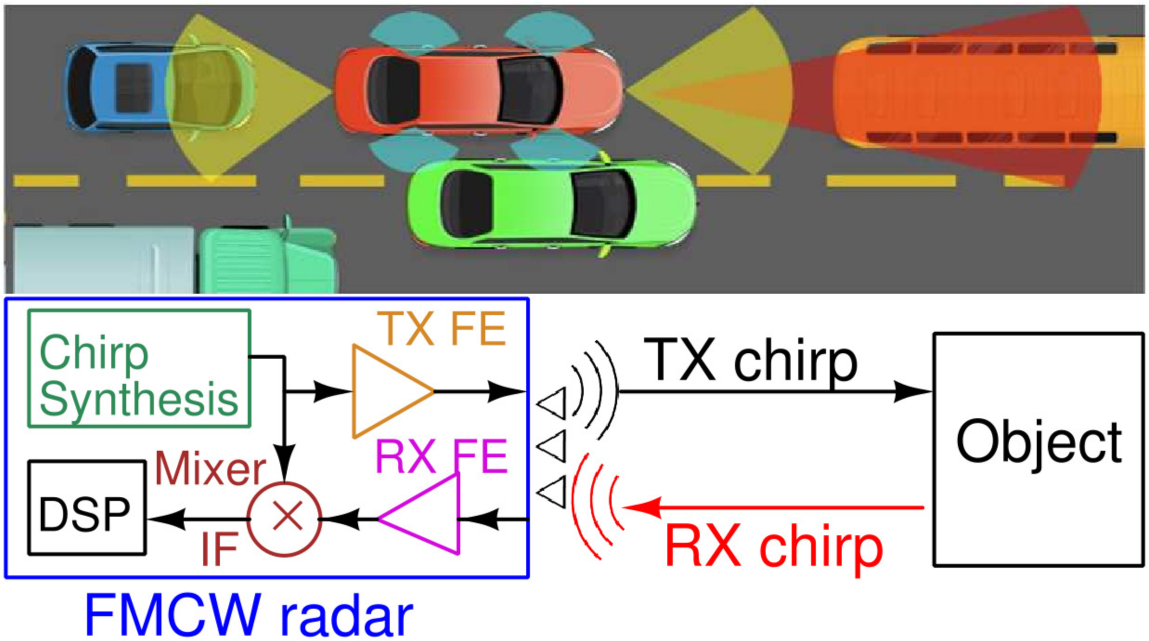


Figure 7.1: mmWave FMCW based radars in ADAS applications

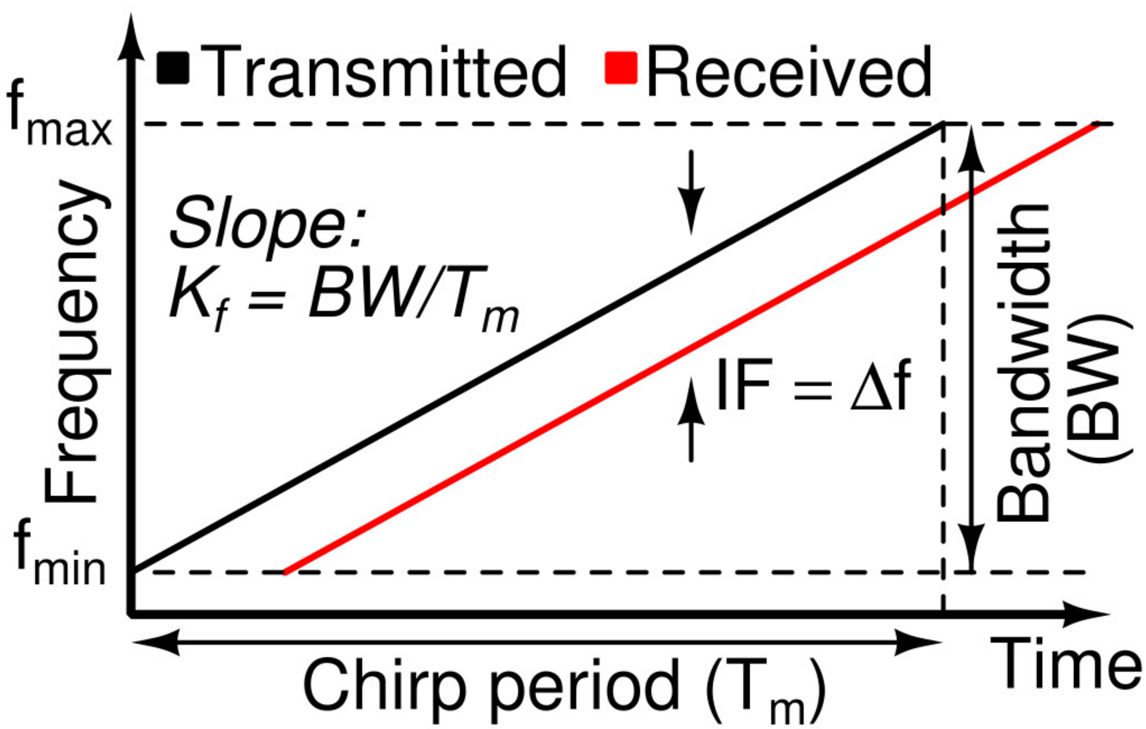


Figure 7.2: FMCW chirp characteristics

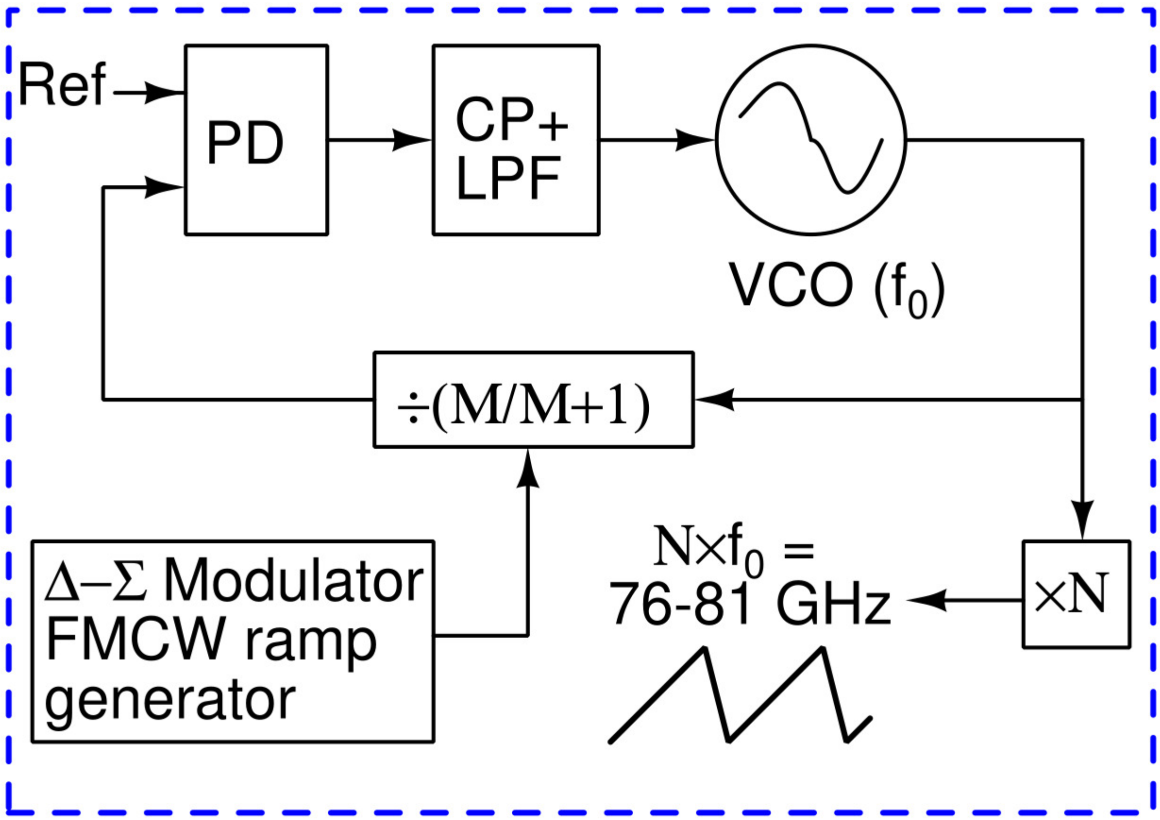


Figure 7.3: PLL based chirp synthesizer

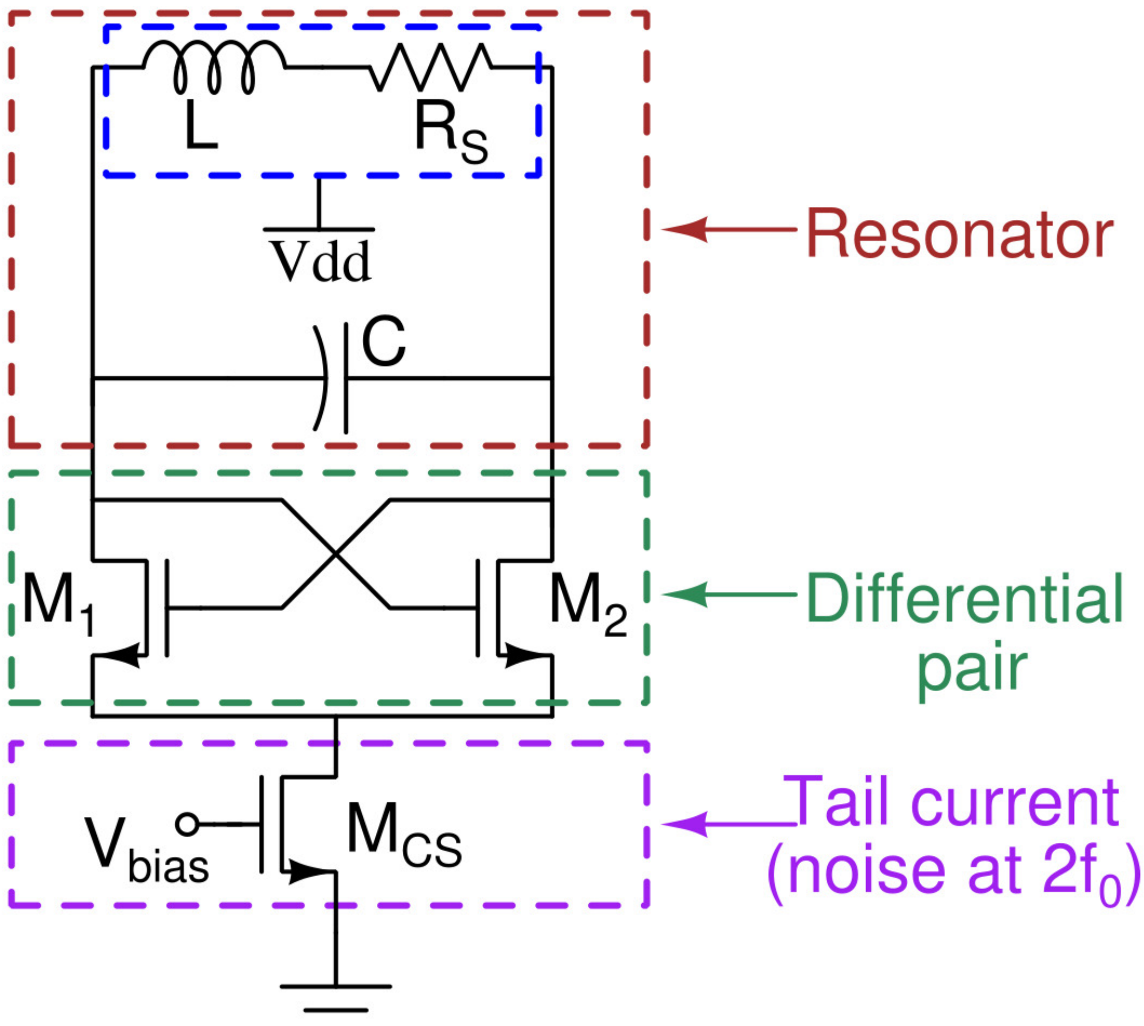


Figure 7.4: Noise sources in LC VCO [42]

In recent times, there has been a surge of reported Phase Locked Loop (PLL) based chirp synthesizers designed for FMCW mmWave radars [38]. Fig. 7.3 illustrates the configuration of an FMCW chirp synthesizer, wherein a frequency f_0 is synthesized within a PLL using a voltage-controlled oscillator (VCO). This frequency is then multiplied by a factor N to generate a 76-81 GHz signal. It is important to note that directly generating a 76 GHz frequency is prone to vulnerabilities arising from parasitic values. To ensure greater stability and reduced phase noise of the chirp signal in the 76 GHz band, a multiplier ($N = 2, 3,$ or 4) is employed. The VCO serves as a critical component in generating the mmWave chirp signal with high fidelity. Fig. 7.4 showcases a conventional cross-coupled LC oscillator topology, along with the primary noise sources that cannot meet the stringent phase noise requirements at mmWave frequencies (above 10 GHz) [39], [40]. Therefore, in pursuit of building VCOs with low phase noise for 76-81 GHz FMCW chirp synthesizers, this study presents the following: 1) a comprehensive analysis of an mmWave VCO topology incorporating a coupled transformer tank load, 2) a low phase noise VCO topology for the frequency range of 18.98-20.46 GHz, 3) the implementation of the proposed VCO using 65 nm CMOS technology, and 4) post-layout simulation results that validate the effectiveness of the proposed low phase noise mmWave VCO topology. The multiplier based architecture also necessitates a multi-modulus programmable divider capable of producing a wide range of divide ratios with high precision to allow for fine frequency resolution. The divider is crucial in generating chirp signals continuous in time with the help of an established negative feedback loop. In this work, we present - 1) the design of a multi-modulus programmable frequency divider with a wide divide ratio of 256-511 capable of dividing mmWave frequencies near 20 GHz to conventional on-chip crystal oscillator frequency range (10's of MHz), 2) implementation of proposed multi-modulus divider design in 65 nm CMOS technology and 3) its schematic simulation result.

This chapter is organised as follows: In Section 7.2, the proposed mmWave (20 GHz) VCO topology is presented and Section 7.3 details the multi-modulus divider topology and design methodology. The circuit implementation & simulations results are presented in Section 7.4 and conclusion is presented in Section 7.5.

7.2 Proposed VCO Topology

In this work, the current reuse VCO topology shown in Fig. 7.5(a), as proposed in [48] and [49] is employed. This topology utilizes a transformer as the load tank of the VCO, with a turn ratio ($n < 1$).

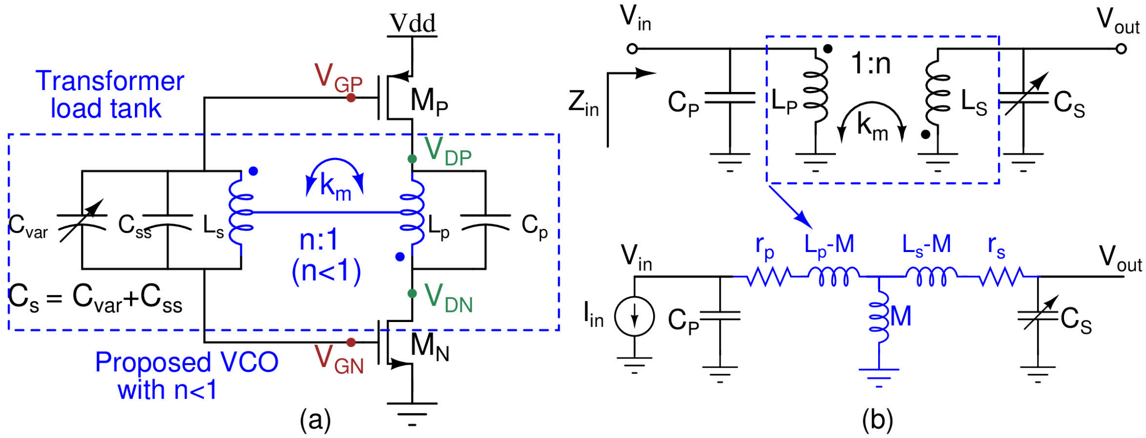


Figure 7.5: (a) Proposed VCO topology with $n < 1$ for mmWave operation (b)Transformer based resonator and its equivalent model

The turn ratio (n) for a multi-turn transformer with a $1 : n$ configuration can be defined by the following equation (Eq. 7.1).

$$n = k_m \sqrt{\frac{L_s}{L_p}} \tag{7.1}$$

where, L_p, L_s and k_m are the primary-side, secondary-side inductors and coupling coefficient , respectively. In Fig. 7.5(a), the primary-side capacitor is denoted as C_p, and the secondary-side capacitor is represented as C_{ss}, both of which are fixed metal-insulator-metal (MIM) capacitors. The varactor C_{var} is utilized to achieve the desired tuning range. The transconductance necessary for initiating the oscillations is provided by M_P and M_N. Fig. 7.5(b) displays the electrical equivalent of the transformer [48], [44]. In this representation, $(C_s = C_{ss} + C_{var})$ represents the total capacitance at the secondary-side, $(M = k_m\sqrt{L_pL_s})$ corresponds to the mutual inductance, and r_p and r_s represent the loss resistance of L_p and L_s, respectively. In order to achieve reduced phase noise, it is crucial to have a load tank with a high-Q factor near the frequencies of a pseudo sinusoidal waveform containing f_0 and $2f_0$ components. The subsequent subsections will describe the design considerations for the low phase noise mmWave VCO design.

7.3 Multi-Modulus Divider Design Methodology

The proposed multi-modulus frequency divider has a cascade of eight 2/3 dual modulus cells as illustrated in Fig. 7.7, the first two stages are realized with CML latch-based prescaler cells and the later stages are designed with CMOS logic-based prescaler. Each of the CML cells is followed by a

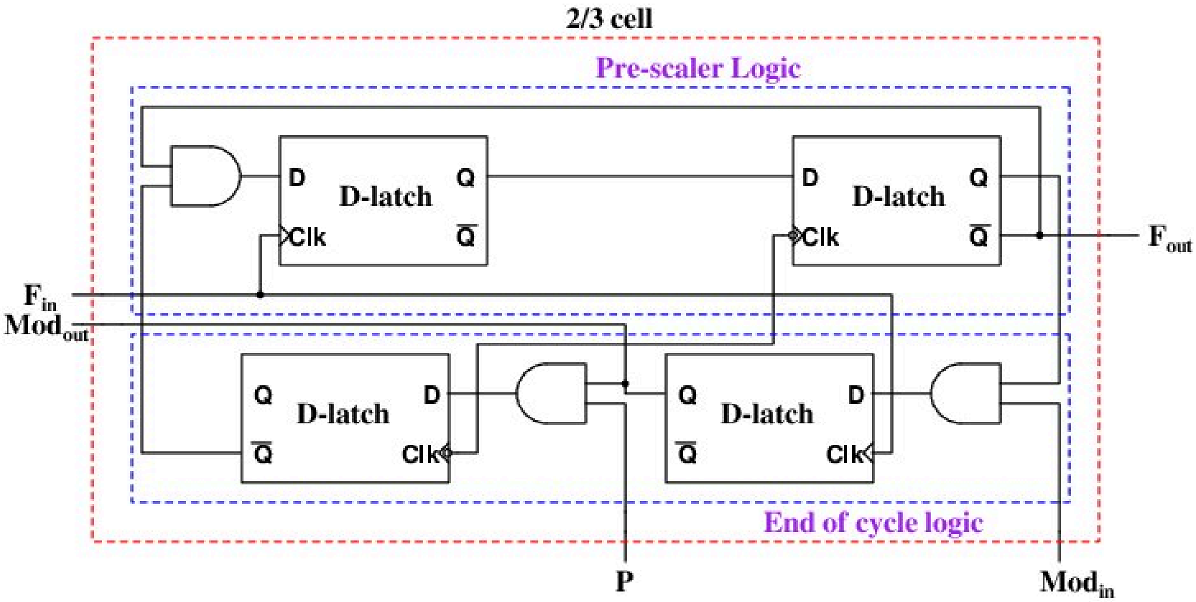


Figure 7.6: divide by 2/3 cell

CML buffer to ensure sufficient voltage swing to drive the next CML stage. For the transition of CML logic levels to CMOS, a CML to CMOS converter is placed after the second CML stage and to inhibit the effect of loading of the later stages, the CML and CMOS stages are isolated using a CMOS tapered buffer.

7.3.1 2/3 Dual modulus prescaler cell

As shown in Fig. 7.6, the architecture of the prescaler cell consists of 2 main sections - prescaler logic and end-of-cycle logic. When the input bit P is 0, the end-of-cycle logic part is inactive while the prescaler logic part is active and the prescaler cell divides by 2 using the two D-latches, forming a D-flipflop, with the negated output ($\overline{Q}$) given as input (D) to the flipflop. When the input bit P is 1, if the input Mod_{in} is high, then the later part becomes active and the whole cell divides by 3. During this cycle Mod_{in} is propagated to the output signal Mod_{out} for modulus control to the previous prescaler cell. If the input Mod_{in} is low, the end of cycle part becomes inactive and the prescaler cell divides by 2.

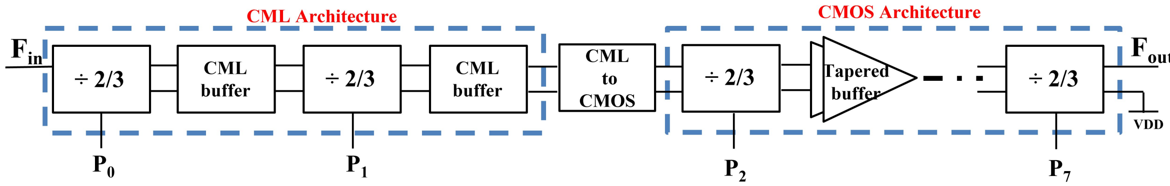


Figure 7.7: Proposed MMFD comprising of a cascade of eight 2/3 dual modulus prescalers.

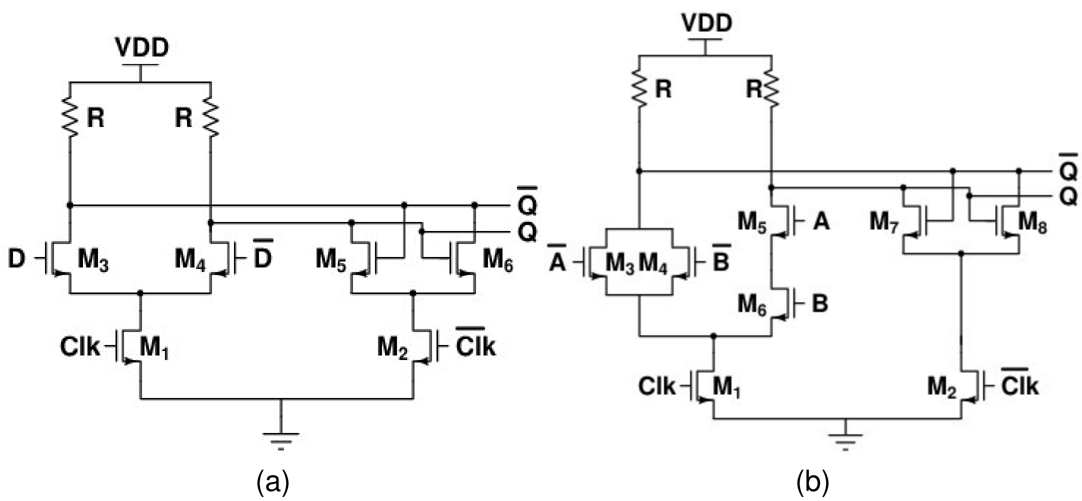


Figure 7.8: (a) CML Latch (b) CML latch integrated with AND gate

7.3.2 CML latch and buffer

Fig. 7.8(a) shows the schematic of the CML D-latch capable of two modes of operation - signal tracking and signal holding. These modes are decided by the input differential clock signal (Clk) given at the gates of the MOSFET's M_1 and M_2. When the Clk signal is high, the latch goes into the tracking phase activating the MOSFET's M_3 and M_4 and the output Q is equal to the input D. When Clk is low, the latch switches to the hold state activating the MOSFET's M_5 and M_6 which retains the value of output Q. The latch operates well when satisfies the condition $g_{m_4}R$ (gain of the tracking pair) ≥ 1 and accordingly the suitable value of load resistance R is selected. If the gain is less than 1, then when the MOSFET's M_5 and M_6 are activated in the hold state, the previous state of Q cannot be retained. In the prescaler cell shown in Fig. 7.6, the latches are preceded by an AND gate, so for improved performance and to avoid the effects of delay in the circuit, the AND gate is integrated with the CML D-latch as shown in the Fig. 7.8(b) where A and B are the inputs of the AND gate instead of an external CML based AND/NAND gate[4]. The CML latch does not give a complete rail-to-rail voltage swing, it is

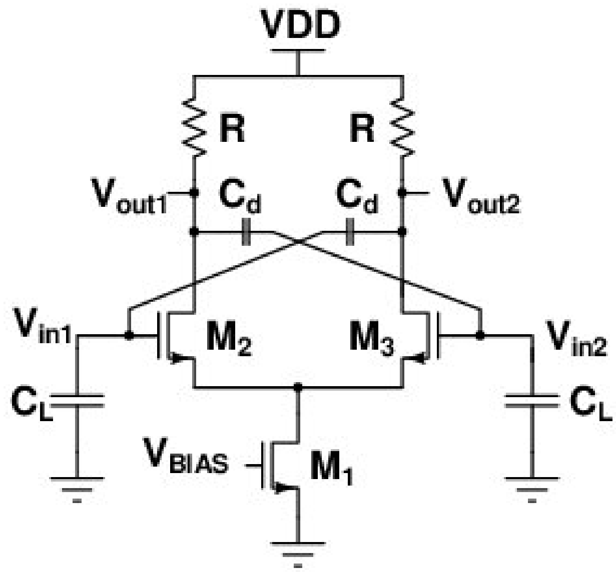


Figure 7.9: CML buffer architecture

around $4V_{TH}$. Buffers are used to polish and maintain the voltage swing of the signal to be able to drive the other stages. Fig. 7.9 shows the schematic of a CML-based buffer which outputs the input signal with restored voltage levels for the given input differential signal. The capacitances C_d are placed to diminish the effects of input-output coupling which neutralises the circuit. The MOSFET M_1 provides input-independent current biasing to the circuit with the help of V_{BIAS}. For improved performance of the buffer, the load resistances of this buffer have to be small to reduce the RC delay of the circuit which in turn increases the bandwidth of operation.

7.3.3 CML to CMOS converter

CML logic-based buffer gives a differential output with low voltage swing which cannot drive a CMOS logic-based prescaler. So, a CML to CMOS converter as shown in Fig. 7.11 is inserted in between as shown in Fig. 7.7 which takes in the differential input signal ($In, \overline{In}$) with low voltage swings and gives output signal ($Out, \overline{Out}$) with full rail-to-rail voltage swing as using current mirrors. Table 7.1 shows the $\frac{W(\mu m)}{L(\mu m)}$ ratios of all the MOSFET's (M_{1-12}) and the bias current (I_{BIAS}) [59].

7.3.4 CMOS Latch and buffer

After the initial stages of CML logic-based prescaler cells and buffers, the frequency of operation of the circuit is lowered below 6 GHz. So for better performance of the circuit with maximum voltage

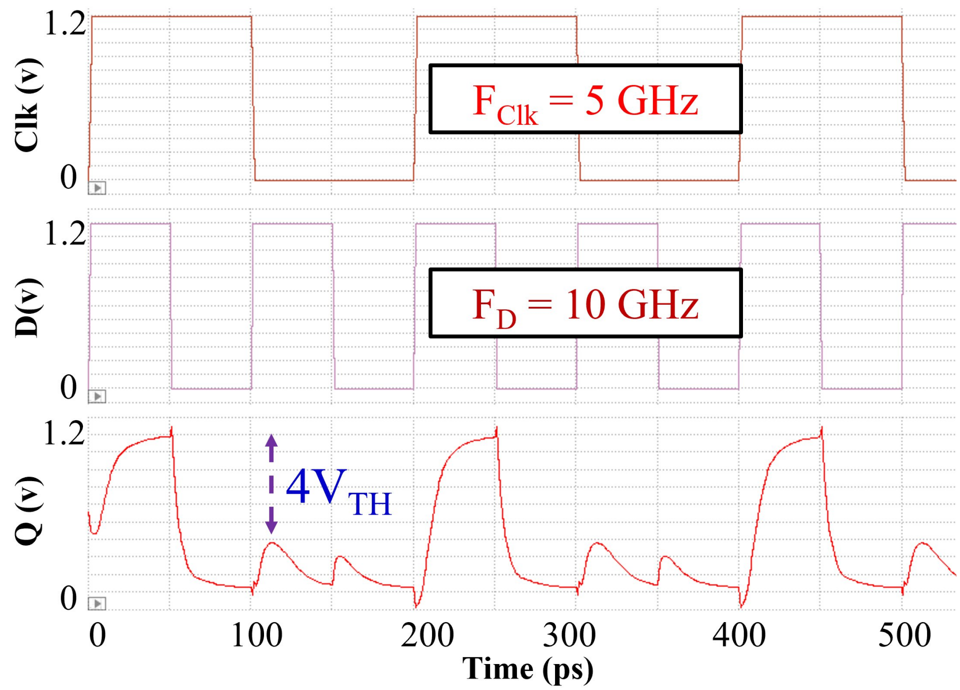


Figure 7.10: Transient plots of CML latch when given clock signal of frequency 5 GHz and data signal of frequency 10 GHz.

swings, CMOS logic-based prescalers are implemented depicted in Fig. 7.12(a). It is based on D-latch which is made using CMOS NAND gates. These prescalers give full rail-to-rail voltage swing outputs but that may not be sufficient enough to drive huge loads due to insufficient flow of current. So, it is often required to have inverter buffer chains with appropriate sizing based on their electrical effort to isolate the stages and inhibit the loading effects. Fig. 7.12(b) shows the schematic of a 2-stage tapered buffer consisting of two inverters - one of minimum size and the other 4 times the minimum size which will be able to drive the load of the corresponding next stages in the divider chain.

7.4 Implementation & Simulation Results

7.4.1 Low Phase Noise VCO

This subsection presents the implementation details and simulation results of the proposed custom-designed transformer and complete VCO in 65nm CMOS process.

The transformer was designed using ASITIC and further optimized in HFSS to achieve a high Q factor in the mmWave frequency range. The designed transformer, as depicted in Fig. 7.13(a), has L_p =

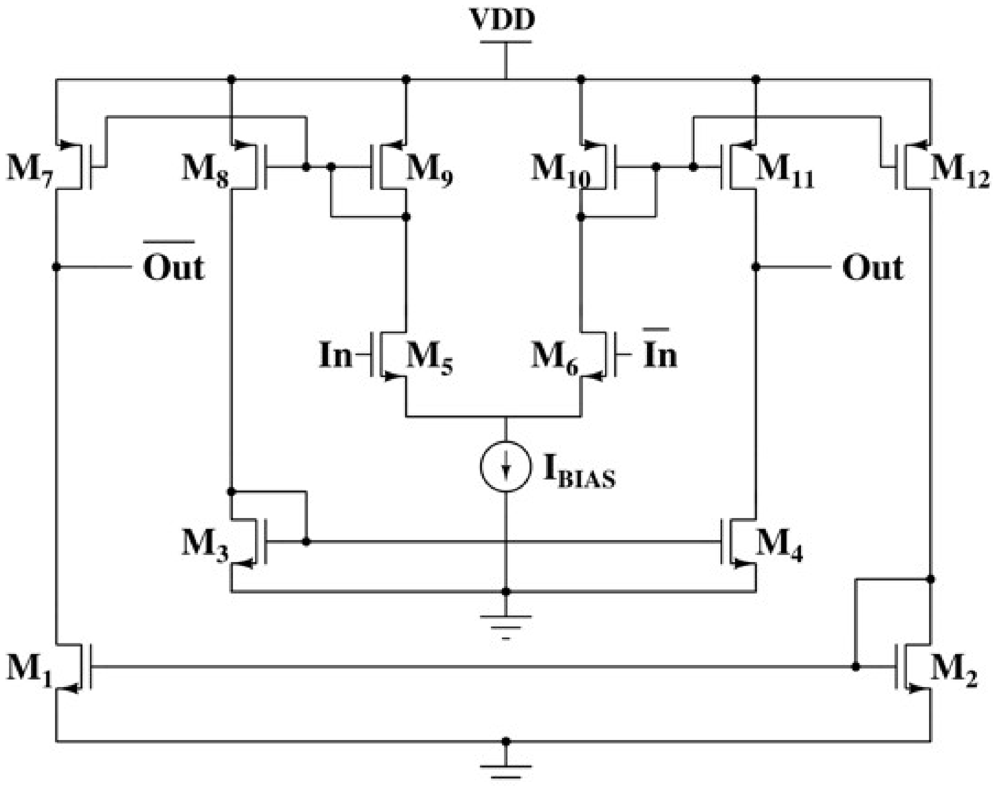


Figure 7.11: CML to CMOS converter

$M_{5,6}$	4/0.06
M_{7-12}	5/0.06
M_{1-4}	2/0.06
I_{BIAS}	1 mA

Table 7.1: Transistor Sizing

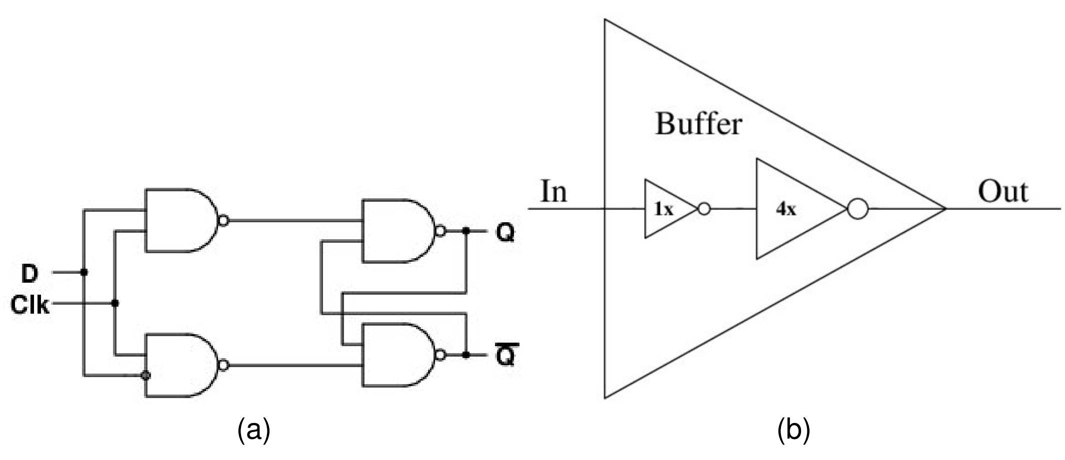
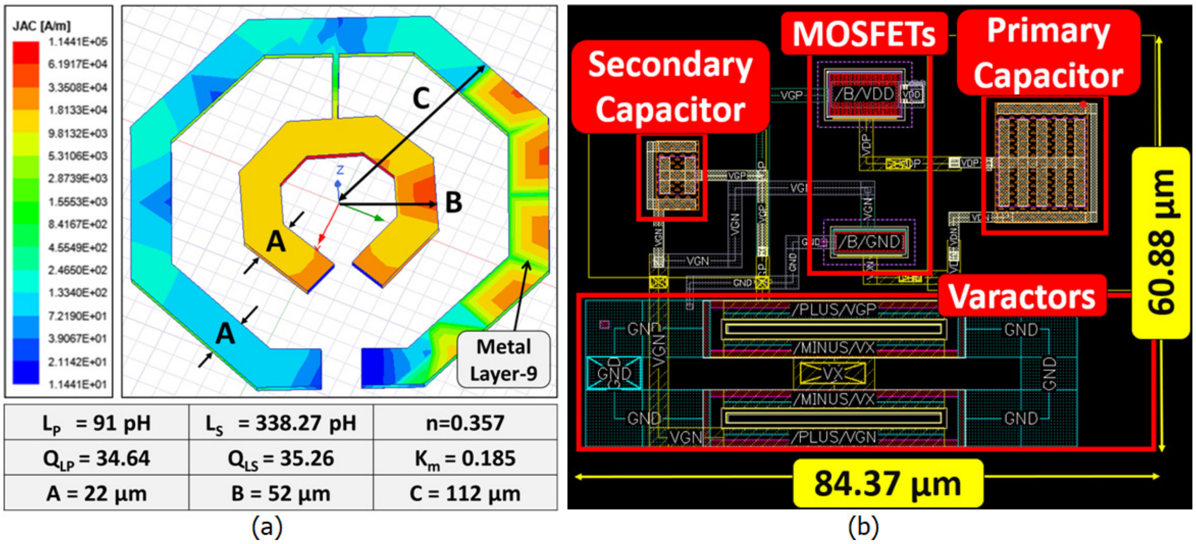


Figure 7.12: (a)CMOS D-latch (b) CMOS tapered buffer



L_P = 91 pH	L_S = 338.27 pH	n=0.357
Q_{LP} = 34.64	Q_{LS} = 35.26	K_m = 0.185
A = 22 µm	B = 52 µm	C = 112 µm

Figure 7.13: (a) Specifications of custom-designed transformer with $n < 1$ in HFSS (b) Layout in 65 nm CMOS technology (TSMC) of the proposed design

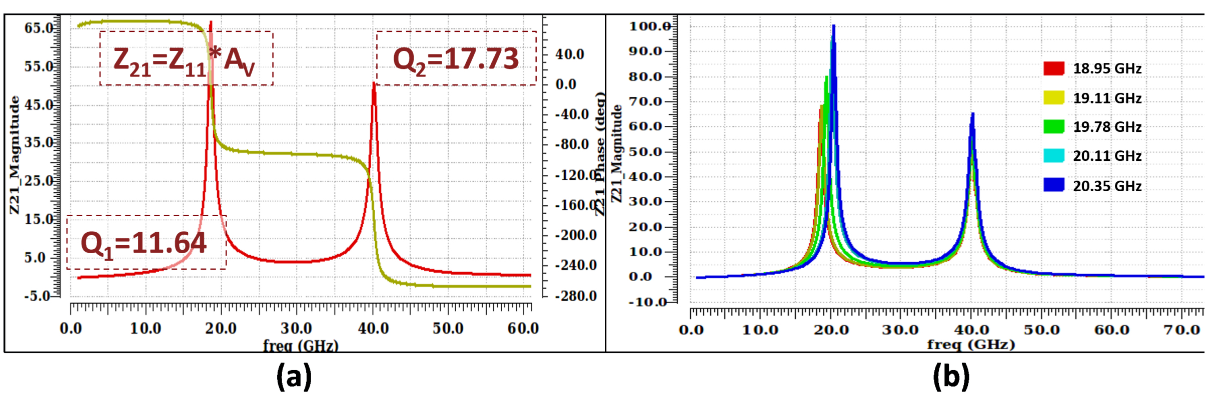


Figure 7.14: Post layout simulation results showing (a) phase and (b) magnitude values of transformer with Q_2 and Q_1 values

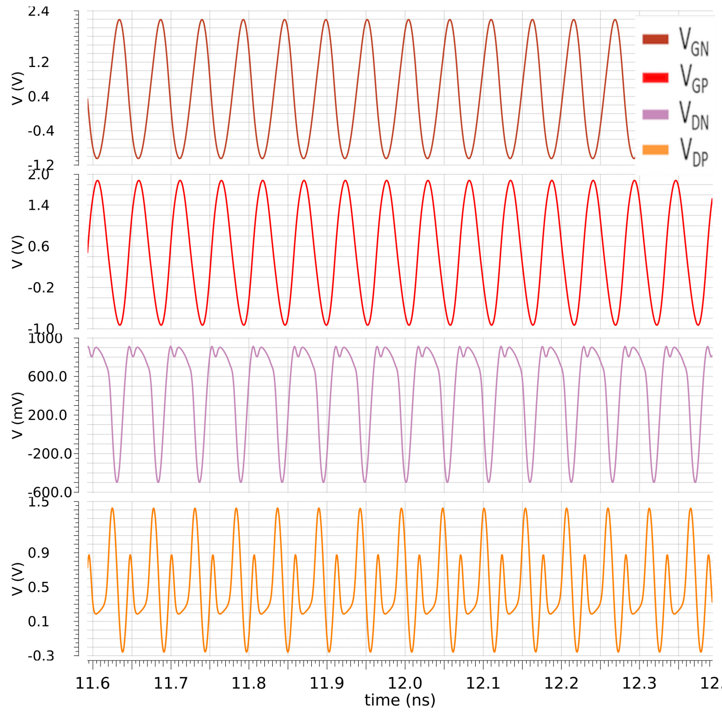


Figure 7.15: Post layout simulation results showing transient waveform showing pseudo sinusoid behaviour at drain nodes and pure sinusoid at gate nodes

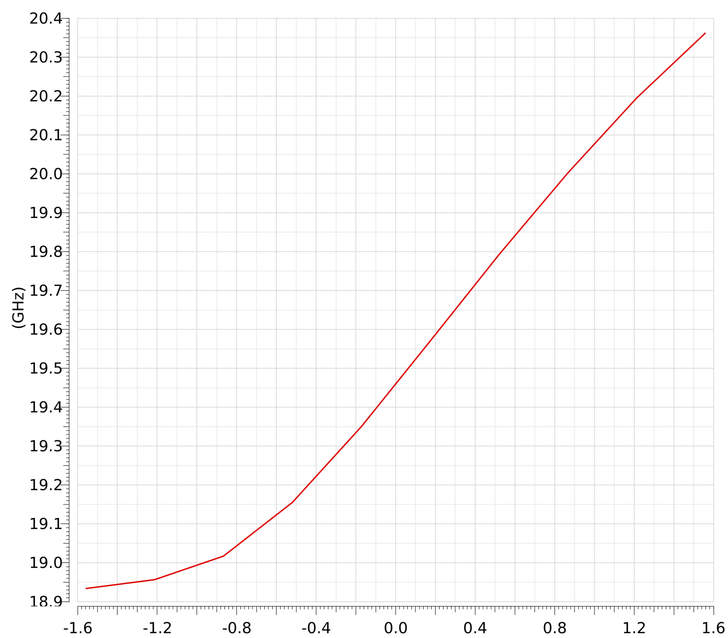


Figure 7.16: Post layout simulation results showing tuning range of 18.94 GHz to 20.36 GHz

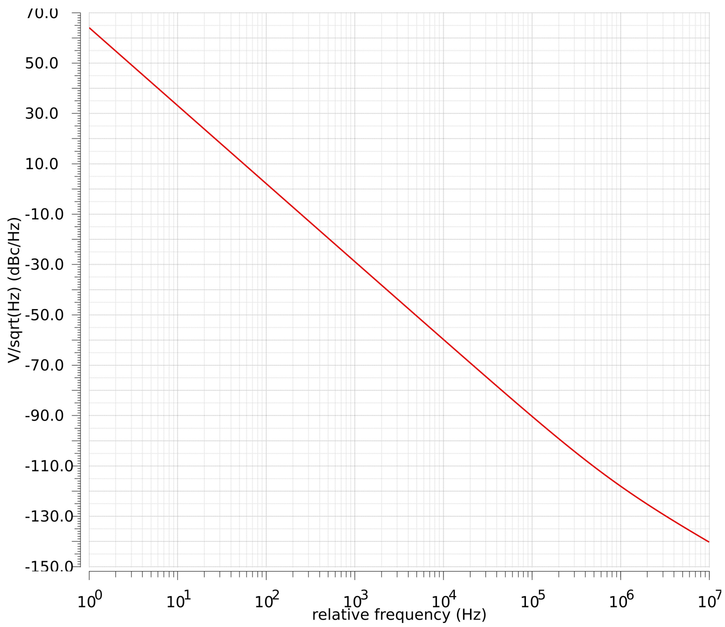


Figure 7.17: Post layout simulation results showing phase noise of -117.98 dBc/Hz at 1 MHz offset from center frequency of 18.94 GHz

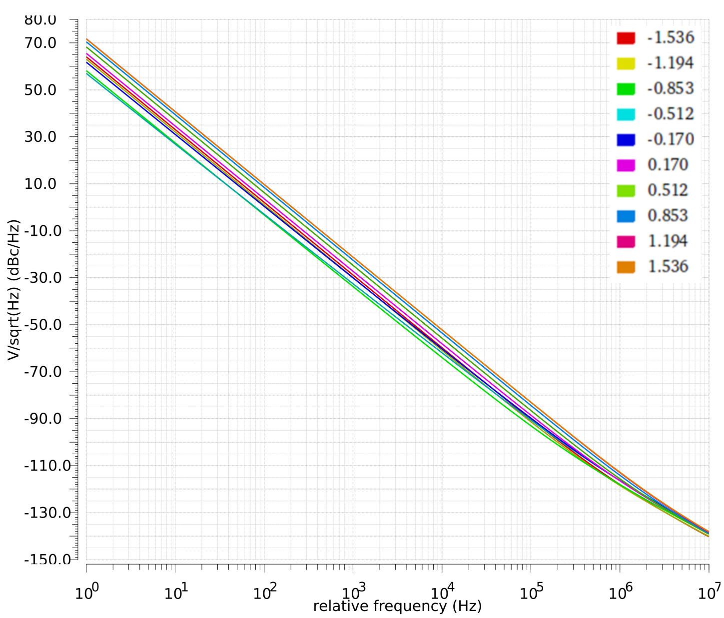


Figure 7.18: Post layout simulation results showing phase noise across tuning range

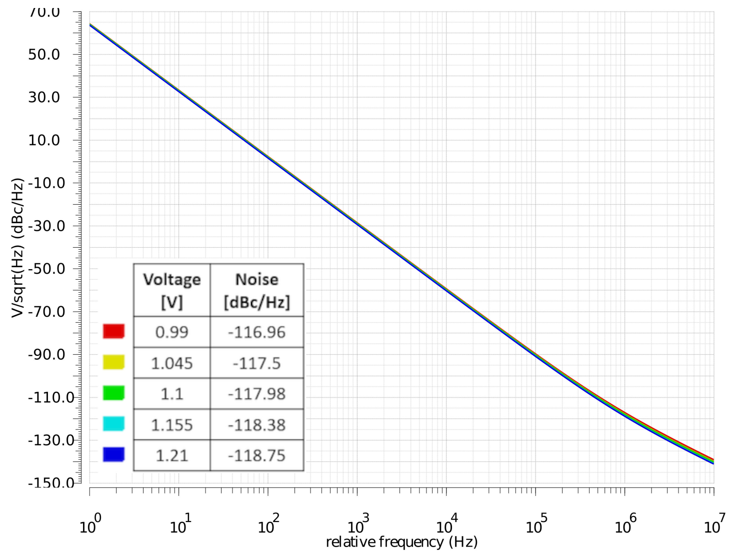


Figure 7.19: Post layout phase noise variation at 1 MHz offset with +-10% variation in supply voltage

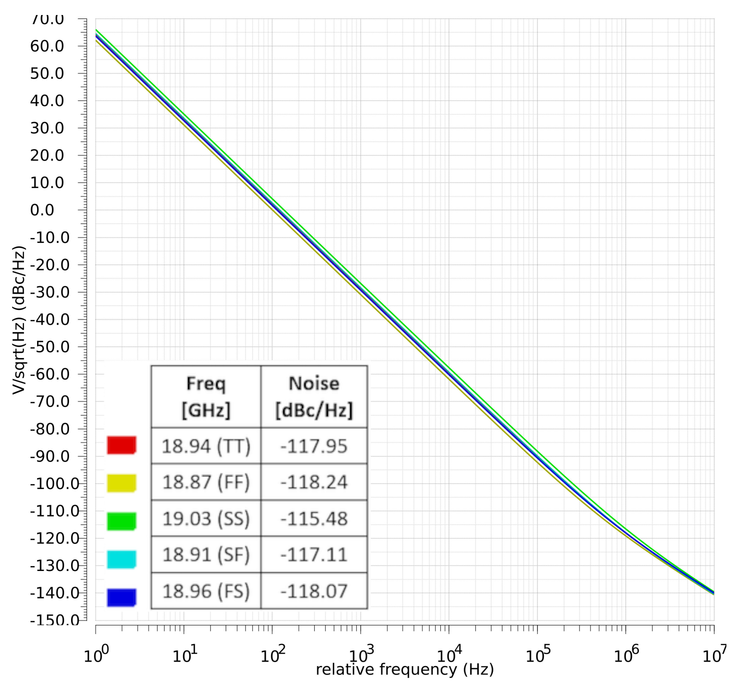


Figure 7.20: Post layout phase noise variation at 1 MHz offset across process corners

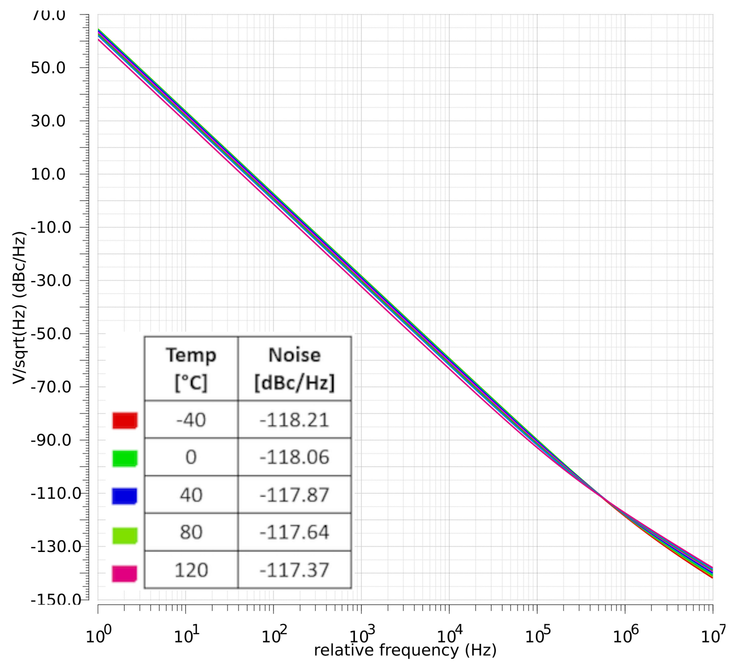


Figure 7.21: Post layout phase noise variation at 1 MHz offset with variation in temperature from -40°C to 120°C

Parameters	[51]	[52]	[53]	[54]	[55]	[56]	This Work
Measured / Simulated	Measured	Measured	Measured	Measured	Measured	Measured	Simulated
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS	180 nm CMOS	22 nm FD-SOI	65 nm CMOS	65 nm CMOS
Supply Voltage (V)	0.48	1	1	NA	0.8	0.6	1.1
Frequency (GHz)	25.48-29.92	24.62-28.66	20.7-28	17.5	24.9	25	18.94-20.36
Power Consumption (mW)	4	9.7-10.5	12.65-15.12	2.3	8.8	4.8	13.78
Phase Noise at 1MHz offset (dBc/Hz)†	-115.27	-111.4	-107.9	-110.77	-110.2	-110	-117.98
FoM (dBc/Hz) $^{\dagger\diamond}$	191.6	189.4	184.75	191.95	188.6	191.2	192.13

†Estimated from plots

$^\diamond FoM = -PN + 20log_{10}(f_{lo}/\Delta f) - 10log_{10}(P_{DC}/1mW)$

Table 7.2: Performance Summary and Comparison with State of the Art

91 pH and L_s = 338.27 pH, ensuring high Q factors for improved phase noise performance. Schematic and post-layout simulations were performed using the S-parameter file generated by HFSS. Fig. 7.13(b) illustrates the implementation of the proposed VCO in a 65nm CMOS process, where the schematic simulations indicate a current consumption of 12.52 mA from a 1.1 V supply.

In Fig. 7.14, the phase and magnitude plots of the transformer show $Q_1 = 11.64$ and $Q_2 = 23.79$, demonstrating a significant $\frac{Q_2}{Q_1}$ ratio for improved phase noise performance. Fig. 7.15 presents the transient waveforms obtained at each of the primary and secondary coil nodes, where V_{DN} and V_{DP} exhibit pseudo-sinusoidal behavior, and V_{GN} and V_{GP} comprise the 1^{st} and 2^{nd} harmonics of the drain node voltages, respectively. The transformer's passive gain amplifies the 1^{st} harmonic and compresses the 2^{nd} harmonic, resulting in sinusoidal voltages. The phase and amplitude mismatches between the two terminals caused by parasitics can be rectified through optimization of transistor sizing to ensure matching of harmonic peaks.

In post-layout simulations, as shown in Fig. 7.16, the tuning range of the VCO is 1.42 GHz (18.94 - 20.36 GHz), slightly lower than the 1.48 GHz (20.48 - 21.96 GHz) achieved in schematic simulations. This decrease in operating frequency is attributed to the presence of parasitic capacitances. However, it is accompanied by an improvement in phase noise performance, as evidenced by a change from -115.36 dBc/Hz at a 1 MHz offset from 20.48 GHz in schematic simulations to -117.98 dBc/Hz at a 1 MHz offset from 18.94 GHz in post-layout simulations. Fig. 7.17 displays the phase noise performance of the implemented VCO, which reaches -117.98 dBc/Hz at a 1 MHz offset from the oscillation frequency of 18.94 GHz.

The high $\frac{Q_2}{Q_1}$ ratio in the mmWave frequency range, as shown in Fig. 7.18, greatly enhances the VCO's phase noise performance, with a phase noise of -117.98 dBc/Hz at $f_{osc} = 18.94$ GHz and a figure of merit (FoM) of 192.13 dB. During VCO tuning, the variation in C_{var} causes a frequency mismatch between the 1^{st} and 2^{nd} harmonic impedance peaks, resulting in some flicker noise up-conversion and phase noise degradation. As depicted in Fig. 7.19, Fig. 7.20 and Fig. 7.21, the deviation in phase noise performance is 1.79 dBc/Hz for a $\pm$ 10% variation in supply voltage and 2.76 dBc/Hz across process corners. The phase noise remains below -115.48 dBc/Hz at a 1 MHz offset for all corners. Furthermore, the phase noise performance remains consistent across temperatures, with values below -117.37 dBc/Hz at a 1 MHz offset for temperatures ranging from -40°C to 120°C, highlighting the robustness of the proposed VCO.

7.4.2 Multi-Modulus Programmable Divider

The VCO of the frequency synthesizer generates an output signal whose frequency modulates linearly from 19.25 - 20.25 GHz from a 40 MHz reference crystal oscillator (f_{ref}) which is fed as input to the proposed frequency divider. According to Eq.**??** the divider can achieve a wide division ratio (N) ranging from 256 to 511 i.e, it can operate well for input frequencies varying from 10.24 to 20.44 GHz. For specific combinations of the digital control bits, the division ratio can be restricted to 481.25-506.25.

Table 7.3 shows the digital control bit sequence ($[P_0, P_1, \cdots, P_7]$) that is required to get 40 MHz (f_{ref}) at the output of divider for input frequency varying from 19.24 to 20.24 GHz. The frequency resolution (F.R) of this architecture of multi-modulus frequency divider can be formulated as

$$F.R = (\Delta N) \times f_{ref} \tag{7.2}$$

ΔN is the minimum increment of the division ratio by varying the digital control bits. From Eq. **??** considering all P_i to be constant binary bits, ΔN is equal to 1 and hence F.R = f_{ref} = 40 MHz. So, to achieve fine resolution, ΔN should be less than 1 i.e., the division ratio of the divider should be fractional. For a $N/N+1$ dual modulus prescaler divider when the digital control bit is 0 or 1, the divider divides by either N or $N+1$ respectively. To have a fractional division ratio $N+\mathcal{F}$, where $\mathcal{F}$ is the fractional part, the input bit code word should be modulated such that it divides by N for α cycles of T_{ref} and by $N+1$ for β cycles of T_{ref} where T_{ref} is the time period of the reference signal. The division ratio thus can be formulated as -

$$N+\mathcal{F} = \frac{\alpha}{\alpha+\beta}(N) + \frac{\beta}{\alpha+\beta}(N+1) \tag{7.3}$$

Depending on the fraction $\mathcal{F}$ required, the values of α and β can be chosen accordingly and so can the digital control bit be modulated. Now, the minimum increment in the division ratio (ΔN) is $\mathcal{F}$ which determines the frequency resolution of the proposed frequency divider to be -

$$F.R = \mathcal{F} \times f_{ref} \tag{7.4}$$

From Eq. 7.4, the minimum fractional change in division ratio needed for a specific frequency resolution of the synthesizer is obtained and based on that the input bit code word has to be programmed. To obtain a much finer resolution, more prescaler cells have to be used which means more input bits to be programmed. This complexity can be reduced by using the RAFS method to determine the variables α and β and program the divider efficiently. Fractional division ratios can be derived by extending the

P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	Division ratio	F_{in}(GHz)
1	0	0	0	0	1	1	1	481	19.24
0	1	0	0	0	1	1	1	482	19.28
1	1	0	0	0	1	1	1	483	19.32
.	.	.	.	.	.	.	.	.	.
0	0	0	1	1	1	1	1	504	20.16
1	0	0	0	1	1	1	1	505	20.20
0	1	0	1	1	1	1	1	506	20.24

Table 7.3: Bit code word for required ratio

formula used in Eq. 7.3 to

$$N + \mathcal{F} = \frac{c_1\alpha_1 + c_2\alpha_2 + \cdots + c_{n-1}\alpha_{n-1} + c_n\alpha_n}{\alpha_1 + \alpha_2 + \cdots + \alpha_n} \tag{7.5}$$

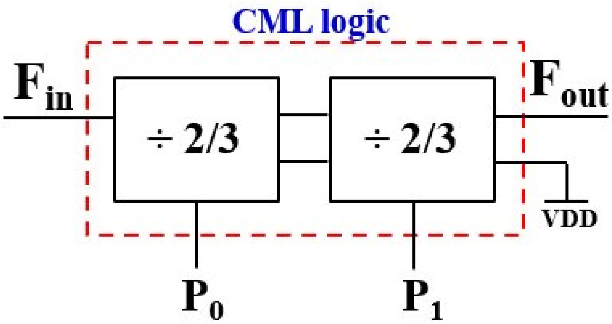
where α_i determine the number of cycles of T_{ref} the divider divides by the corresponding division ratios c_i. From Eq. 7.5 $(\Sigma\alpha_i)T_{ref}$ determines the total simulation time and for it to be 1 μs, the total number of cycles of T_{ref} is

$$\alpha_1 + \alpha_2 + \cdots + \alpha_{26} = 40. \tag{7.6}$$

Using Eq. 7.5 and Eq. 7.6, based on the division ratio required for a given input frequency, one set of values of $[\alpha_1, \alpha_2, \cdots, \alpha_{26}]$ can be obtained which determines the duration of each division ratio and accordingly set the input bit code word P which is generated using a $\Sigma - \Delta$ modulator.

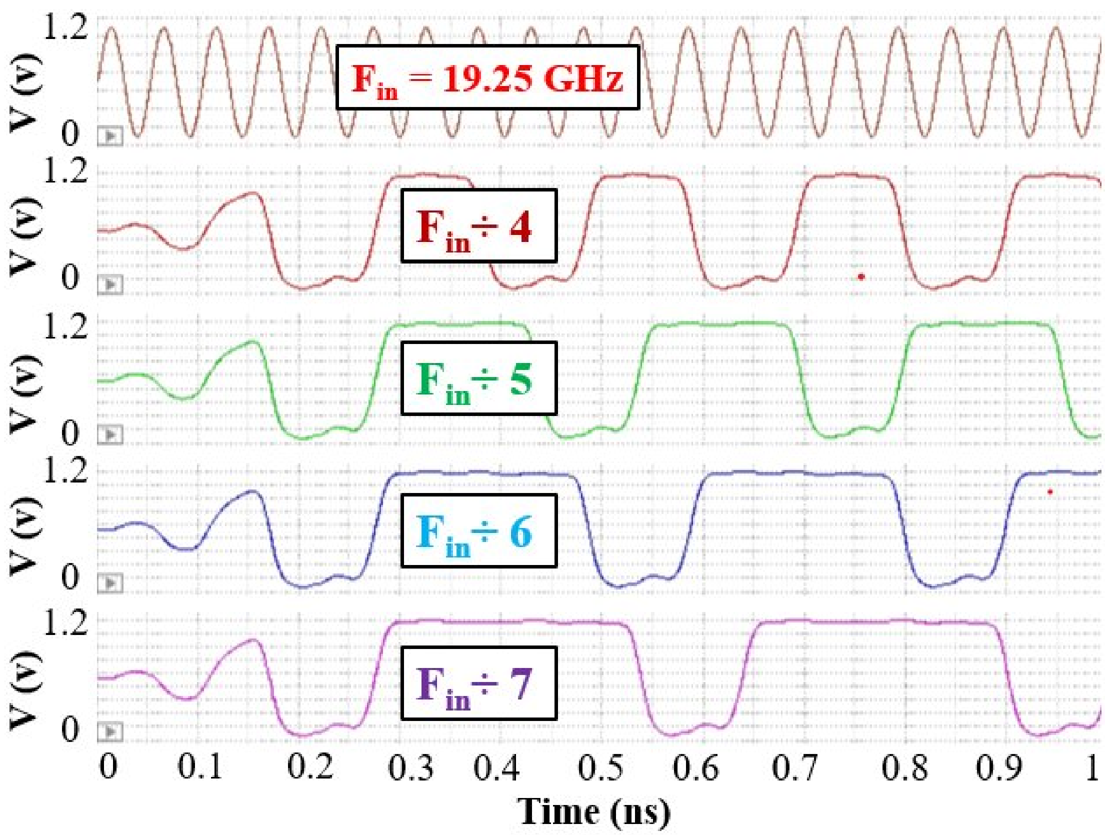
The proposed multi-modulus frequency divider shown in Fig. 7.7 has been designed and simulated in a 65 nm CMOS process. The divider achieves a frequency resolution of 1 MHz by modulating the digital control bits according to the method discussed in section IV by consuming a power of 14.1 mW for a supply voltage of 1.2 V. Fig. 7.10 shows the transient response of the CML latch when given clock signal of frequency 5 GHz and data signal of frequency 10 GHz. Fig. 7.22(a) shows two 2/3 prescaler cells in cascade employing CML topology. Each of the prescaler cells is followed by a CML buffer. This divider can realise all the division ratios from 4 (2^n) to 7 ($2^{n+1} - 1$) based on the digital control bits ($[P_0, P_1]$) as shown in Fig. 7.22(a). The transient response plots of the divider output (F_{out}) have been illustrated in Fig. 7.22(b) for an input sinusoidal signal (F_{in}) of frequency 19.25 GHz.

Fig. 7.23 shows the digital control bits ($[P_0 \ to \ P_4]$) which have been modulated to achieve the required fractional division ratio (N + $\mathcal{F}$) for different input frequencies. The other input bits ($[P_5 \ to \ P_7]$)



P_0	P_1	Division Ratio
0	0	4
1	0	5
0	1	6
1	1	7

(a)



(b)

Figure 7.22: CML logic based 2 stage 2/3 prescaler cell showing frequency division (4-7) for given input signal $F_{in} = 19.25$ GHz

Parameters	[60]'2010	[61]'2019	[62]'2021	[63]'2021	[15]'2015	This work
Operating frequency	77-77.6 GHz	26∼44 GHz	22 GHz	13∼18 GHz	17.9 GHz	**19.25∼20.25 GHz**
Technology	90 nm CMOS	55 nm	180 nm SiGe BiCMOS	65 nm CMOS	40 nm CMOS	**65 nm CMOS**
Supply Voltage	1.2 V	1.2 V	3.3 V	1.2 V	1.1 V	**1.2 V**
Power consumption	100 mW	15.2 mW	N/A	42 mW	245 μW	**14 mW**
Division ratios	1024	256∼508	1∼511	16∼255	32/33	**256∼511**

Table 7.4: Performance comparison of MMFD operating around 20 GHz

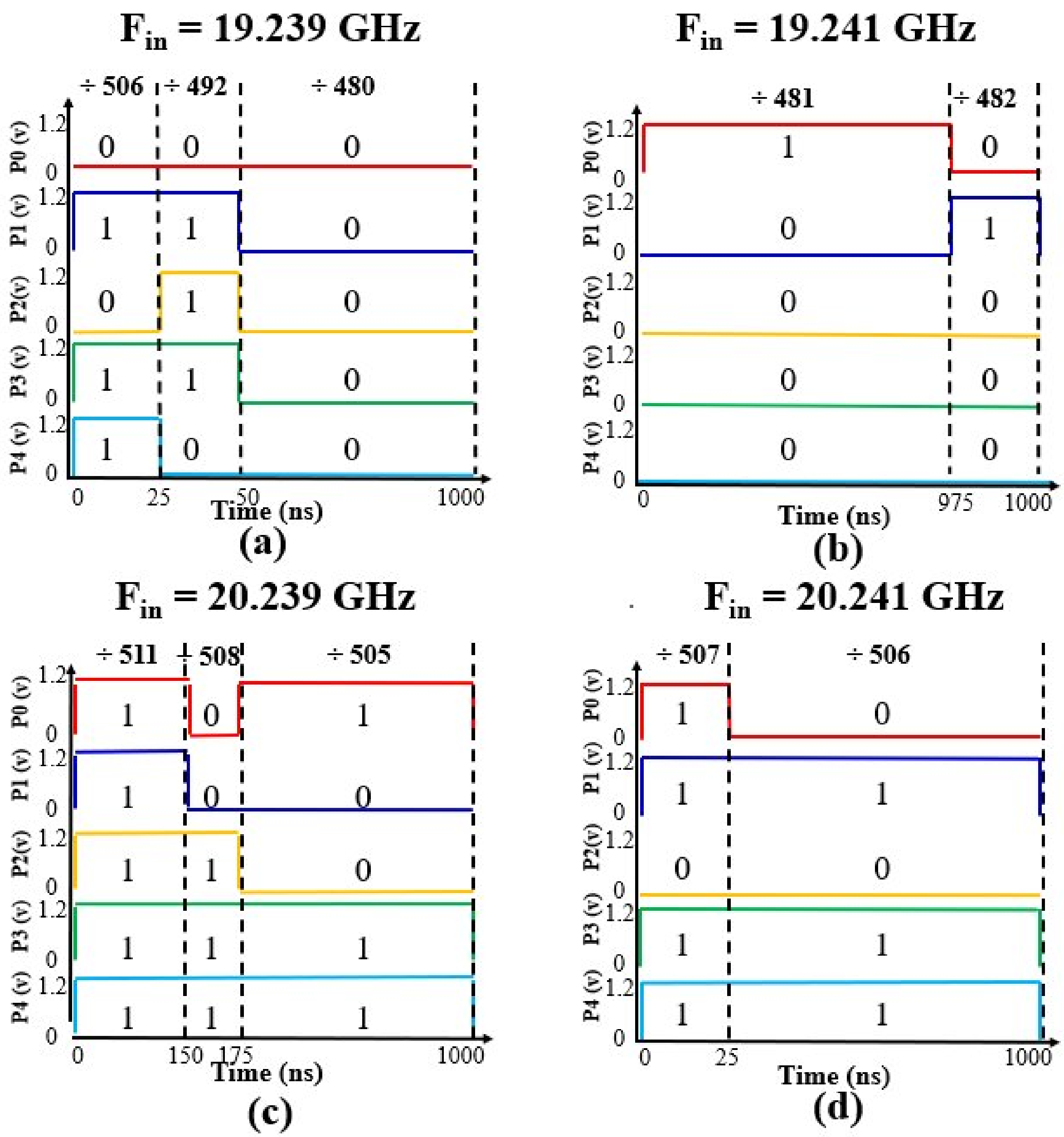


Figure 7.23: Input bit code word for different input frequencies (a) 19.239 GHz (b) 19.241 GHz (c) 20.239 GHz (d) 20.241 GHz

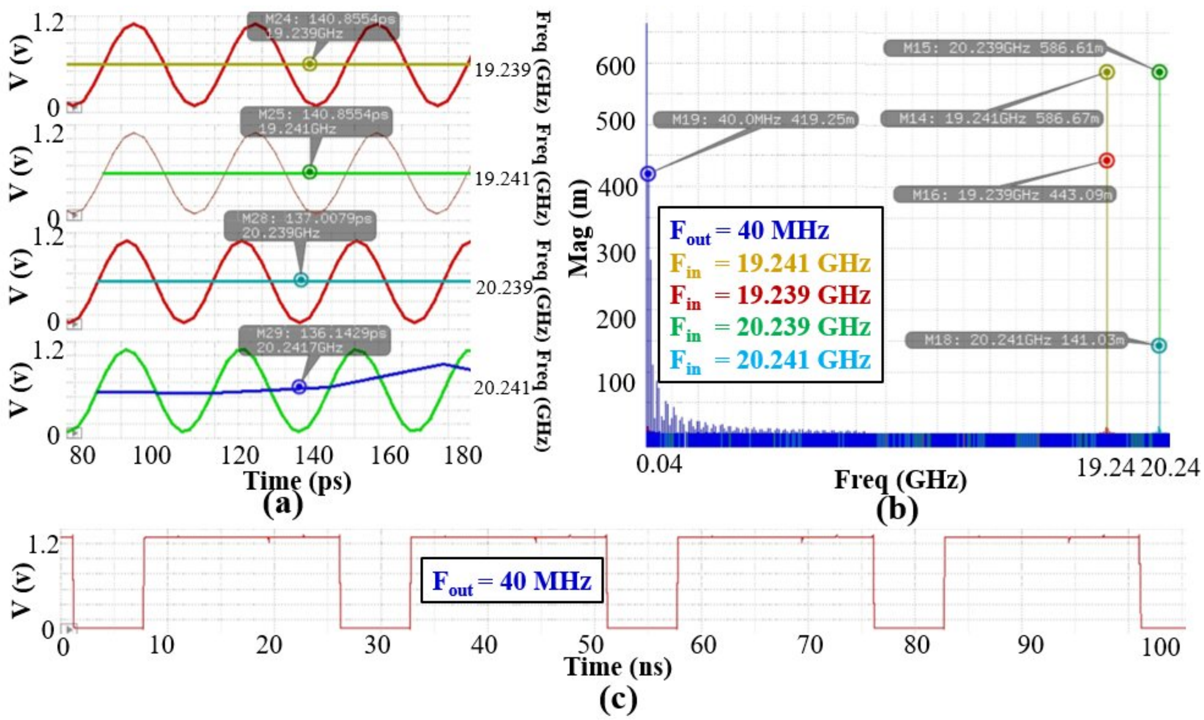


Figure 7.24: (a) Transient plots of various input signals (b) DFT plot for the input signals and 40 MHz output signal. (c) Transient response of the output signal.

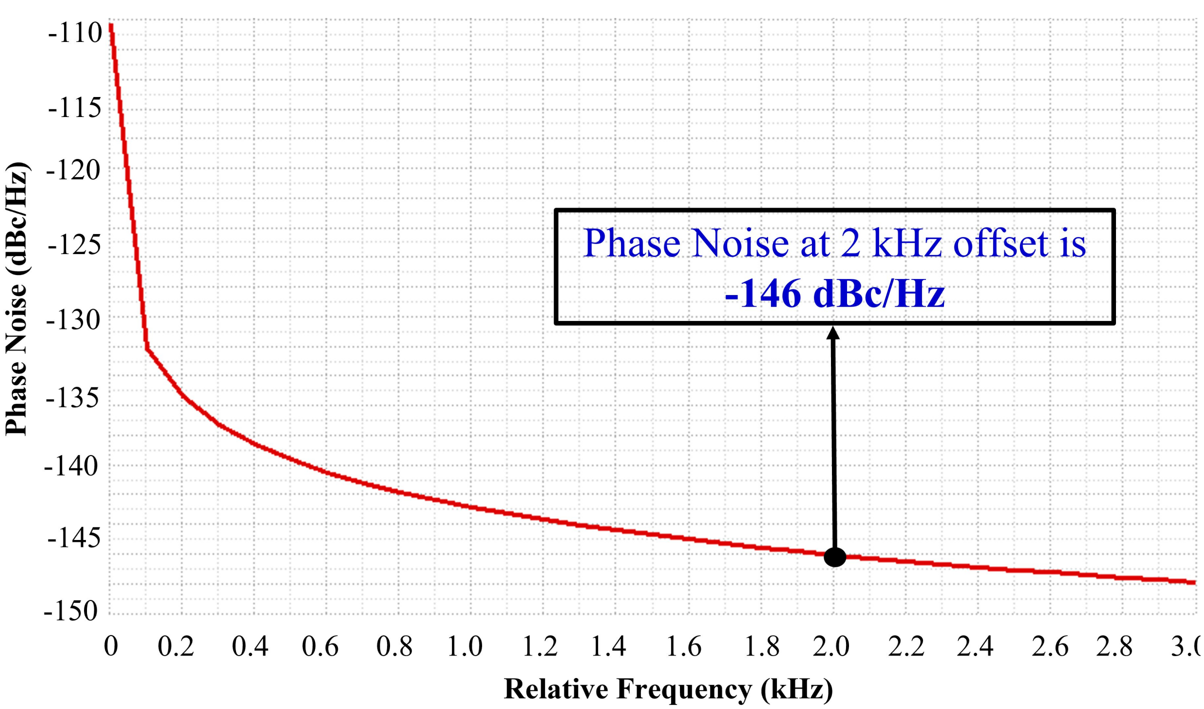
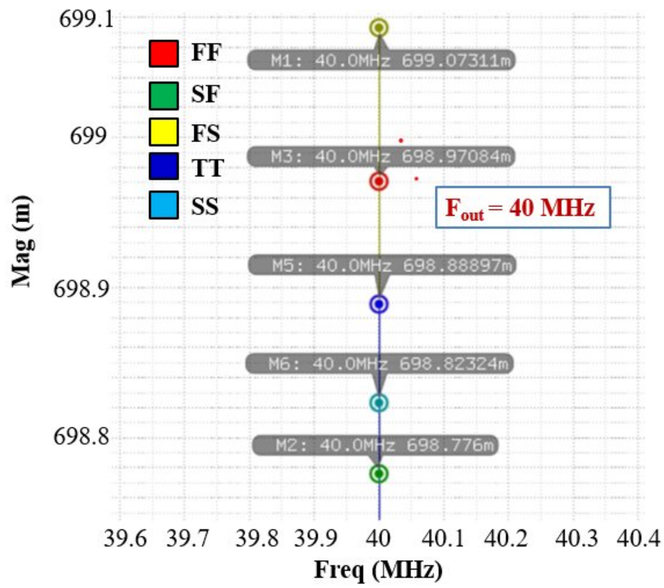


Figure 7.25: Phase noise of the divider measured at an offset of 2 kHz



(2).jpg (2).bb

Figure 7.26: DFT plot of output across different process corners

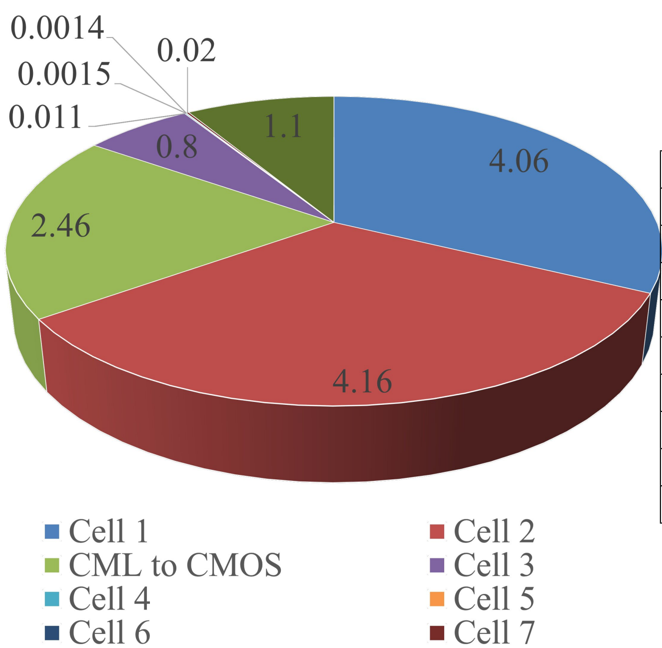


Figure 7.27: Power distribution across various blocks

Blocks	Power (mW)
CML - Cell 1	4.06
CML - Cell 2	4.16
CML to CMOS	2.46
CMOS - Cell 3	0.8
CMOS - Cell 4	0.011
CMOS - Cell 5	0.0015
CMOS - Cell 6	0.0014
CMOS - Cell 7	0.02
CMOS - Cell 8	1.1

Table 7.5

are set to 1 according to Table 7.3. Fig. 7.24 shows the transient and DFT plots of the input and output of MMFD for input frequencies of 19.239, 19.241, 20.239, 20.249 GHz achieving an output of frequency 40 MHz. The phase noise of a divider with a division ratio of N changes from the ideal (PN = -110 dBc/Hz) by $10\log_{10} N$ (ΔPN). To measure ΔPN the proposed divider is given a sinusoidal signal of frequency 20 GHz to output a signal of frequency 40 MHz (division ratio (N) = 500). ΔPN turns out to be nearly 30 which satisfies this criterion and produces a phase noise of -146 dBc/Hz at an offset of 2 kHz as shown in Fig. 7.25. Fig. 7.26 shows the DFT plot of the divider output across various process corners - FF, FS, SF, TT and SS. For the SS corner, more current is required in the CMOS tapered buffers to drive the load so the supply voltage is increased to 1.5 V. Fig. 7.27 shows the distribution of the total power consumed by all the blocks - CML-based 2/3 divider cells, CMOS-based 2/3 divider cells and the CML to CMOS converter and the same has been tabulated in Table 7.5.

7.5 Summary

This chapter presents the design and analysis of a transformer tank-based voltage controlled oscillator (VCO) operating in the mmWave frequency range, specifically targeting 77 GHz FMCW chirp synthesizers. The main focus of the design is to achieve low phase noise performance. To accomplish this, a unique approach of utilizing a transformer with a turn ratio of less than 1 (n ¡ 1) is proposed, and a thorough analysis supported by simulation results is provided. The proposed VCO design is implemented in a 65 nm CMOS technology. The post-layout simulations demonstrate excellent performance, with a figure-of-merit (FoM) of 192.13 dBc/Hz and a phase noise level of -117.98 dBc/Hz at a 1 MHz offset while operating at a frequency of 18.94 GHz. The VCO achieves a tuning range of 1.42 GHz (18.94-20.36 GHz) and consumes a power of 13.78 mW from a 1.1 V supply. These results highlight the effectiveness of the proposed design in achieving the desired low phase noise performance for mmWave applications. This chapter also presents a multi-modulus programmable frequency divider for a 77-81 GHz FMCW radar transceiver. Eight 2/3 dual modulus prescalers in cascade have been used to realize a wide division range of 256-511 which upon programming the input code word appropriately can be modelled to generate output VCO frequencies varying linearly from 19.25 to 20.25 GHz with a fine-tuning range of 1 GHz. The proposed divider achieves a frequency resolution of 1 MHz shown by portraying frequency and transient responses for 19.239, 19.241, 20.239, 20.241 GHz and the corresponding input bit patterns. The phase noise measured at the output of the divider is -146 dBc/Hz at an offset of 2 kHz. These results have been validated and verified over various process corners. A significant amount of power can be optimized using the proposed design for the frequency divider.

Chapter 8

CNN based Portable and Real Time Object Classification System using mmWave Radar Point Cloud Data for Road Safety Applications

8.1 Introduction

Recent advancements in millimeter-wave (mmWave) radar technology have opened up new possibilities in various fields. These radars, characterized by their high chirp bandwidth and slope, offer exceptional accuracy in detecting the range, velocity, and angle of objects [37]. As a result, they find applications in diverse areas such as road safety infrastructure, healthcare monitoring, security gate monitoring, gesture recognition, vibration monitoring, and fitness tracking [64]-[68].

When it comes to road safety and monitoring infrastructure, conventional technologies rely heavily on cameras and lidar systems. However, these systems often struggle to perform optimally in challenging weather conditions such as heavy rain, snow, or fog [69], [70]. One of the significant advantages of FMCW radars is their ability to penetrate fog, smoke, and snow with ease [73], [74]. This feature makes them highly suitable for widespread deployment in road monitoring applications. Alert systems utilizing FMCW-based object classification techniques can be employed to notify drivers, pedestrians, and traffic control rooms under adverse weather conditions, thereby maintaining safety even in conditions of poor visibility. Furthermore, the low cost and ease of implementation of FMCW radars make them an ideal choice for large-scale deployment in road monitoring, as depicted in Fig. 8.1. By incorporating FMCW radars into road safety infrastructure and monitoring, the risk of accidents can be reduced, and overall safety for drivers, passengers, and pedestrians can be improved. Road safety audits play a vital role in developing safer road networks [71], [72]. The data collected from FMCW radars regarding the movements of different vehicles and pedestrians in various areas can provide valuable insights for engineers in designing safer road networks that cater to specific vehicle classes, ensuring smoother traffic

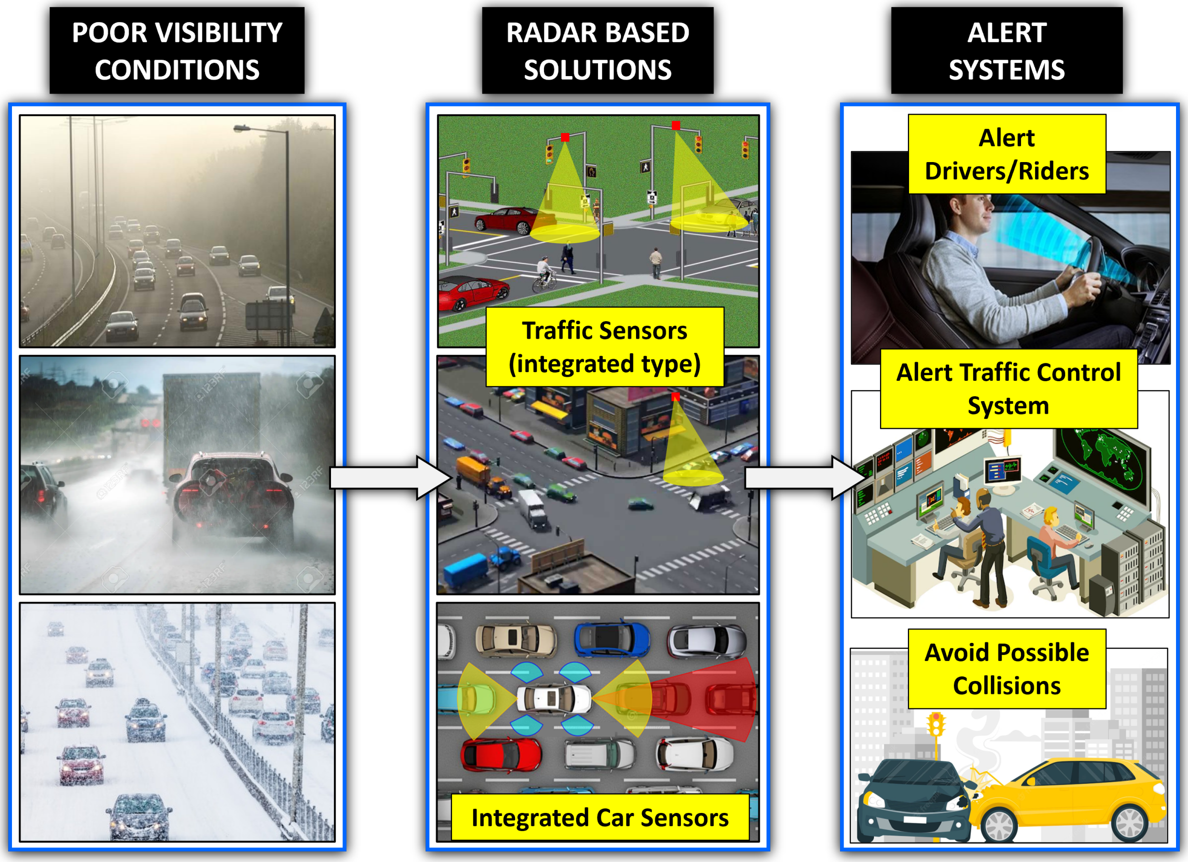


Figure 8.1: Radar based systems for traffic assistance under poor visibility conditions

flow. Compared to ultrasonic radars, FMCW radars offer higher spatial resolution while being compact and lightweight, making them an excellent choice for developing road safety audit tools in conjunction with existing CCTV cameras.

Numerous studies have explored object classification techniques using FMCW radar data in combination with machine learning/artificial intelligence (ML/AI) methods. SVM-based human-vehicle classification systems utilizing FMCW radars were presented in [75], [76], and [77]. These approaches extracted features from range and velocity profiles of targets, which were then used by the SVM for classification. While this approach suffices for distinguishing humans and vehicles since their velocities differ significantly in most cases, it may not be suitable for classifying vehicles into specific categories such as two-wheelers and four-wheelers, as their velocities can be similar. A more effective approach for object classification is the utilization of convolutional neural networks (CNNs), a type of deep learning network. Several studies [78], [79] have demonstrated that CNNs trained on micro-Doppler signatures and range-angle heatmaps can achieve high accuracy in object classification. However, these techniques rely on raw radar data, which can be challenging to access and may necessitate expensive data acquisition boards, making them less cost-efficient. Additionally, the use of data acquisition boards can impede real-time functionality, which is crucial for certain applications. This work proposes a proof of concept for a real-time target classification system based on a low-cost 77 GHz FMCW radar sensor.

The chapter is organized as follows: The architecture of the proposed system is presented in Section 8.2. In Section 8.3, the data collection setup and dataset are discussed initially, followed by a detailed explanation of the methodology used to choose the most suitable convolutional neural network (CNN) for this work. Verification results for the chosen CNN model are also provided in this section. Section 8.4 details the system implementation, including the overall system accuracy and corresponding results. Discussions on future related works are also presented in this section. Finally, conclusions are drawn in Section 8.5.

8.2 Overview of Proposed Architecture for Object Classification

The classification of objects using FMCW radar can be achieved using various commercially available radars such as those by IWR [82], Analog Devices [83], and Infineon [84]. This can be accomplished by utilizing either the data from the digital signal processor (DSP) or the raw data from the analog-to-digital converter (ADC).

One commonly employed approach for object classification involves the utilization of Fast Fourier Transform (FFT), as illustrated in Fig. 8.2. FFT is performed on the raw data acquired using a data acquisition board, which generates frequency spectra from which information about the range, velocity, and angle of the target can be extracted [68]. This information is then utilized to generate a point cloud that is employed for object classification. However, the FFT-based strategy has certain limitations, including increased latency and the cost associated with acquiring and processing raw data. While this approach offers high accuracy, implementing it in a real-time system can be challenging.

The proposed methodology, depicted in Fig. 8.3, eliminates the need for a separate data acquisition unit. Instead, it leverages the integrated radar digital signal processor (DSP) to directly obtain point cloud data. This eliminates the requirement for separate raw data acquisition and processing. The point cloud data is acquired using the Texas Instruments (TI) mmWave ROS package [86] integrated with the Robot Operating System (ROS), a specialized set of software libraries and tools designed for robot and

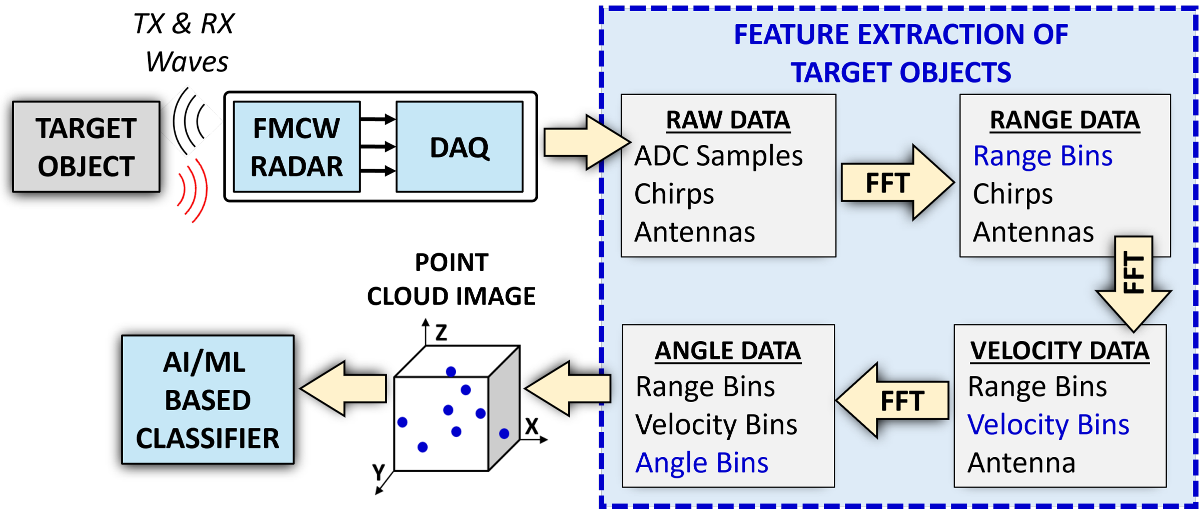


Figure 8.2: Commonly used FFT based object classification system

sensor applications. This real-time data collection and processing capability enables the development of a real-time object classification system. The acquired point cloud data is preprocessed to generate 3D point cloud images, which are then used for feature extraction by a lightweight convolutional neural network (CNN) model. This enables the model to classify objects into different classes.

By adopting this approach, the overall system cost and latency are reduced, and the system becomes more portable. To further minimize latency, it is crucial to optimize the CNN model in terms of memory and processing requirements while maintaining high accuracy. The following section outlines the methodology employed to select an appropriate CNN model that satisfies these criteria.

8.3 Data Collection and CNN-based Classifier

Convolutional Neural Networks (CNNs), a type of artificial neural network, have gained widespread use in image classification tasks due to their ability to extract relevant features from image data. However, deep learning-based CNNs often consist of numerous layers and parameters, demanding significant computing resources for training and deployment. When it comes to classifying point cloud images on mobile platforms, these models need to be optimized to meet accuracy, memory, and processing requirements within the constraints of limited resources.

This section introduces various CNN options that can be employed for point cloud image-based classification. The selection process involved conducting experiments on the collected dataset to validate the

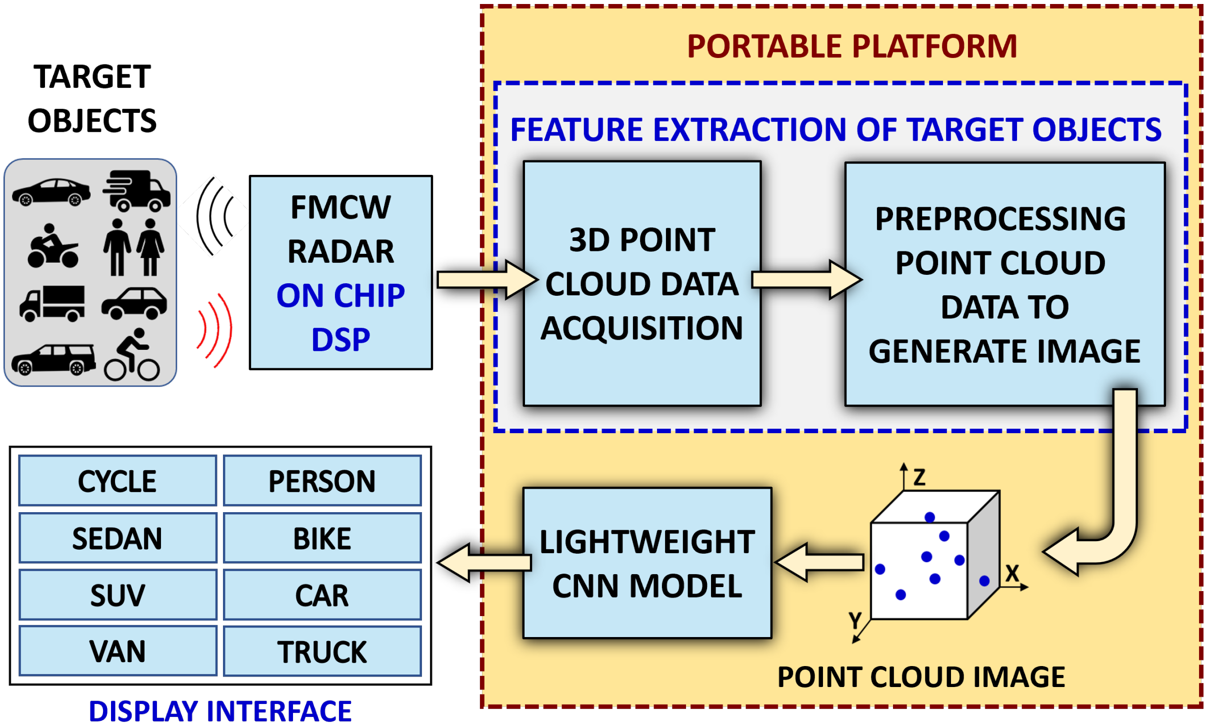


Figure 8.3: Proposed system for object classification

suitability of each model. Ultimately, the most suitable model for this study was chosen after extensive deliberation on its feasibility and compatibility with the given constraints.

8.3.1 Data Collection

The data collection setup consists of TI's IWR1843BOOST board connected to a laptop running the TI mmWave ROS package and the data collection scripts. Table 8.1 shows the configuration of different radar parameters.

In the data collection process, depicted in Fig. 8.4, objects of interest were positioned in front of the setup, and the radar was either moved around the object or the object itself was moved in front of the radar. This approach allowed for the collection of point cloud data from various angles, ensuring diversity in the dataset. The point clouds were generated using ROS on a laptop, and a Python script running on the same laptop saved the respective point cloud data as a Numpy array file. The aim was to create a dataset that encompasses a wide range of environmental conditions, enabling robust training of the CNN model and accurate classification of objects under different scenarios.

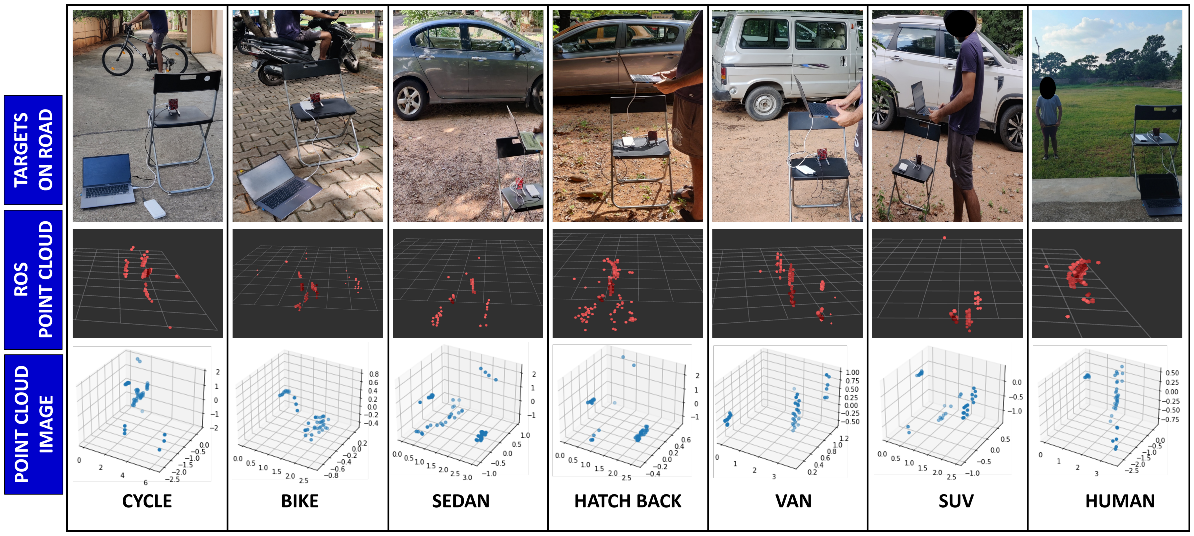


Figure 8.4: Dataset collection for all classes

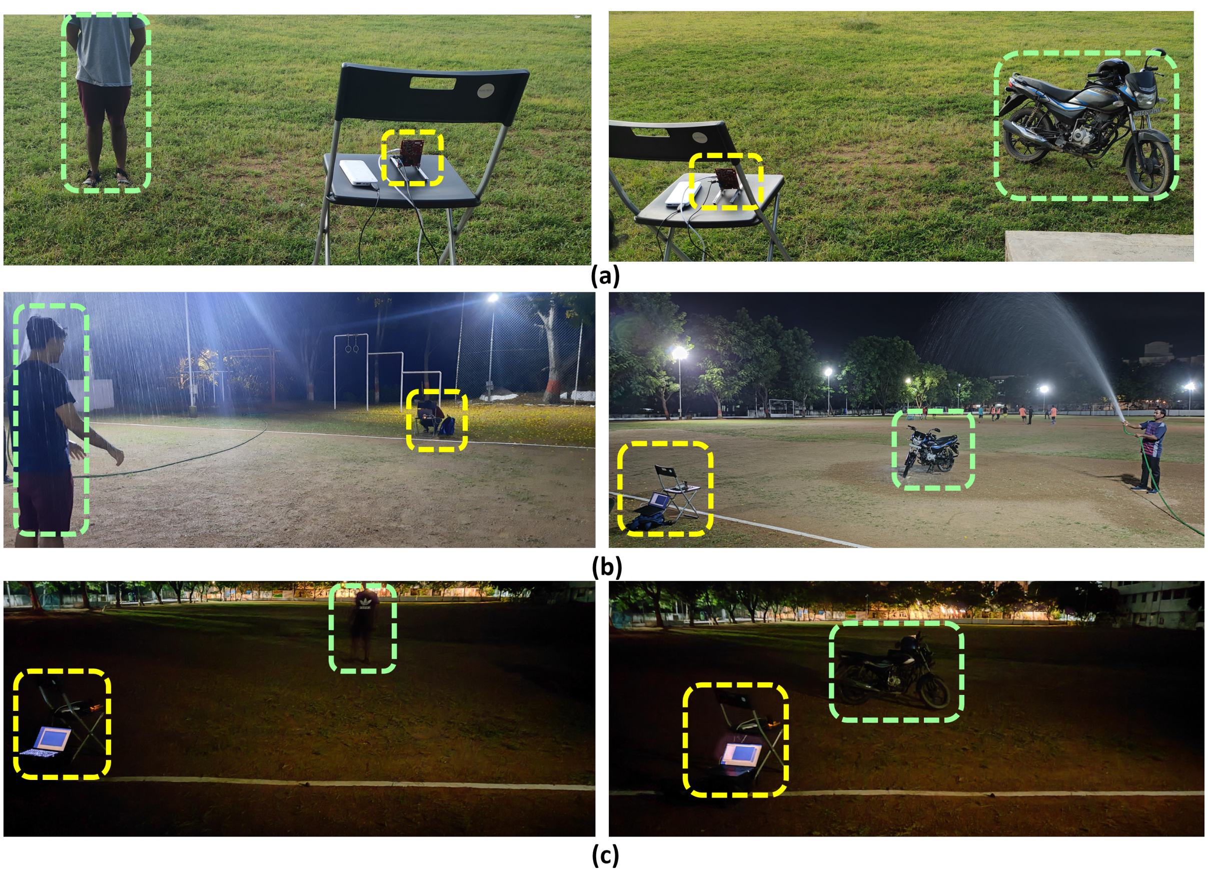


Figure 8.5: Different environments for data collection (a) normal light (b) rainy condition (c) poor light

Radar Parameter	Value
Transmit Antenna	3
Receive Antenna	4
Starting Frequency	77 GHz
Stop Frequency	80.6 GHz
Bandwidth	3.6 GHz
Frequency Slope	29.982 MHz/μs
Chirps Per Frame	64
Sampling Rate	6 Msps
Samples Per Chirp	128
Frame Rate	10 fps

Table 8.1: Radar configuration parameters

Data collection took place at multiple locations within the institute campus and the surrounding roads. Fig. 8.5 illustrates the various experiments conducted to record data in different circumstances, including simulated rain (using a water pipe), strong winds, and low-light conditions. The dataset comprises grayscale images, representing the projection of the three-dimensional point clouds onto a two-dimensional plane. The focus is solely on the location of the points within the point cloud, disregarding the background pixels.

8.3.2 CNN Choices for Point Cloud Image Based Classification

Several CNN architectures are available for point cloud image classification, including VGG16[94], VGG19, ResNet-50, ResNet-18[95], Squeezenet[96], MobileNetV2[97], YOLO, and AlexNet, among others. However, certain models like VGG16, VGG19, and YOLO require significant computational resources, making them unsuitable for portable systems with limitations on processing power and memory. On the other hand, ResNet-18, Squeezenet, and MobileNetV2 are relatively lightweight models that offer acceptable accuracy by employing various techniques.

The data was preprocessed and divided into training and testing sets. To facilitate this, the images were converted to grayscale, and the background pixels were set to zero. For testing purposes, twenty randomly selected images from each class were reserved, while the remaining data was split into an 80:20 ratio for training and validation. A mini-batch size of 32 was used during training, and the learning rate was fixed at 0.05 for 100 epochs.

There is a class imbalance issue, with classes such as truck, van, and sedan having fewer samples compared to the other classes. To address this, a sampler was employed to balance the batches used

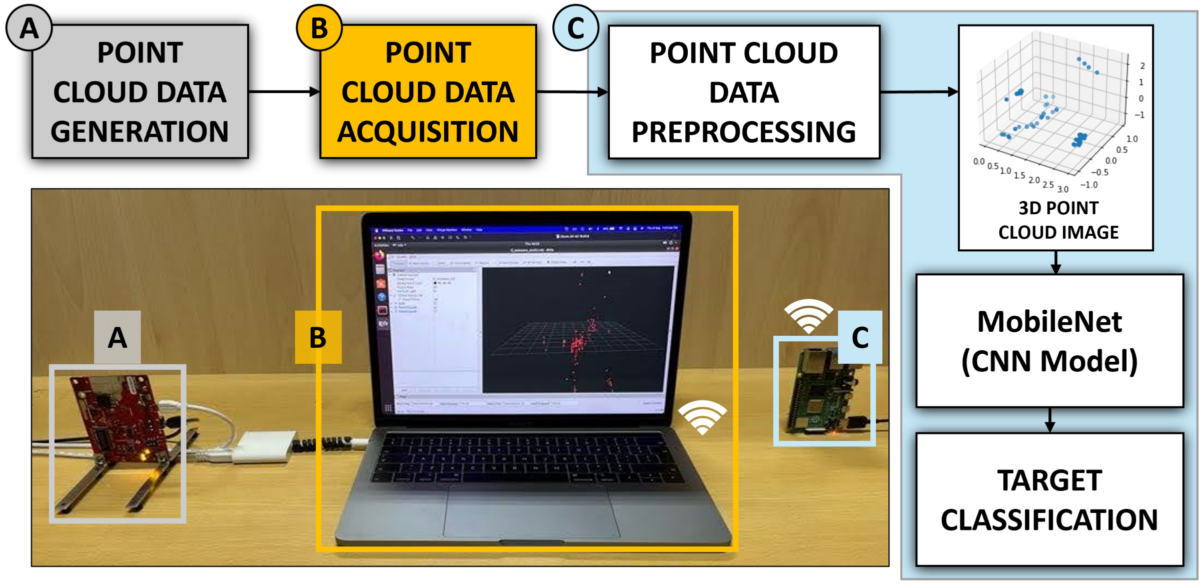


Figure 8.6: Proof of concept for proposed portable system

for training. Image augmentation techniques were applied, including rotating each image by a small angle around the z-axis and flipping images horizontally. Additionally, weighted loss functions were implemented, where the weights were inversely proportional to the number of samples in each class. These measures were taken to prevent the model from overfitting to classes with a larger number of samples, ensuring accurate and reliable results for all classes.

Both MobileNetV2 and ResNet-50 demonstrated satisfactory accuracy across all classes. However, SqueezeNet exhibits low accuracy, particularly for vans, and inferior performance for trucks and hatchbacks. MobileNetV2 requires significantly less memory and time for evaluating a given input in comparison to ResNet-50. Hence, MobileNetV2 is selected as the optimal choice of CNN-based classifier for this portable object classification system.

8.4 Hardware Implementation and Results

The proof-of-concept implementation for object classification is depicted in Fig. 8.6. The sensing component of the system utilizes TI's IWR1843BOOST [82], an evaluation board featuring a single-chip 76-GHz to 81-GHz industrial FMCW radar sensor. The received signal is processed by the on-chip DSP to generate point cloud data. The radar board is connected to a laptop running ROS, with the data being captured using TI's mmWave radar ROS node and published as a ROS topic. A Python script

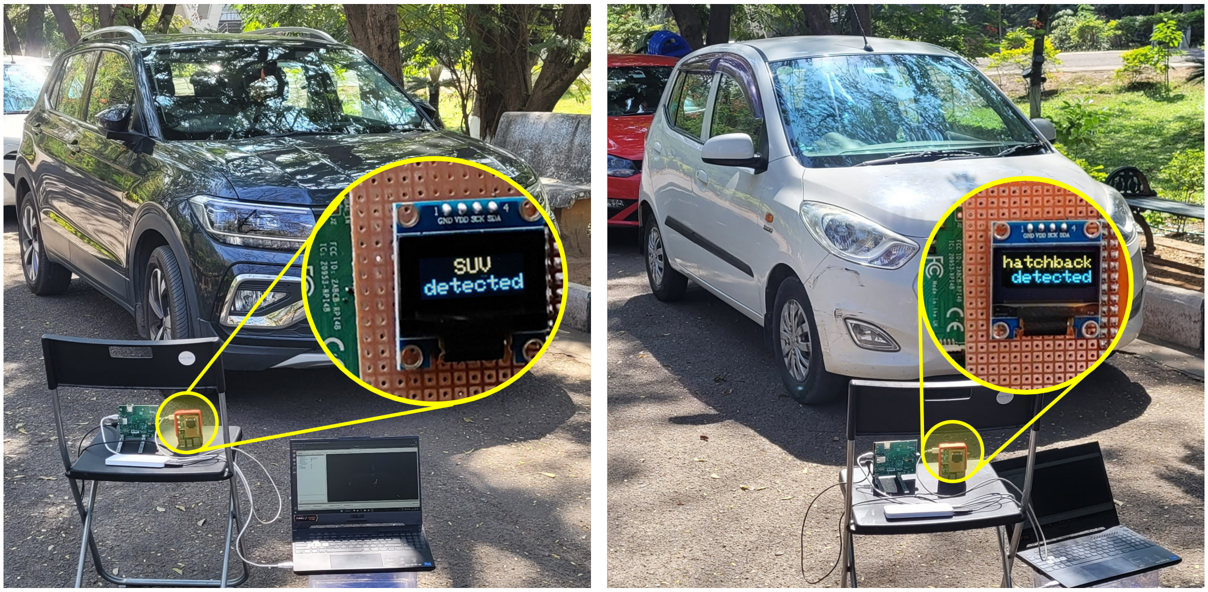


Figure 8.7: SUV and Sedan classification by the system

captures the data from this specific ROS topic and further processes it by converting it into a Numpy array that consists solely of the point cloud data. 3D point cloud images are then generated from this data using Matplotlib.

The laptop and a Raspberry Pi 4 Model B (RasPi) are connected over a wireless network. Data transfer is facilitated through an HTTP server. The trained CNN model is loaded onto the RasPi, which receives the point cloud images over the wireless network and performs classification using the trained model. It is important to note that the current limitation in terms of overall portability arises from the lack of support for ROS 2 versions by the TI mmWave radar ROS package, as well as the discontinuation of ROS 1 for newer versions of Ubuntu that are compatible with the latest RasPi boards. This issue will be addressed once the TI mmWave radar ROS package is ported to ROS 2.

To evaluate the proposed methodology, Table 8.2 provides a comparison with other similar works focusing on on-road object classification. This work achieves sufficinetly high accuracy of 85% across 3 classes namely human, 2-wheelers and 4-wheelers while optimizing the classification system for a portable platform.

8.4.1 Limitations & Future Works

During the development of this system, a significant challenge was the lack of an available 3D radar point cloud datasets for benchmarking the hardware and models. To overcome this limitation, a custom

Ref.	System Description	Type of Input	Type of AI/ML Model	Model Size(MB)	No. of Classes	Avg. Accuracy
[87]	1) Camera 2) mmWave Radar (24 GHz)	1) Radar Data 2) Video Data	Alex-Net CNN	233	6	98 %
[88]	1) mmWave Radar (77 GHz)	1) 2D Radar Point Cloud Data	SVM	-	2	94.5%
[91]	1) mmWave Radar (77 GHz)	1) Range-Angle Heatmap	YOLO	235	3	94.53%
[93]	1) Camera 2) mmWave Radar (77 GHz)	1) Camera Data 2) Azimuth Angle 3) Distance 4) Radar Cross Section	YOLO & Custom NN	-	3	60.0%
This Work	1) mmWave Radar (77 GHz)	1) 3D Point Cloud Image	MobileNetV2	10.65	3	85%

Table 8.2: Comparison with other recently reported related works

dataset is being created for the purpose of training and testing. Another important constraint is the unavailability of compatible ROS packages, which hindered the realization of a fully portable system.

Future endeavors for this project will involve expanding the dataset further, incorporating adaptive learning techniques to enhance the robustness of the CNN model, and ultimately achieving the development of a fully portable system.

8.5 Summary

This chapter describes a proof of concept for a portable object classification system suitable for on-road deployment. The system successfully classified objects into eight different classes with an average accuracy of 85% across all classes. The utilization of Raspberry Pi (RasPi) ensures the portability and cost-effectiveness of the system. With further training on extensive and diverse datasets, the system can be enhanced for deployment in broader areas, expanding its applicability.

Chapter 9

Conclusion and Future Work

This work presents the design techniques and architectural solutions for VCO, frequency divider and frequency synthesizer blocks that form an essential sub-system in portable sensing applications. Proof-of-concept implementations have also been presented for a portable object classification system for on-road deployment and an automated system for classifying respiratory sounds.

A design technique has been detailed for LC VCO with low gain and reduced gain variation, specifically for highly sensitive quantum sensing applications. A new Figure of Merit (FoM) has also been defined to capture the effect of variations in the VCO gain on its performance. We have also presented a 2.87 GHz microwave signal generator (MWG) for CMOS quantum sensing applications based on NV-ODMR. The proposed MWG offered on-chip programmable sweep capability, eliminating the need for an external source and reducing power consumption and system complexity. The proposed automated system for classifying respiratory sounds was designed to help recognize anomalies that may be signs of respiratory diseases. This system can assist in timely diagnosis and improve the effectiveness of respiratory disease detection. Focus has also been put on the design and analysis of a transformer tank-based VCO and multi-modulus frequency divider operating in the mmWave frequency range for 77 GHz FMCW chirp synthesizers. The design aimed to achieve low phase noise performance by utilizing a transformer with a turn ratio of less than 1. The proof of concept for a portable object classification system for on-road deployment has also been detailed. The system achieved an average accuracy of 95% across eight different classes of objects utilizing Raspberry Pi (RasPi) to ensure portability and cost-effectiveness.

The scope of improvement for the presented work includes:

1. Design and development of NV-ODMR system with MWG offering on-chip programmable sweep capability for accurately measuring magnetic field strengths less than 1 μT.

2. Design and development of FMCW chirp synthesizer operating in mmWave frequency range of 77-81 GHz.

3. Design and development of a portable object classification system using FMCW radar arrays for improved classification accuracy.

4. Propose novel CNN architectures specifically for radar point clouds.

5. Propose ensemble modelling strategies for improved accuracy of respiratory sound classification using characteristics such as MFCC in addition to Mel spectrograms.

Related Publications

Conference Papers (Published/Accepted)

[1] **A. S. Edakkadan**, K. Desai and A. Srivastava, "A 2.75-2.94 GHz Voltage Controlled Oscillator with Low Gain Variation for Quantum Sensing Applications," 2022 35th International Conference on VLSI Design and 2022 21st International Conference on Embedded Systems (VLSID), Bangalore, India, 2022, pp. 186-191, doi: 10.1109/VLSID2022.2022.00045.

[2] **A. S. Edakkadan**, K. Saha, M. S. Baghini and A. Srivastava, "Design of 2.87 GHz Frequency Synthesizer with Programmable Sweep for Diamond Color Defect based CMOS Quantum Sensing Applications," 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX, USA, 2022, pp. 3092-3096, doi: 10.1109/ISCAS48785.2022.9937824.

[5] **A. S. Edakkadan** and A. Srivastava, "Deep Learning Based Portable Respiratory Sound Classification System," 2023 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Hyderabad, India, 2023.

[3] H. Kambham, S. S. Chatterjee, **A. S. Edakkadan** and A. Srivastava, "Analysis and Design of Low Phase Noise 20 GHz VCO for Frequency Modulated Continuous Wave Chirp Synthesizers in mmWave Radars," 2023 36th International Conference on VLSI Design and 2023 22nd International Conference on Embedded Systems (VLSID), Hyderabad, India, 2023, pp. 395-400, doi: 10.1109/VLSID57277.2023.00084.

[4] S. Mantha, **A. S. Edakkadan**, A. Sahni and A. Srivastava, "An mmWave Frequency Range Multi-Modulus Programmable Divider for FMCW Radar Applications," 2023 36th International Conference on VLSI Design and 2023 22nd International Conference on Embedded Systems (VLSID), Hyderabad, India, 2023, pp. 407-412, doi: 10.1109/VLSID57277.2023.00086.

Journal Papers (Under Review)

[6] S. S. Chatterjee, P. Mahajan, **A. S. Edakkadan**, J. Benny, A. Sahni, R. K. Sarvadevabhatla and A. Srivastava, "SVM based Object Classification System using FMCW Radar for Road Safety Applications." (Submitted to IEEE Sensors Journal)

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