Design and Implementation of Trim-free Voltage and Current References for Energy-Efficient IoT Applications

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Chetan Mittal
2021702019
chetan.mittal@research.iiit.ac.in

International Institute of Information Technology
Hyderabad - 500 032, INDIA
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International Institute of Information Technology
Hyderabad, India

CERTIFICATE

It is certified that the work contained in this thesis, titled ***"Design and Implementation of Trim-free Voltage and Current References for Energy-Efficient IoT Applications"*** by Chetan Mittal, has been carried out under my supervision and is not submitted elsewhere for a degree.

_____ _____

Date Advisor: Dr. Zia Abbas

To the Past, Present and Future

Acknowledgments

I begin this acknowledgment by expressing my sincere thanks to Professor Dr. Zia Abbas. He has been more than just an advisor to me during my time at IIIT-Hyderabad; he has been a mentor and a close guide. His unwavering support and guidance have been crucial to my academic journey. Dr. Abbas's unique approach to encouraging innovation and his focus on teamwork have been a great source of motivation for me, pushing me to strive for excellence in research. Additionally, he has taught me the importance of being passionate about my work and showing kindness to others, which have not only shaped my academic growth but also my personal development.

My initial interest in Analog Circuit design was sparked by online resources like NPTEL lectures, which I found to be highly intuitive and easy to understand. These lectures were delivered by renowned experts in the field, including Dr. Shanthi Pavan from IIT-Madras, Dr. Nagendra Krishnapura from IIT-Madras, Dr. Behzad Razavi from UCLA, Dr. Ali Hajimiri from CalTech. These resources not only helped me grasp the fundamentals of Analog Circuit design but also inspired me to delve deeper into the field. The clarity and depth of the lectures provided me with a solid foundation, motivating me to pursue further study and research in this area. I thank Intel semiconductors for introducing me to the real fabrication issues from industry perspective. I would like to express my gratitude to Micron Technology for providing me with an opportunity to gain a better understanding of circuit design.

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Abstract

The Internet of Things (IoT) has witnessed exponential growth, enabling a plethora of smart applications ranging from wearable devices to smart cities. However, the widespread adoption of IoT devices hinges on their ability to operate with minimal power consumption. However, one of the critical challenges in IoT design is the need for ultra-low power consumption to enable long battery life and energy harvesting. Moreover, systems powered by energy harvesting sources need to operate effectively with lower supply voltages. Similarly, systems relying on miniaturized batteries must be capable of functioning over a broad range of supply voltages, eliminating the necessity for voltage regulators.

Low power, high precision and low supply voltages are the primary requirement of an IoT based design. Voltage and current references are the basic blocks used in IoT based system. This thesis focuses on the designing of Voltage and current references circuit with low power consumption, low supply voltage and high precesion without using any external calibration circuit.

Firstly. the thesis introduces a All-in-one low-power, voltage and current reference design into a single block without using any external calibration. The design works with a supply of 1V with a power consumption of 37nW shows temeprature invariancy through a wide tempertaure range of -40 to 100°C. This design specification shows the best results among the previous state-of-art works. Furthermore, in response to the growing demand of low power high precsion circuits we designed an ultra-low power current reference circuit which is independent of temperature, voltage and process without using any extra trimming circuitry. The design works with a supply of 0.8V and generates a refrence current of 543pA by consuming a power of 3.3nW. Lastly, we come up with a novel design of voltage reference. The proposed work is designed in 180nm with a supply voltage of 0.6V with an excellent Line sensitivity of 0.0012/V without using an external calibration circuit.

In summary, this thesis encompases the circuit designing of low power, low voltgae and high accuracy voltage and current references without using resistors, amplifiers and external calibration circuit used in IoT applications.

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Chapter 1

Introduction

In the past seventy years, computing systems have undergone a remarkable transformation, transitioning from isolated interactions with computers to their ubiquitous integration into our daily lives. Initially, the collection of data on the internet relied heavily on human input and intervention. However, as the volume of data grew exponentially, there arose a need for a new paradigm where systems could autonomously interact with their environment. This marked the advent of the Internet of Things (IoT), a technological era characterized by the interconnection of everyday objects to networks. This connectivity revolutionizes how we interact with the world around us, creating new possibilities for innovative services and opportunities.

As the Internet of Things (IoT) grows, there is a greater need for devices that can operate efficiently. This demand for energy-efficient devices is driving the expansion of the IoT market, which has the potential to become the largest electronics market globally. With almost everything now connectable to the internet, the IoT market continues to expand rapidly. The graph below shows a steady increase in global active IoT connections, indicating a growing market size in billions of dollars over the years.

IoT applications rely heavily on analog circuit design to interface with the physical world. Analog circuits are crucial for tasks such as sensor signal conditioning, analog-to-digital conversion, power management, and wireless communication. These circuits play a vital role in ensuring that IoT devices can accurately sense, process, and communicate data in real-world environments. In general, these applications typically exhibit low-speed operation, low accuracy requirements, and low activity rates. However, they can greatly benefit from enhanced energy efficiency, which enables increased portability, reduced complexity, and cost savings. Researchers around the globe are confronted with the complex task of modifying different Internet of Things (IoT) subsystems, such as sensing networks, biasing networks, and radio frequency transmission circuitry, to accommodate the evolving requirements of IoT devices. To tackle these challenges, this thesis presents a comprehensive set of circuit-level techniques and system-level optimizations tailored to meet the diverse demands of emerging IoT applications.

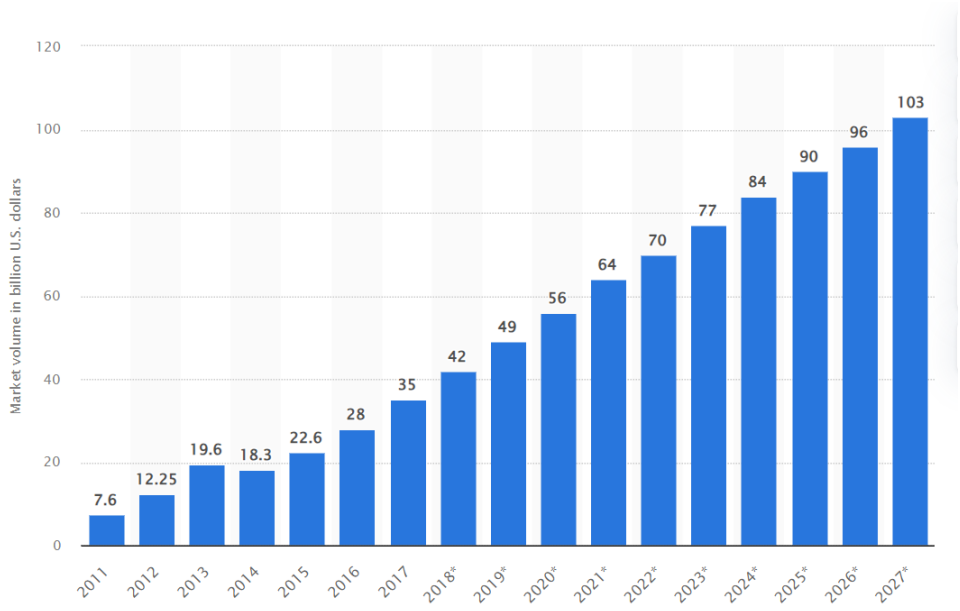

Figure 1.1: Market size revenue (in billion dollar) forecast worldwide from 2011 to 2027 [1]

1.1 Motivation behind low-power Analog circuits for IoT applications

The motivation behind low-power analog circuits for IoT applications stems from the unique requirements of IoT devices. IoT devices are often deployed in remote or hard-to-reach locations and are powered by batteries or energy harvesters. As such, they must operate efficiently to prolong battery life or operate in energy-constrained environments. Low-power analog circuits are essential in IoT devices for several reasons:

- **Energy Efficiency**: Low-power analog circuits help minimize energy consumption, extending the operational life of battery-powered IoT devices and reducing the need for frequent battery replacements. Energy-efficient circuits are often more reliable than their high-power counterparts. They generate less heat, which can reduce the risk of component failure and ensure consistent performance over time.

- **Cost-Effectiveness**: By reducing power consumption, low-power analog circuits can lead to cost savings, as smaller batteries or energy harvesters can be used.

- **Scalability**: Low power Analog circuits are crucial for the scalability of IoT deployments. As the number of connected devices grows, the demand for energy-efficient solutions becomes increasingly important to manage power consumption effectively.

This thesis aims to delve into the intricate design considerations, innovative methodologies, and comprehensive system-level optimizations essential for Low Power Analog Circuit Design in IoT and Biomedi-

cal Applications. It investigates the unique challenges posed by these fields, ranging from the imperative of extended battery life and effective energy harvesting in IoT devices to the stringent power constraints and biocompatibility prerequisites in biomedical scenarios.

By thoroughly examining these design principles, the significance of this thesis emerges. It addresses the urgent needs of our progressively interconnected world and the constantly evolving realm of healthcare technology, where efficient, low-power analog circuits have the potential to not only augment device functionality but also enhance the quality of life for individuals. This endeavor aims to unlock the full potential of IoT and Biomedical Applications, offering solutions that are not only technologically advanced but also environmentally sustainable and centered on human well-being.

1.2 Thesis Organisation

In this thesis, we introduced ultra-low power analog circuits designed for IoT and biomedical applications, focusing on the importance of voltage and current references. These references are critical in IoT systems, requiring them to adjust their power consumption to meet new demands. In systems with analog-to-digital converters (ADCs), voltage and current references play a crucial role in calibrating the ADCs for accurate digitization of analog signals. They are also essential in circuits requiring temperature compensation, ensuring stable performance across varying temperatures. Additionally, voltage and current references are used in biasing networks to set component operating points, ensuring proper circuit functionality. It is essential for these references to operate accurately over a wide temperature range without the need for external trimming circuits.

Chapter 2 of this thesis presents the foundational knowledge required for designing voltage and current references tailored for ultra-low-power IoT and biomedical applications. The chapter explores diverse techniques for temperature compensation, improving supply sensitivity, and ensuring process invariance for these references. Furthermore, it examines the essential parameters and specifications relevant to analog circuits, such as voltage and current references, highlighting their significance in circuit design.

Chapter 3 introduces a novel All-in-One low-power, Trim-free Voltage/Current Reference without using Resistors and Amplifiers designed specifically for IoT and biomedical applications. The voltage reference is created through the combination of Complementary to Absolute Temperature (CTAT) and Proportional to Absolute Temperature (PTAT) voltages, while the current reference utilizes a MOSFET in its linear region to function as a resistor, minimizing power consumption without increasing the device's form factor. Implemented in a 90nm CMOS process, the proposed voltage/current reference achieves an output voltage and current of 820mV and 3.23nA, respectively. Notably, the reference design does not require trimming, exhibiting a process variation of 1.34% (σ/μ) / 1.75% (σ/μ) and a temperature coefficient of 62ppm/°C / 332ppm/°C over a wide temperature range from -40oC to 100oC. The line sensitivity of the voltage/current reference stands at 0.296%/V / 0.414%/V across a broad

supply range of 1V to 3.5V. Occupying a minimal area of 0.0112mm^2, the total power consumption of the circuit design is measured at 37nW under typical conditions of 27°C and 1V supply.

Chapter 4 introduces a sub-1V, sub-nA current reference with the absence of large resistors, hence occupying a small area. A 593pA temperature-independent current reference is generated by incorporating a CTAT gate to source voltage and a PTAT drain to source voltage in an NMOS-based subthreshold-biased circuit. Without trimming, the proposed reference current has ± 0.75% variation across the process corners. The proposed circuit is implemented in a 90nm CMOS process having a temperature coefficient of 378ppm/oC over a temperature range of -40°C to 100°C and a line sensitivity of 0.198%/V in a range of supply voltage from 0.8V to 2.8V. A duty-cycle technique is applied to enable 1% duty-cycling of the CTAT generator, resulting in a reduction in power consumption of the overall circuit. The area occupied by the resistor-less circuit is 0.0286mm^2, while the total power consumption of the design with duty-cycling technique is 4nW at the typical corner of 27°C and 0.8V supply.

Chapter 5 presents a low-voltage, low-power PVT-invariant voltage reference with excellent line sensitivity for IoT and biomedical applications. By applying a bias current(I_{bias}) in NMOS-based composite pair and bias voltage(V_{bias}) at the body of NMOS to get the temperature-compensated voltage reference over a wide temperature range. The proposed design implemented in 180nm CMOS process gives an outputs of 141mW which is independent of process, voltage and temperature. Without trimming, the process variation of proposed design is 1.51%(σ/μ) and the temperature coefficient of proposed voltage reference is 23ppm/°C over a wide temperature range of -40°C to 100°C. For a supply voltage ranging from 0.6V - 2.1V the line sensitivity of the reference is 0.0012%/V. The simulated results shows that the proposed voltage reference could operate on a minimum supply of 0.6V and the power supply rejection ratio at 1-Hz is ... .The area occupied by the total circuit is 0.0085mm^2 , while the total power consumption of the design is 14.2nW at the typical corner of 27^{o}C and 0.6V supply.

Finally in Chapter 6, the conclusions drawn from the research done so far are presented. Additionally, potential areas for further improvement and future research directions are discussed.

Chapter 2

Literature Review

2.1 Introduction

The field of microelectronics is witnessing exciting developments in ultra-low power LSIs, offering significant promise for various applications demanding power efficiency. These LSIs hold particular relevance for portable mobile devices, implantable medical devices, and smart sensor networks [2]. Given the anticipated deployment in environments with limited energy sources, such as microbatteries or energy scavenging devices, these devices must operate on ultra-low power levels, typically in the range of a few microwatts or less [3].

A critical milestone in advancing these LSIs is the development of voltage and current reference circuits capable of ultra-low current operation, often in the realm of several tens of nanoamperes or less, corresponding to sub-microwatt operation. To achieve such remarkable power efficiency, these circuits must operate in the subthreshold region, where the gate-source voltage of MOSFETs falls below the threshold voltage [4, 5].

2.2 Subthreshold region(Weak inversion region) of MOSFETs

The subthreshold region in MOSFET operation is a crucial domain for achieving ultra-low power consumption in integrated circuits. In this region, the gate-source voltage of the MOSFET is lower than the threshold voltage, resulting in a low drain-source current. This region is particularly important for applications where minimizing power consumption is paramount, such as in IoT devices, biomedical implants, and energy harvesting systems. By operating in the subthreshold region, MOSFETs can achieve high energy efficiency, making them ideal for applications requiring long battery life or operation on limited power sources. However, designing circuits to operate in the subthreshold region poses challenges, including increased sensitivity to process variations and temperature effects, requiring careful optimization and design techniques.

The subthreshold region of a MOSFET occurs when the gate-source voltage falls below the threshold voltage. In this regime, a small leakage current, known as subthreshold current, flows through the

MOSFET. This current exhibits an increasing exponential relationship with the gate-source voltage and typically operates at the nanoampere level. The subthreshold drain current (I_{DS}) in a MOSFET follows an exponential relationship with both the gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}) [6]. Specifically, it is given by:

$$I_{DS} = K_n \frac{W}{L} (\eta - 1) V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \left(1 - \exp\frac{-V_{DS}}{V_T}\right) \tag{2.1}$$

where $K_n = \mu_n C_{ox}$, V_{TH} represents the threshold voltage of the transistor, V_T is the thermal voltage and η is the sub-threshold slope constant. Fig. 2.1 shows the Ids vs vgs characterstics of a NMOS operating in subthreshold region at different temperature range.

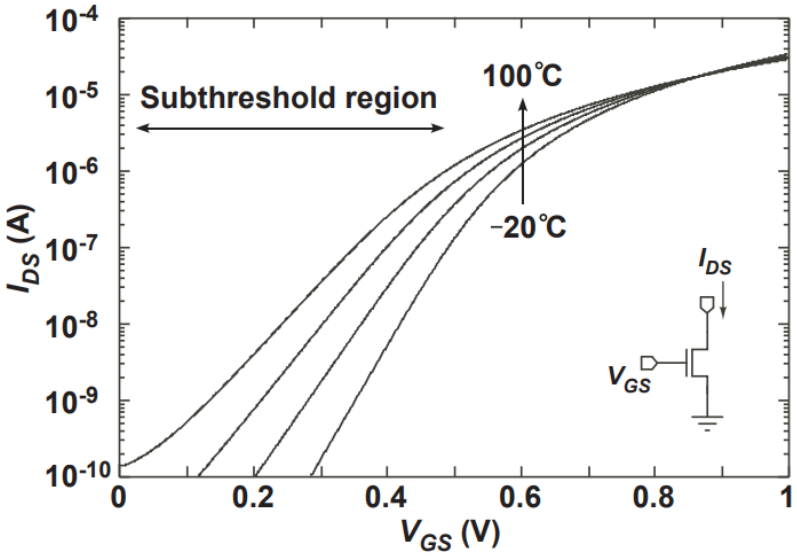

Figure 2.1: MOSFET operates in subthreshold region

When the vds of mosfet operates in subthreshold region is greater than 4 times of thermal voltage i.e the current obtained through the mosfet is independent of Vds and is given by :

$$I_{ref} = K_n \frac{W}{L} (\eta - 1) V_T \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \tag{2.2}$$

2.3 Process, voltage and temperature independent Analog circuits

Process, voltage, and temperature (PVT) independent analog circuits are essential components in modern integrated circuit design, particularly for applications requiring high reliability and performance across varying operating conditions. These circuits are designed to maintain consistent functionality and performance regardless of manufacturing process variations, supply voltage fluctuations, or temperature changes. Achieving PVT independence often involves sophisticated design techniques, such as using compensation circuits to counteract process variations, designing circuits with wide supply voltage

ranges, and employing temperature compensation methods. PVT independent analog circuits are particularly valuable in applications where precise and stable analog signal processing is critical, such as in sensor interfaces, data converters, and communication systems.

2.3.1 Temperature variation

Temperature-invariant analog circuits are crucial components in electronic systems, ensuring stable performance across a wide range of operating temperatures. These circuits are designed to maintain consistent functionality and performance regardless of temperature fluctuations. The parameter used for temperature variation is the temperture coefficent. In analog circuits, the temperature coefficient (TC) refers to the rate of change of a circuit parameter (such as voltage, current, or resistance) with respect to temperature. It is expressed in units of the parameter per degree Celsius (e.g., ppm/°C for voltage or current). In the realm of analog circuits, the behavior of certain parameters such as voltage or current with respect to temperature is of particular interest. When the parameter increases proportionally with an increase in temperature, it is referred to as Proportional to Absolute Temperature (PTAT). Conversely, if the parameter decreases as temperature rises, it is termed Complementary to Absolute Temperature (CTAT). Finally, when the parameter remains constant regardless of temperature variations, it is known as Constant with respect to Temperature (CWT). Understanding these temperature-dependent behaviors is crucial in designing circuits. Fig. 2.2 shows the parameter nature with predictable and stable performance across varying thermal conditions.

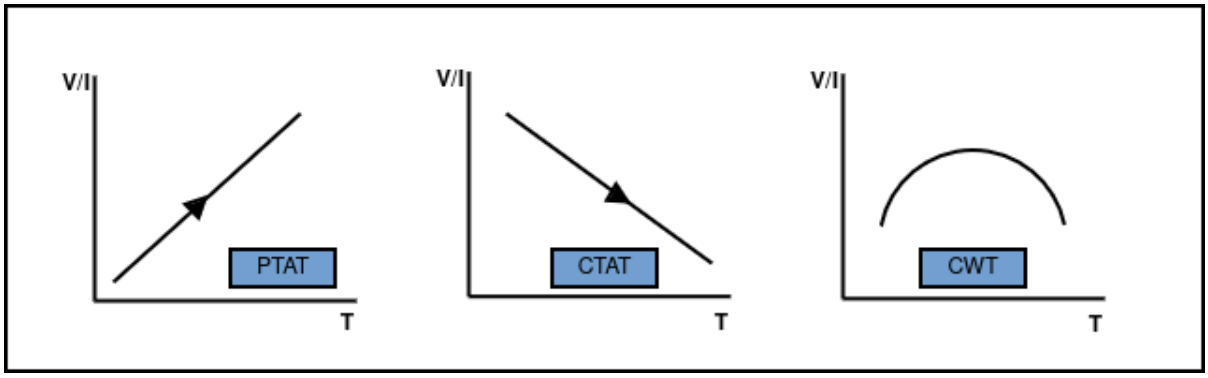

Figure 2.2: Variations of voltage/current across temperatures

2.3.2 Voltage variation

Voltage-invariant analog circuits are fundamental components in electronic systems, designed to maintain consistent functionality despite fluctuations in the supply voltage. These circuits are crucial for ensuring stable performance across a wide range of operating conditions, as variations in the supply voltage can significantly impact the behavior of analog circuits. we expressed the voltage variation in terms of line sensitivity. Line sensitivity, refers to the change in output voltage of a circuit in response

to variations in the supply voltage. It is a critical parameter in analog circuits, especially in applications where the stability of the output voltage is crucial. Line sensitivity is typically expressed in percentage change in output voltage per volt change in supply voltage (%/V). A lower line sensitivity indicates that the circuit's output voltage is less affected by changes in the supply voltage, which is desirable for maintaining stable circuit operation. In this thesis we applied line sensitivity improving techniques to improve the varaition of output quantities i.e voltgae or current with respect to supply voltage.

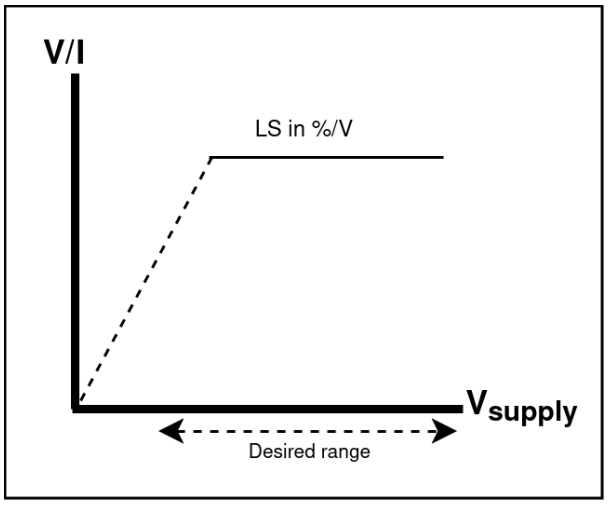

Figure 2.3: Variation of Voltage/Current w.r.t supply voltage

2.3.3 Process Variation

Process variation is a significant challenge in analog circuit design, stemming from manufacturing inconsistencies that lead to differences in the electrical characteristics of individual components. These variations can result in deviations from the intended circuit behavior, affecting performance metrics such as gain, bandwidth, and power consumption. To mitigate the impact of process variation, designers employ various techniques, including layout strategies, statistical design methodologies, and calibration circuits. Additionally, advances in semiconductor manufacturing processes, such as improved process control and modeling, have helped reduce process variation. Despite these efforts, managing process variation remains a critical consideration in analog circuit design, particularly in applications requiring high precision and reliability.

Process variations can be classified into two categories: i.e., within-die (WID) (intra-die) variation and die-to-die (D2D) (inter-die) variation .The WID variation is caused by mismatches between transistor parameters within a chip and affects the relative accuracy of the parameters. In contrast, the D2D variation affects the absolute accuracy of transistor parameters between chips [7, 8, 9, 10]. Process variations can also affect the threshold voltage of a MOSFET. Variations in doping concentrations, oxide thickness, and other fabrication parameters can lead to variations in the threshold voltage across

different transistors on the same chip. These variations can impact circuit performance and may require additional design considerations to ensure reliable operation.

2.3.4 Fundamental Analog blocks : Voltage and current reference

Voltage and current reference circuits serve as foundational elements in microelectronics, playing a crucial role in ensuring the reliable performance of analog, digital, and mixed-signal circuit systems. These circuits are primarily characterized by their ability to maintain stable bias voltages and currents, which are essential for the proper functioning of various components like operational amplifiers, comparators, AD/DA converters, oscillators, and PLLs. To achieve this stability, bandgap reference circuits utilizing CMOS-based vertical bipolar transistors have traditionally been the go-to choice in CMOS LSIs, providing a constant and precise reference voltage and current.

2.3.4.1 Generation of Voltage and current reference

Generating a voltage/current reference typically entails either combining two quantities with opposite temperature dependencies or subtracting two quantities with similar temperature dependencies resulting into a voltage and current reference with no variation of current and voltage with temperature.

Case 1: Combination of Voltage/Current with opposite temperature dependencies

This method approach is to combine two quantities that have opposite temperature dependencies. This means that as one quantity increases with temperature, the other decreases, and vice versa. By combining these two quantities, the overall effect cancels out the temperature variations, resulting in a stable output. For example, in a voltage reference circuit, one can combine a voltage source that increases with temperature (PTAT) with a voltage source that decreases with temperature (CTAT). By appropriately choosing and combining these sources, the temperature-dependent variations can cancel each other out, resulting in a stable output voltage over a wide temperature range. In a current reference circuit, a similar principle applies. By combining two current sources with opposite temperature coefficients, the variations in one source can offset the variations in the other, leading to a stable output current despite changes in temperature. Figure explain the generation of voltage/current reference by combing two opposite temperature dependecies i.e PTAT and CTAT with a slope of a and b respectivily to get V_{ref}

$$V_{ref}/I_{ref} = a * V_{PTAT1}/I_{PTAT1} + b * V_{CTAT2}/I_{CTAT2}$$

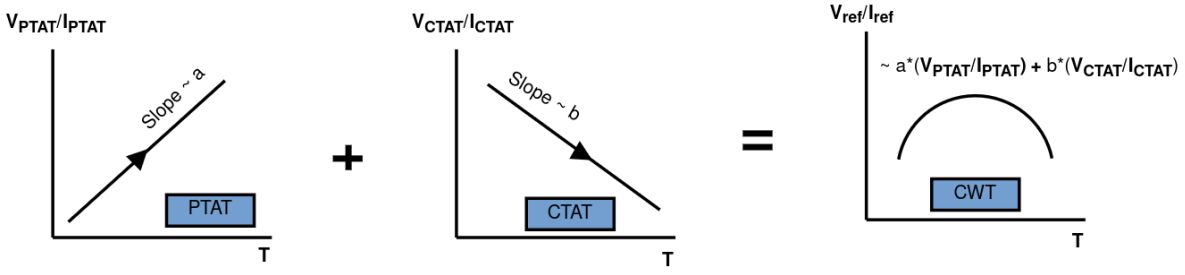

Figure 2.4: Combination of PTAT and CTAT

Case 2: Combination of Voltage/Current with same temperature dependencies

The second approach to generating a voltage or current reference involves subtracting two quantities with similar temperature dependencies. This method relies on the fact that some components or materials exhibit temperature-dependent characteristics that change in a predictable manner with temperature. For example, in a voltage reference circuit, one can use two voltage sources with similar positive temperature coefficients (PTAT) with different slope or with similar negative temperature coefficent (CTAT) with different slope. By subtracting one voltage source from the other, the temperature-dependent variations can be made to cancel out, resulting in a stable output voltage over a wide temperature range. Similarly, in a current reference circuit, two current sources with similar temperature coefficients can be subtracted from each other to achieve a stable output current despite changes in temperature. The Figure 2.5 and 2.6 shows the explaination as discussed above i.e

$$V_{ref}/I_{ref} = \left\{ \begin{array}{l} a * V_{PTAT1}/I_{PTAT1} - b * V_{PTAT2}/I_{PTAT2} \\ a * V_{CTAT1}/I_{CTAT1} - b * V_{CTAT2}/I_{CTAT2} \end{array} \right\}$$

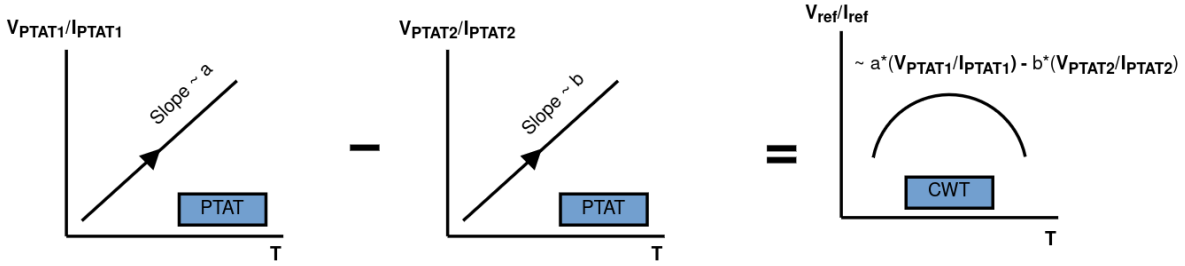

Figure 2.5: Combination of two PTAT sources with different slope

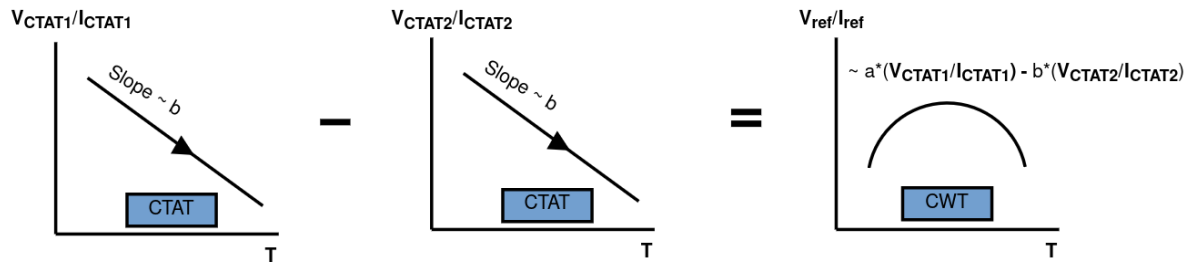

Figure 2.6: Combination of two CTAT sources with different slope

2.3.5 Methods of generating PTAT and CTAT voltage/current

Generating Proportional to Absolute Temperature (PTAT) and Complementary to Absolute Temperature (CTAT) voltage and current references is crucial in analog circuit design, especially for applications sensitive to temperature variations. A commonly used method to generate a PTAT voltage involves utilizing the base-emitter voltage of a bipolar junction transistor (BJT), which exhibits a positive temperature coefficient. By biasing the BJT appropriately, its base-emitter voltage can serve as a PTAT voltage reference. Conversely, for CTAT voltage generation, components like diodes or resistors with negative temperature coefficients can be combined with PTAT sources. Similar principles apply to current reference generation, where the temperature-dependent voltage across a resistor or diode is leveraged to create a PTAT or CTAT current reference. These methods necessitate meticulous component selection and precise circuit design to achieve the desired temperature characteristics for voltage and current references. Here are the some PTAT and CTAT current/voltage circuits used in our thesis.

Circuit 1: CTAT voltage using diode connected MOSFET

CTAT (Complementary to Absolute Temperature) voltage generation using a diode-connected MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is a technique commonly employed in analog circuit design [11]. In this method, the MOSFET is biased in the Subthreshold-saturation region, where the drain and gate are connected together, effectively forming a diode-like structure. The voltage across this diode-connected MOSFET exhibits a negative temperature coefficient, meaning that it decreases with increasing temperature.

The threshold voltage (V_{th}) exhibits a complementary to absolute temperature (CTAT) behavior, expressed as $V_{th0} - k_1 T$, where V_{th0} is the nominal threshold voltage, and k_1 represents the slope of the threshold voltage. The term μ_n is directly proportional to $T^{-3/2}$ [12, 13], causing the term $\eta V_T \ln\left(\frac{I}{\mu_n C_{ox}(\eta-1)V_T^2}\right)$ to be proportional to $\ln(T^{-1/2})$, assuming I remains constant with temperature. Despite being a weak function of temperature, the predominant CTAT nature of V_{th} extends to V_{GS}.

$$V_{GS} = V_{th} + \eta V_T \ln\left(\frac{I}{\mu_n C_{ox}(\eta-1)V_T^2}\right) \tag{2.3}$$

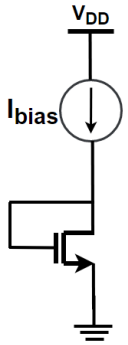

Figure 2.7: CTAT generator using diode connected MOSFET

Circuit 2: CTAT/PTAT voltage generation using single block

As shown in Fig. 2.8, the CTAT generator is applied as an input to the PTAT/CTAT generator and biased with the reference current (I_{ref}). Since the MOSFET operates in the sub-threshold region, V_{GG} can be expressed as follows:

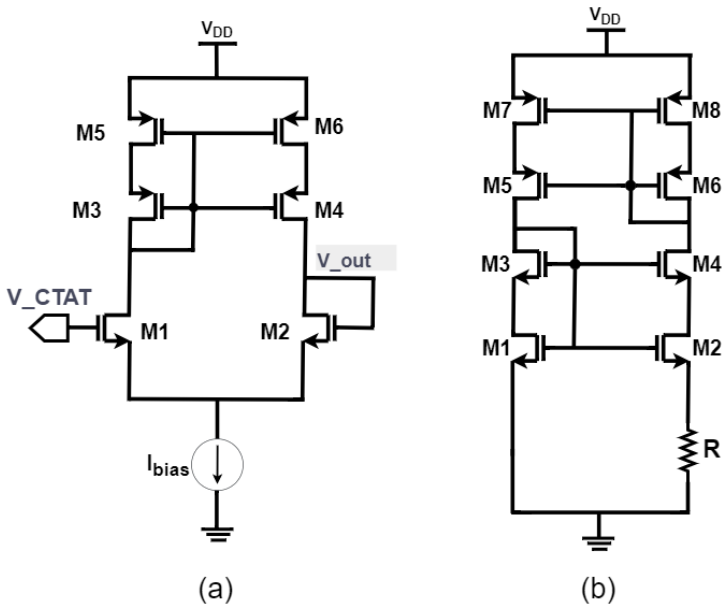

Figure 2.8: (a) CTAT voltage generator using differential pair mosfet (b) PTAT current generator using Beta-multiplier

$$
\begin{aligned}
V_{GG} &= V_{ref} - V_{CTAT} = V_{GS,M18} - V_{GS,M17} \\
&= V_{TH} + \eta V_T \ln\left(\frac{I_{M18}}{K_{M18} I_0}\right) - V_{\mathrm{TH}} - \eta V_T \ln\left(\frac{I_{M17}}{K_{M17} I_0}\right) \\
&= \eta V_T \ln\left(\frac{K_{M14} K_{M17}}{K_{M13} K_{M18}}\right)
\end{aligned} \tag{2.4}
$$

Where, I_0= $\mu C_{OX}(\eta - 1)V_T^2$ is a process dependent parameter. K_{M17}, K_{M18}, K_{M13} and K_{M14} are the aspect ratios of the NMOS differential pair and the PMOS current mirrors respectively. If $K_{M14}K_{M17} > K_{M13}K_{M14}$ the V_{GG} will PTAT in nature whereas, $K_{M14}K_{M17} < K_{M13}K_{M14}$ the voltage V_{GG} is CTAT in nature.

Circuit 3: PTAT current generation using beta multiplier circuit

Proportional to Absolute Temperature (PTAT) current generation using a beta multiplier circuit with Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) is a technique commonly employed in analog circuit design for temperature-independent current generation. The circuit utilizes the temperature-dependent threshold voltage of MOSFETs to create a current that varies proportionally with absolute temperature[14]. The beta multiplier circuit with MOSFETs typically consists of two MOSFETs, one acting as a diode-connected device and the other as a current mirror. By appropriately biasing the MOSFETs and adjusting the resistor values, the circuit can produce a PTAT current that compensates for temperature variations, making it suitable for applications requiring stable and accurate current references over a wide temperature range. The figures shows the operation of PTAT current using beta multiplier.

Chapter 3

A 37nW, All-in-One Trim-free Voltage/Current Reference without using Resistors and Amplifiers

3.1 Introduction

In recent years, significant progress has been made in developing low-power designs that are essential for battery-powered devices like wearables and IoT devices, where power consumption is a critical factor. Voltage/current references being essential components of any IoT system should also scale their power to satisfy the new requirements. Moreover, it is highly desirable for these references to operate over a wide temperature range with good accuracy and line sensitivity, without incorporating external trimming circuits. Trim-free designs eliminate the need for external calibration, reduce manufacturing costs and improve the circuit's reliability. Also, it is beneficial to have both the reference circuitry (voltage and current) to be integrated into a single block.

The voltage reference is a crucial component in the construction of analog, digital, and mixed-signal circuit systems. For operational amplifiers, comparators, and AD/DA converters to work properly, a constant reference voltage is needed. Voltage references are conventionally realized using BJTs and are called bandgap references (BGR) [15, 16]. Although the generated voltage in BGRs is highly resilient to process, supply, and temperature (PVT) variations, they consume power in the µW range and require a high supply voltage. Recently, CMOS subthreshold voltage references have received much attention since they operate at low supply voltages and consume very low power [17, 18, 19, 20]. [17] proposes a sub-µW voltage reference using MOSFETs and resistors. However, high resistance values used for lowering the power consumption have a direct tradeoff with the silicon area. [18] presents a resistor-less voltage reference with nW power consumption, but external trimming circuitry is required to correct the process variation of the design.

[19] proposes a CMOS-based voltage reference having power consumption in nW without using resistors and trimming circuits, but the process variation (σ/μ) of the design is 7%. To get further power reduction [20] proposes a pW voltage reference. However, it reports no functionality at negative temperatures. This constraint is mainly due to the exponential dependency of subthreshold leakage

on temperature. Also, they use native oxide devices (NVT MOSFETs), which are not provided by many foundries [21]. The conventional approach for generating current references involves variants of the beta multiplier, utilizing the V/R principle with opamps to effectively compensate the temperature coefficients of both resistance and voltage [22, 23].

However, resistance-based designs require an inconsiderably higher area to scale the power consumption of the pW and nW regime. To mitigate this issue, [24] replaces the resistor in the beta-multiplier with a MOSFET in deep triode to achieve power consumption in nW but at the cost of high process variation and large voltage supply (Min. supply $= 1.3V$). [25] proposes a current reference with a lower supply and nW power consumption. However, the process variation (σ/μ) of the design is $>10\%$. [26] improves the process variation of the current reference with a process tracking circuit but the power consumption, line sensitivity and temperature range make it unsuitable for low-power IoT applications. Design [27] proposes a trim-free nW current reference with a low process variation of 8.8% (6σ). However, the architecture works from a minimum supply of 1.5V. [28, 29] proposes pico-watt current references using tunneling currents, although these references require lower area, the susceptibility of tunneling currents to tox variations [30] ($>600\%$ across process corners) necessitates extensive trimming and increases the cost. References [31, 32, 33] explain voltage and current reference in a single block. [31] proposes nW voltage/current reference using resistors and amplifiers whereas, using amplifiers incurs additional design complexity like offset, power consumption, etc. [32] does not use an amplifier but requires a trimming circuit to improve process variation. [33] consumes power in pW but uses native oxide devices and trimming circuits.

This thesis presents a 37nW, trim-free voltage/current reference with a wide temperature range of -40^{o}C to 100^{o}C without using resistors, amplifiers and native oxide devices. The rest of the thesis is structured as follows: Section 3.2 describes the proposed voltage/current reference. Section 3.3 presents the simulated results and conclusions are drawn in Section 3.4.

3.2 Proposed Voltage/Current reference

The architecture of the proposed circuit is shown in Fig. 3.1. All the MOSFETs except M0 are in the subthreshold saturation region. The MOS resistor M0 is operated in a strong inversion, deep-triode region. The design consists of a triode resistance-based Beta-multiplier, a CTAT generator and a PTAT generator. A combination of triode resistance-based Beta-multiplier and CTAT generator results in a current reference [27] whereas, the PTAT and CTAT generator compensates for any variation of the generated voltage reference. Moreover, the generated reference current (I_{ref}) is used to bias the PTAT generator.

A capacitor (C_{eq}=2.17pF) implemented using a thick oxide device (M_{L0}) is connected at the output terminal to have a better power supply rejection ratio (PSRR) at higher frequencies. A start-up circuit [34] is added to avoid any degenerative conditions.

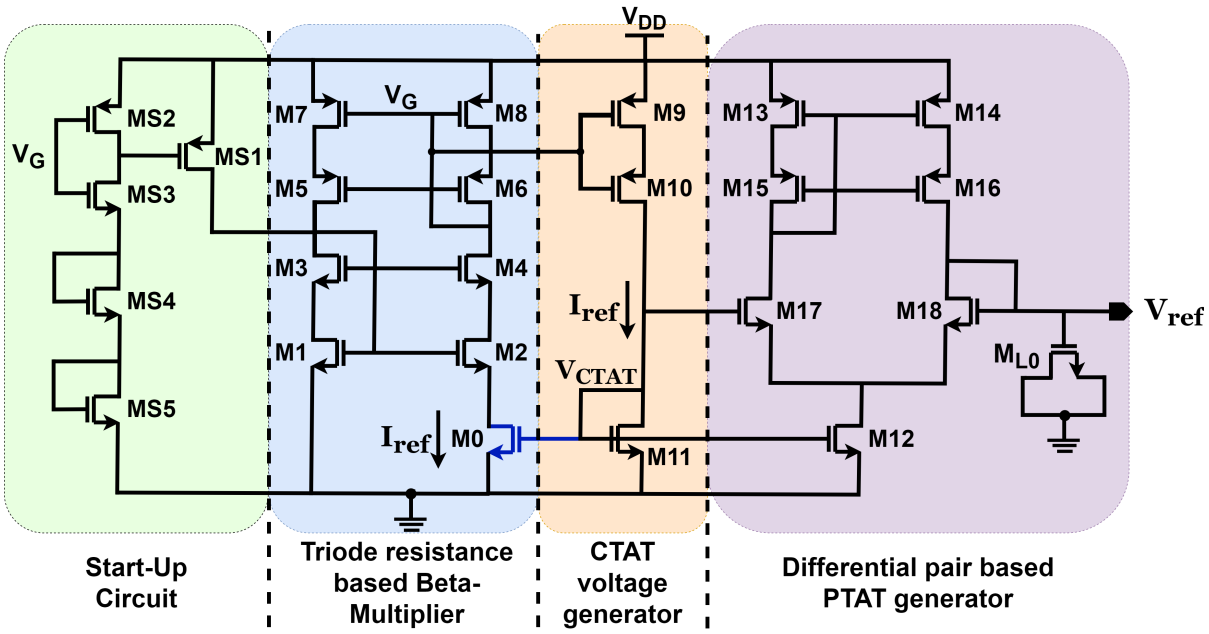

Figure 3.1: Proposed voltage/current reference

3.2.1 Temperature compensation of voltage/current reference

In the circuit, the current I_{ref} is generated by MOS resistor M0 with gate-source voltage $V_{GS,M0}$ and drain-source voltage $V_{DS,M0}$. When MOSFET M0 operates in strong inversion and deep triode region (V_{GS} - $V_{TH} > V_{DS}$) , the current through M0 is given by

$$I_{ref} = K_n \left(\frac{W}{L}\right)(V_{GS,M0} - V_{TH})V_{DS,M0} \tag{3.1}$$

Where, K_n= $\mu_n C_{ox}$, $\frac{W}{L}$ is the aspect ratio of the MOSFET M0 and $V_{DS,M0}$ = $V_{GS,M1}$ - $V_{GS,M2}$. To analyze the temperature behavior of reference current (I_{ref}) , differentiating (3.1) with respect to temperature (T) we get

$$\frac{\partial I_{ref}}{\partial T} = K_n \left(\frac{W}{L}\right) V_{DS} \left(\frac{\partial V_{GS}}{\partial T} - \frac{\partial V_{TH}}{\partial T}\right) + K_n \left(\frac{W}{L}\right) (V_{GS} - V_{TH}) \left(\frac{\partial V_{DS}}{\partial T}\right) + \frac{\partial K_n}{\partial T}(V_{GS} - V_{TH})V_{DS} \tag{3.2}$$

Therefore, the circuit is designed in such a way that the CTAT term K_n gets compensated by the PTAT terms $V_{DS,M0}$(=$\eta V_T \ln n$) and (V_{GS} - V_{TH}) as shown in Fig. 3.2(a) to obtain the temperature-compensated reference current (I_{ref}).

The PTAT generator along with a CTAT generator and a current reference is required to obtain a temperature-compensated voltage reference (V_{ref}).

The CTAT generator is applied as an input to the PTAT generator and biased with the reference current (I_{ref}). Since the MOSFET operates in the subthreshold region, V_{GG} can be expressed as follows:

$$\begin{aligned} V_{GG} &= V_{ref} - V_{CTAT} = V_{GS,M18} - V_{GS,M17} \\ &= V_{TH} + \eta V_T \ln\left(\frac{I_{M18}}{K_{M18} I_0}\right) - V_{\mathrm{TH}} - \eta V_T \ln\left(\frac{I_{M17}}{K_{M17} I_0}\right) \\ &= \eta V_T \ln\left(\frac{K_{M14} K_{M17}}{K_{M13} K_{M18}}\right) \end{aligned} \tag{3.3}$$

Where, I_0= $\mu C_{OX}(\eta - 1)V_T^2$ is a process dependent parameter. K_{M17}, K_{M18}, K_{M13} and K_{M14} are the aspect ratios of the NMOS differential pair and the PMOS current mirrors respectively.

$$\begin{aligned} V_{ref} &= V_{GG} + V_{CTAT} \\ &= \eta V_T \ln\left(\frac{K_{M14} K_{M17}}{K_{M13} K_{M18}}\right) + V_{th} + \eta V_T \ln\left(\frac{I_{ref}}{I_0}\right) \\ &= V_{th} + \eta V_T \ln\left(\frac{K_{M14} K_{M17} I_{ref}}{K_{M13} K_{M18} I_0}\right) \end{aligned} \tag{3.4}$$

Considering the temperature coefficient, V_{ref} can be given as:

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{th}}{\partial T} + \eta \frac{k}{q} \ln\left(\frac{K_{M14} K_{M17} I_{ref}}{K_{M13} K_{M18} I_0}\right) \tag{3.5}$$

A temperature-compensated voltage can be obtained by appropriately sizing the transistors M13, M14, M17 & M18.

3.2.2 Process variation of voltage/current reference

To study the effect of process variation on the voltage/current reference, one needs to check the process variant terms present in the equations of V_{ref} and I_{ref}. Eq.1 shows that threshold voltage is mainly responsible for process variation, where $V_{GS,M0}$ = V_{TH} + $\eta V_T \ln(I_{ref}/I_0)$. After substituting the value of $V_{GS,M0}$ in (3.1):

$$\begin{aligned} I_{ref} &= \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{TH} + \eta V_T \ln\left(\frac{I_{ref}}{I_0}\right) - V_{TH}) V_{DS,M0} \\ &= \mu_n C_{ox}\left(\frac{W}{L}\right) \eta V_T \ln\left(\frac{I_{ref}}{I_0}\right) V_{DS,M0} \end{aligned} \tag{3.6}$$

Here, V_{TH} cancellation takes place, which ultimately improves the process variation of the reference current. The value of V_{GS} - V_{TH} as shown in Fig. 3.2(a) at different process corners has minimal variation, demonstrating the reference current is less susceptible to process.

From 3.4, it can be observed that the expression of V_{ref} has three process variant terms V_{TH}, η, and I_{ref}. V_{TH} contributes the most and I_{ref} contributes the least amongst these. The input to the PTAT generator i.e. V_{CTAT} voltage is generated by passing I_{ref} into a diode-connected MOSFET. In any

process corner, if the V_{TH} increases, the corresponding current decreases, and as I_{ref} decreases the drain to source voltage V_{DS} (=$\eta V_T \ln(n)$) across the triode MOSFET M0 also decreases meaning that, η decreases for both PTAT terms. η is the subthreshold slope factor which depends on the gate oxide and depletion layer capacitances [35]. So, the process variation of V_{TH} is inversely related to the process variation of η and I_{ref}. The small process variation of I_{ref} along with the multiplication constant $(K_{M14}K_{M17}/K_{M13}K_{M18})$ that amplifies the process variation of η, mitigates the V_{TH} variation to a great extent, resulting in smaller process variation of the reference voltage (V_{ref}).

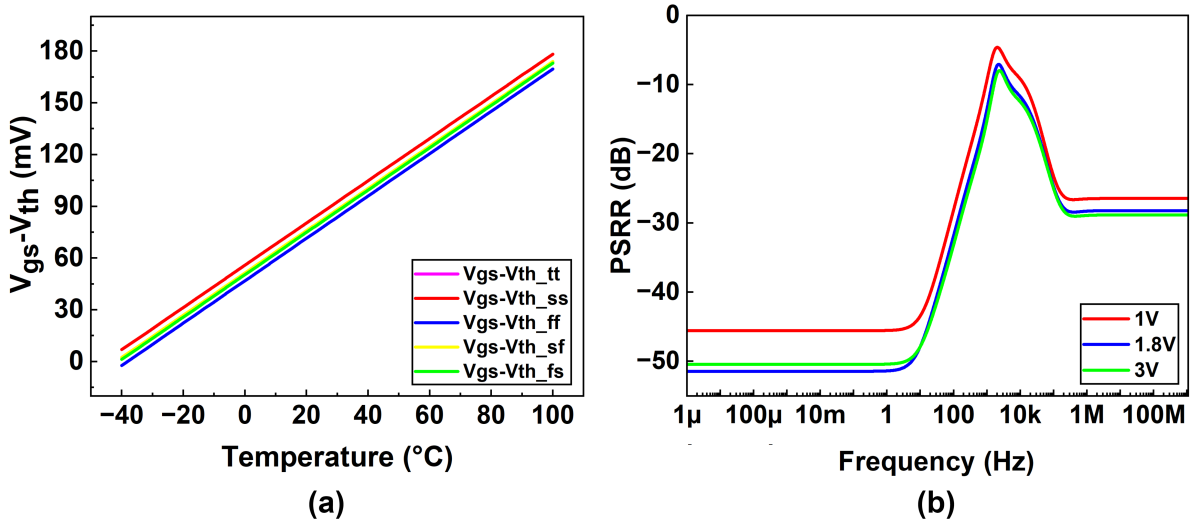

Figure 3.2: (a) V_{gs} - V_{th} vs temperature across corners (b) PSRR of V_{ref} w.r.t supply

3.3 Results and Discussion

The proposed voltage/current reference is designed and implemented in a 90nm CMOS process. Fig. 3.2(b) shows the PSRR at DC for the voltage reference at 1V, 1.8V, and 3V are -48dB, -52dB, and -51dB respectively. Fig. 3.3(a) shows temperature-compensated voltage and current reference plots; it depicts temperature coefficients (TC) of 62ppm/°C and 332pm/°C respectively for the temperature range of -40 to 100°C. The nominal value of the current and voltage reference is 3.23nA and 0.820V respectively. Fig. 3(b) shows the supply sensitivities of voltage and current references as 0.296%/V and 0.414%/V respectively for the supply range of 1 to 3.5V. As this architecture contains a self-biased loop, to avoid any degenerative conditions, a start-up circuit is added. Fig. 3.4 shows the 99% settling times for the voltage and current reference to be 11.73ms and 11.84ms, respectively. The statistical results for voltage and current reference are presented in Fig. 3.5 Using Monte Carlo simulation with 1000 samples the observed mean and standard deviation from Fig. 3.5(a) for the voltage reference are 820mV and 10.99mV respectively, which results in process variation (σ/μ) of 1.34%. Fig. 3.5(b) illustrates the Monte Carlo results for the current reference. The mean and standard deviation are 3.23nA

and 56.52pA respectively, resulting in process variation (σ/μ) of 1.75%. Fig. 3.6(a) shows the Monte Carlo results for V_{ref} over the temperature range of -40 to 100°C, from which 3σ variation of $\pm 4.02\%$ can be observed. Similarly, from Fig. 3.6(b) $\pm 3\sigma$ variation of $\pm 5.25\%$ can be observed for the I_{ref} w.r.t temperature. Fig. 3.7(a) shows the Monte Carlo results (1000 points) for the TC of V_{ref}. The observed mean and the standard deviation are 64.55ppm/°C and 2.564ppm/°C, respectively. Similarly, Fig. 3.7(b) shows the Monte Carlo results (1000 points) for the TC of I_{ref}, which comes out to have a mean of 337.17ppm/°C and a standard deviation of 15.16ppm/°C. These results prove that we can avoid trimming in this architecture, considering the achieved nominal values and accuracies for both voltage and current reference. The layout of the proposed voltage/current reference takes an area of $0.0112mm^2$ as illustrated in Fig. 3.8.

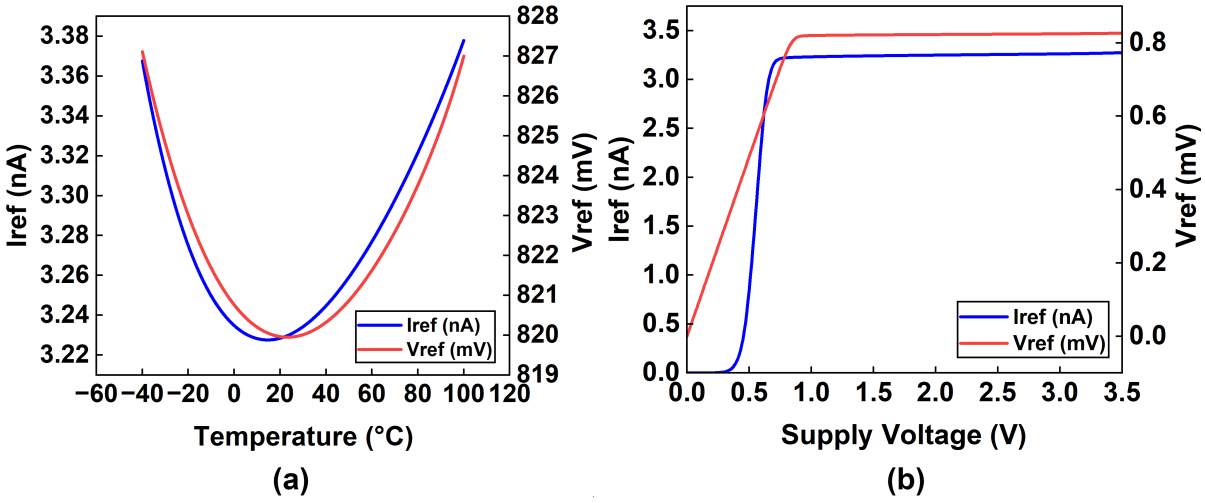

Figure 3.3: (a) V_{ref} & I_{ref} vs Temperature (b) Supply sensitivity of V_{ref} & I_{ref}

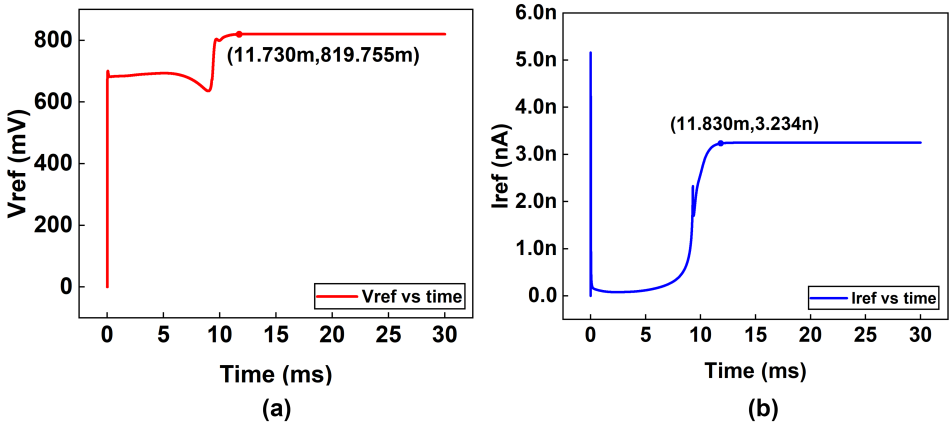

Figure 3.4: Start-up time of (a) V_{ref} and (b) I_{ref}

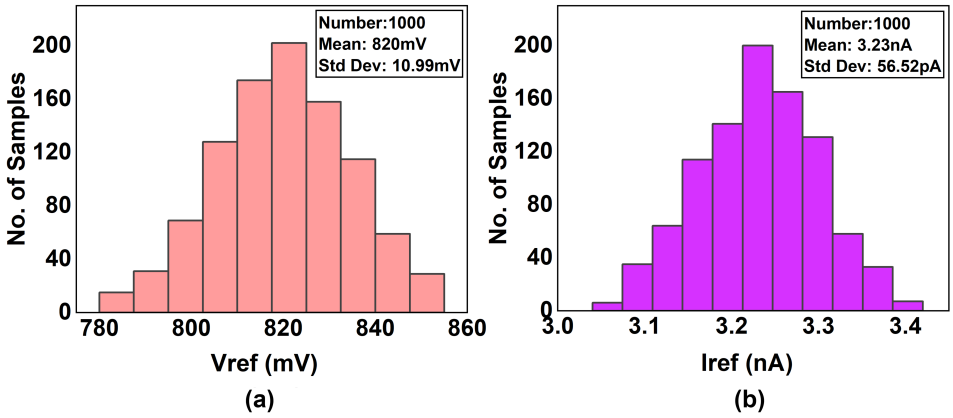

Figure 3.5: Monte Carlo results for (a) V_{ref} (b) I_{ref} value at 27°C

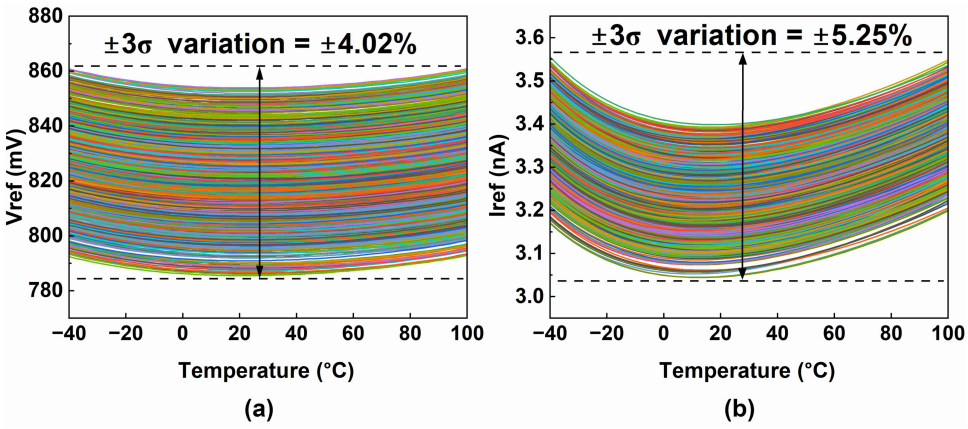

Figure 3.6: $\pm 3\sigma$ variation of (a) V_{ref} (b) I_{ref}

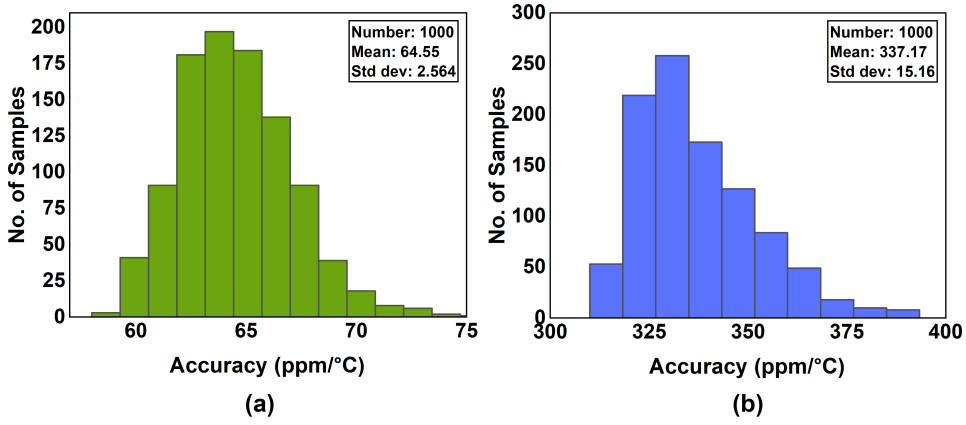

Figure 3.7: Monte Carlo results for TC of (a) V_{ref} (b) I_{ref}

Table 3.1: Performance summary and comparison with the state-of-arts

	This work	**[31]**	**[32]**	**[33]**	**[19]**	**[18]**	**[26]**	**[24]**
Technology(nm)	**90**	180	180	90	350	180	65	350
Type	**Vref/Iref**	Vref/Iref	Vref/Iref	Vref/Iref	Vref	Vref	Iref	Iref
V_{DD} (Supply range)	**1V-3.5V**	0.7V-2V	2-5V	1V-3V	1.4V-3V	0.8-2.2	1.2V-1.5V	1.3V-3V
Power(nW)	**37**	28	192	0.156	300	360	126560	88.53
V_{ref}(V)/I_{ref}(nA)	**0.820/3.23**	0.368/9.97	1.2/51	0.534/0.043	0.745/-	0.489/-	-/8800	-/9.95
$\sigma/\mu(\%)$	**1.34/1.75**	0.35/1.6	0.17/1.15	4.2/2	7/-	0.5/-	-/1.4	-/14.1
Trimming used	**No**	Yes	Yes	Yes	No	Yes	No	No
Temperature Range($^\circ$C)	**-40 - 100**	-40 - 125	-45 - 125	-55 - 100	-20 - 80	-30 - 110	0 - 100	-20 - 80
TC (ppm/$^\circ$C)	**62/332**	43.1/149.8	32.7/89	22/58	7/-	6.5/-	-/276.8	-/1190
Line Sensitivity (%/V)	**0.296/0.414**	0.027/0.6	0.058/1.76	0.029/0.059	0.002/-	0.076/-	-/4.5	-/0.046
PSRR (db@DC)	**-48**	-59	-46	-77	-45	-75	-	-
Area (mm^2)	**0.0112**	0.055	0.063	0.00157	0.056	0.0180	-	0.12
Resistors/Amplifiers/Thin oxide	**Not Used**	Used	Used	Used	Not Used	Not Used	Used	Not Used
Result Type	**Simulated**	Measured	Measured	Simulated	Measured	Simulated	Simulated	Measured

Table 3.1 summarizes the performance of the proposed voltage/current reference circuit and compares its performance with the state-of-the-art designs. The designs [31, 32, 33] present both voltage/current references in a single circuit. The usage of resistors in the design[31] increases its area to 0.055mm^2. The design [32] works for a minimum supply of 2V. Design [33] uses thin oxide devices to reduce its power consumption but usage of such devices has increased their process variations (σ/μ) to 4.2%/2%. When compared to the voltage reference designs [18] and [19], design [18] works for a high supply voltage $> 1.3V$, and design [19] consumes power greater than 350nW. Current reference designs [24] and [25] listed in Table 3.1 work for a supply voltage greater than $1V$, but design [24] exhibits a high-temperature coefficient of 1190ppm/^{o}C and substantial process variations. Furthermore, all these designs necessitate additional complex trimming circuitry, increasing the overall design area. Although the design [25] doesn't require trimming, it takes a huge power of 126.56μW and doesn't work for negative temperatures. The presented design in this thesis eliminates the need for external trimming circuitry while maintaining other specifications, with process variations (σ/μ) of 1.34%/1.75% that are comparable to post-trim results of state-of-the-art designs. To the best of the author's knowledge, this thesis presents a first and novel all-in-one trim-free, all-MOSFET V_{ref}/I_{ref} architecture.

3.4 Conclusion

This thesis presents a novel trim-free, low process variation, ultra-low power all CMOS voltage/current reference without using high-valued resistances, BJTs, or NVT devices. As it does not incorporate sub-threshold leakage behavior, it works over a wide temperature range of -40 to 100°C. The circuit consumes 37nW and works from a minimum supply of 1V over the wide supply range of 1V - 3.5V. The proposed architecture is trim-free, as the variations of the temperature coefficients and the nominal values of both the voltage and current references are insignificant. All the above competitive specifications make it a desirable choice for various ultra-low power wearables and IoT applications.

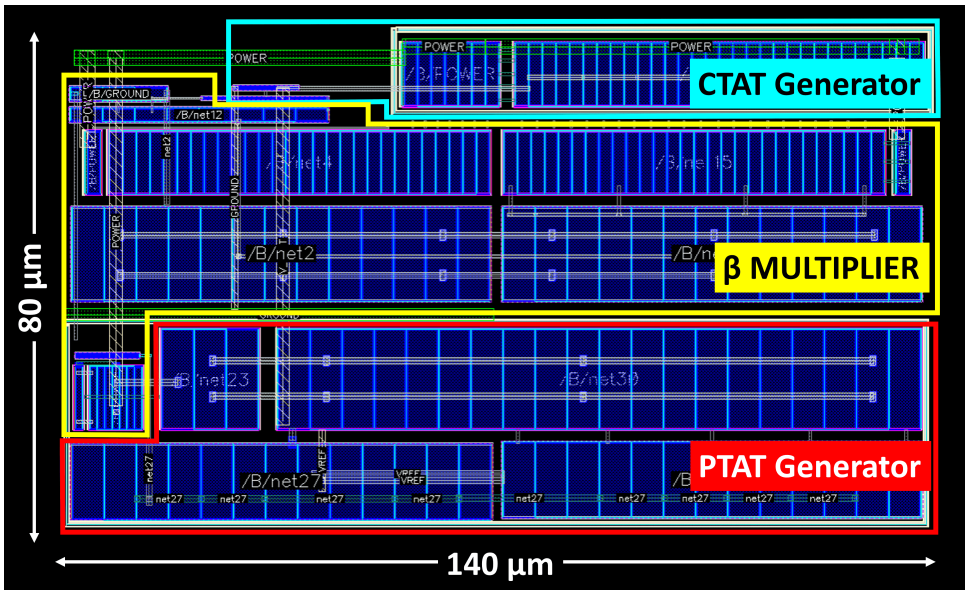

Figure 3.8: Layout of proposed voltage/current reference

Chapter 4

A 0.8-V, 593-pA Trim-free Duty-cycled All CMOS Current Reference for Ultra-Low Power IoT Applications

4.1 Introduction

The increasing need for wireless sensor networks (WSNs) and the Internet of Things (IoT) has led to a significant emphasis on the design of sub-threshold circuits that exhibit ultra-low power consumption [36]. Current references being essential components of any IoT system should also scale their power to satisfy the new requirements and make it ideal for power-constrained applications. Duty cycling has proven to be an effective technique in various applications, including wireless sensor networks, battery-powered devices, and Internet of Things (IoT) systems. By intelligently managing power consumption, duty cycling enables longer battery life, reduced energy costs, and improved overall system efficiency. Traditional current reference circuits often require meticulous manual calibration to compensate for process variations, temperature fluctuations, and aging effects. These calibration procedures not only add complexity to the manufacturing process but also contribute to increased manufacturing costs. By eliminating the need for manual calibration and offering enhanced accuracy and stability, the Trim-free architecture holds tremendous potential to improve the performance, reliability, and power efficiency of IoT devices.

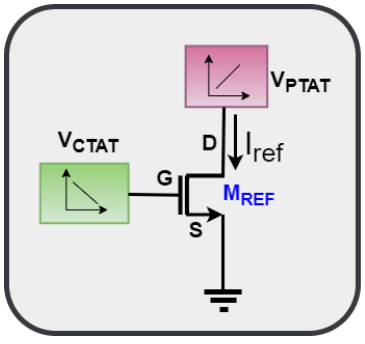

Figure 4.1: Concept of Proposed Current reference

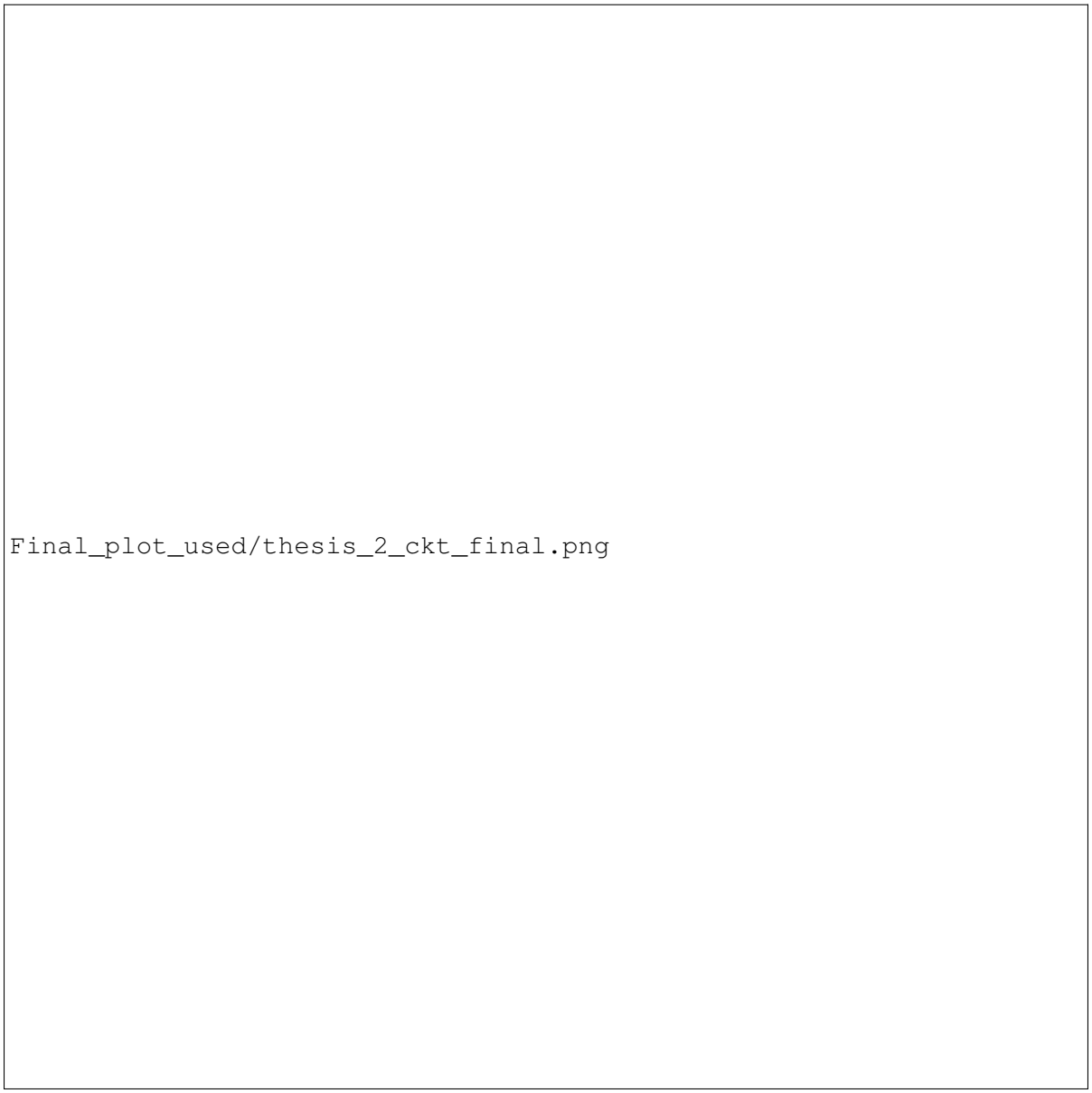

Figure 4.2: Complete schematic of proposed current reference

The conventional current references [37, 38, 39] typically employ resistor-based configuration to generate a stable reference current. However, a resistor-based design shows a significant trade-off arising in terms of area requirements as they demand a considerably larger area to scale the power consumption within the range of nW and pW. To mitigate this issue, [40] replaces the resistor in the beta-multiplier with a MOSFET in deep triode to achieve power consumption in nW but at the cost of high process variation and large voltage supply (Min. supply $=$ 1.2 V). [41] proposed a current reference with a lower supply and nW power consumption. However, the process variation (σ/μ) of the design is $>$ 10%. [42, 43, 44] proposed a trim-free current references without using resistors and operational

amplifiers. However, the architecture of those trim-free circuits requires a minimum supply of 1.4 V. Design [45] improves the process variation of the current reference with a process tracking circuit but the power consumption, line sensitivity, and temperature range make it unsuitable for low-power IoT applications. Design [46] proposed a current reference with low power and excellent line sensitivity but the minimum supply voltage is $>$ 1.2 V. Design [47] proposed a low-supply, low-power sub-nA current reference but a Temperature Coefficient(TC) of $>$500 ppm/^{o}C and requires an external complex trimming circuit to improve process variation of the design. [48] proposed a pico-watt resistor-less current reference with low line sensitivity at the cost of high-temperature variation (780 ppm/^{o}C) and supply voltage (Min. supply $>$ 1.2 V). [49, 50] proposed current references using tunneling currents, although these references require lower area, the susceptibility of tunneling currents to t_{ox} variations [51] ($>$ 600% across process corners) necessitates extensive trimming and increases the cost.

This thesis presents a sub-1V, sub-nA, duty-cycled, All-MOSFETs trim-free current reference without using resistors and amplifiers by applying a CTAT (complementary-to-absolute-temperature) voltage at the gate of the MOSFET (M_{ref}) and PTAT (proportional-to-absolute-temperature) voltage at the drain of M_{ref} as shown in Fig. 4.1. The subsequent sections of this thesis are organized as follows: Section 4.2 provides a comprehensive description of the design and analysis of the proposed current reference. In Section 4.3, the simulated results are presented and conclusions are drawn in Section 4.4.

4.2 Design and analysis of the proposed Current reference

The schematic of the proposed design, as illustrated in Fig. 4.2, comprises several key components. These include a current source bias circuit, a CTAT generator, and a sub-threshold triode-resistor-based beta-multiplier. The biasing circuit creates a current by employing a self-biasing beta-multiplier circuit with a triode resistor [52]. This bias current is used to establish the CTAT voltage. The CTAT generator, based on a differential pair configuration, produces an output voltage that works as the gate-source voltage of the MOSFET M_{ref}. This MOSFET operates in the sub-threshold triode region, resulting in low power consumption. Concurrently, a PTAT voltage, crucial for temperature compensation, needs to be applied as the drain-source voltage of MOSFET M_{ref}. This is achieved with the assistance of the beta-multiplier, ensuring that the generated current, denoted as I_{ref}, remains independent of variations in temperature, process, and voltage. By integrating these components and leveraging their functionalities, the proposed design aims to achieve robust and precise performance across different operating conditions, making it suitable for a wide range of applications.

4.2.1 Temperature Compensation of Proposed Current Reference

As shown in Fig. 4.2, the current I_{ref} is determined by the MOS resistor M_{ref}, where the gate-source voltage is $V_{GS,M_{ref}}$ and the drain-source voltage is $V_{DS,M_{ref}}$. When the MOSFET M_{ref} operates in the sub-threshold triode region, characterized by $V_{GS} < V_{TH}$ and $V_{DS} < V_T$, the current through M_{ref}

can be described by (4.1) as:

$$I_{ref} = K_n \frac{W}{L} (\eta - 1) V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)\left(1 - \exp\frac{-V_{DS}}{V_T}\right) \tag{4.1}$$

where $K_n = \mu_n C_{ox}$, V_{TH} represents the threshold voltage of the transistor, V_T is the thermal voltage and η is the sub-threshold slope constant. To simplify (1), we can approximate the term $\left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right)$ as $\frac{V_{DS}}{V_T}$, leveraging the binomial expansion of the exponential function for cases where $\frac{V_{DS}}{V_T}$ is less than 1. This approximation allows us to rewrite (4.1) as (4.2) i.e.

$$I_{ref} = K_n \frac{W}{L} (\eta - 1) V_T \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) V_{DS} \tag{4.2}$$

Achieving temperature-independent current ($\frac{\partial I_{ref}}{\partial T}$ = 0) requires accounting for the variations in μ_n, V_T and V_{TH} with temperature. Thus, to ensure a temperature-independent current from the M_{ref}, $V_{GS,M_{ref}}$ and $V_{DS,M_{ref}}$ are designed as the functions of temperature. Temperature compensation is a crucial aspect of current reference design to ensure accurate and stable performance. In our design, we incorporate a CTAT generator and a PTAT generator to achieve temperature compensation. The CTAT generator connects a CTAT voltage to the gate of MOSFET M_{ref}. It consists of an NMOS differential pair and a current mirror, which is biased using a current source bias circuit (I_{bias}). When the MOSFETs operate in the sub-threshold region, the output voltage of the CTAT generator i.e. $V_{GS,M_{ref}}$ can be expressed using (4.13)

$$\begin{aligned} V_{GS,M_{ref}} &= V_{GG} + V_1 \\ &= \eta V_T \ln\left(\frac{K_{M14}K_{M17}}{K_{M13}K_{M18}}\right) + V_{th} + \eta V_T \ln\left(\frac{I_{bias}}{I_0}\right) \\ &= V_{TH} + \eta V_T \ln\left(\frac{K_{M14}K_{M17}I_{bias}}{K_{M13}K_{M18}I_0}\right) \end{aligned} \tag{4.3}$$

Where $I_0 = K_n(\eta - 1)V_T^2$, V_{GG} is the gate-to-gate voltage of the CTAT generator, and V_1 is the output voltage of the current source bias circuit which acts as an input to the CTAT generator.
In the proposed circuit, PTAT voltage is generated at the drain of M_{ref} using a supply-independent beta-multiplier circuit. The drain-to-source voltage of MOSFET M_{ref} serves as the PTAT voltage. The V_{DS} of M_{ref} can be expressed as :

$$\begin{aligned} V_{DS,M_{ref}} &= V_{GS,M21} - V_{GS,M22} \\ &= \eta V_T \ln\left(\frac{W_{22}L_{21}}{W_{21}L_{22}}\right) \\ &= \eta V_T \ln(n) \end{aligned} \tag{4.4}$$

where $\frac{W_{22}}{L_{22}} = n\frac{W_{21}}{L_{21}}$ and $n > 1$, to make the V_{DS} of M_{ref} a PTAT voltage. By substituting the expressions for $V_{GS,M_{ref}}$, and $V_{DS,M_{ref}}$ from (3) and (4) into (2), we obtain the expression for I_{ref} in terms of temperature.

$$I_{ref} = K_n \frac{W}{L} \eta(\eta - 1) V_T^2 \ln(n) \left(\frac{K_{M14}K_{M17}I_{bias}}{K_{M13}K_{M18}K_n(\eta - 1)V_T^2}\right) \tag{4.5}$$

$$I_{ref} = \eta \frac{W}{L} \ln(n) \left(\frac{K_{M14} K_{M17} I_{bias}}{K_{M13} K_{M18}} \right) \tag{4.6}$$

(4.5) provides the derived expression, taking into account various transistor parameters and the current source bias circuit. Simplifying (4.5), we arrive at (4.6), which reveals that the terms within the equation are temperature-independent. Consequently, we can conclude that the generated current reference exhibits temperature invariance, ensuring stable operation across a wide temperature range of -40 to 100°C.

4.2.2 Process variation of the proposed current reference

To study the effect of process variation on the current reference, one needs to check the process variant terms present in the equations I_{ref}. (4.2) highlights the significance of the threshold voltage, which plays a key role in process variation [53]. The equation includes $V_{GS,M_{ref}}$, which can be expressed as $V_{GS,M_{ref}} = V_{TH} + \eta V_T \ln\left(\frac{K_{M14} K_{M17} I_{bias}}{K_{M13} K_{M18} I_0}\right)$. Substituting the value of $V_{GS,M_{ref}}$ into (4.2) we get :

$$I_{ref} = K_n \frac{W}{L} \eta(\eta - 1) V_T^2 \exp\left(\frac{V_{TH} + \eta V_T \ln(\frac{K_{M14} K_{M17} I_{bias}}{K_{M13} K_{M18} I_0}) - V_{TH}}{\eta V_T}\right) \tag{4.7}$$

In (4.7), there is a cancellation of the V_{TH} term, leading to an improvement in the process variation of the reference current. Fig. 4.7(b) depicts the value of $V_{GS,M_{ref}} - V_{TH,M_{ref}}$ at different process corners, demonstrating minimal variation. By examining the equations and considering the cancellation of the V_{TH} term, we can say that the reference current is less susceptible to process variations.

4.2.3 Improvement in Line Sensitivity of the Proposed Current Reference

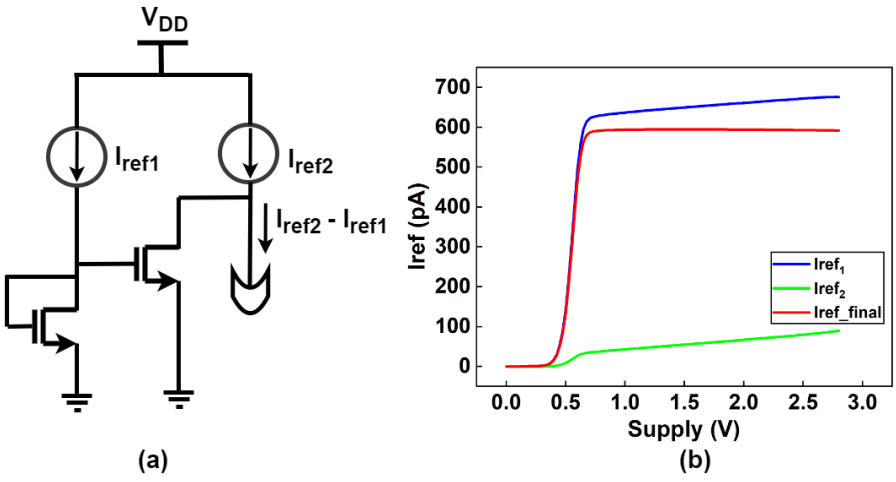

Figure 4.3: (a) Concept of subtracting two current references (b) Simulation of Subtracted current references

In the proposed design, we have implemented a technique to enhance the line sensitivity of the reference current [54]. The technique involves generating a reference current with improved line sensitivity by subtracting two temperature-compensated current references: one with normal line sensitivity (I_{ref1}) and the other with poor line sensitivity (I_{ref2}) as shown in Fig. 4.3(a). These current references are derived from beta-multiplier structures. The equation for the reference current with improved line sensitivity is given as

$$I_{ref} = I_{ref1} - p * I_{ref2} \tag{4.8}$$

where p represents the coefficient of subtraction. To achieve this, we intentionally designed I_{ref2} to have a greater variation with supply voltage (V_{DD}) compared to I_{ref1}. This is accomplished by reducing the lengths of the NMOS transistors and modifying the current mirror architecture. Fig. 4.3(b) illustrates the variations of I_{ref1}, I_{ref2}, and I_{ref} with respect to the supply voltage (V_{DD}). Based on the data analysis, we can approximate the equations for I_{ref1}, I_{ref2}, and I_{ref} in terms of V_{DD} as

$$I_{ref1} = A * V_{DD} + c_1 \quad and \quad I_{ref2} = B * V_{DD} + c_2 \tag{4.9}$$

$$I_{ref} = (A - p * B) * V_{DD} + (c_1 - p * c_2) \tag{4.10}$$

Where A and B are the slopes of I_{ref1} and I_{ref2} respectively. To ensure the desired line sensitivity of the reference current, the value of p is chosen such that the difference between A and $p * B$ approaches zero. Since the slope of B is greater than that of A, selecting $p < 1$ meets our requirement but a small value of p may increase the offset that may occur during the mirroring of I_{ref2} due to the absence of a cascode structure in the beta-multiplier. By considering the aforementioned suggestions, we can enhance the circuit's performance, particularly its line sensitivity, beyond what is achievable with a conventional cascode beta-multiplier-based current reference. This improvement is attained by completely eliminating the first-order dependence on the supply voltage through the appropriate selection of the coefficient p. These advancements signify significant progress in performance, offering enhanced stability and reduced sensitivity to changes in the supply voltage.

Table 4.1: Performance summary and comparison with the state of arts

	This work	**[43]**	**[44]**	**[42]**	**[40]**	**[47]**	**[48]**	**[46]**
Technology (nm)	**90**	180	65	180	180	180	180	350
V_{DD} (Supply range)	**0.8 - 2.5 V**	1 - 2 V	1.25 - 1.4 V	1.5 - 2.4 V	1.2 - 1.8 V	0.7 - 2 V	1.2 - 4V	1.3 - 3 V
Power(nW)	**3.3**	1231	550	1.02	670	1.06	0.023	88.53
I_{ref} (nA)	**0.593**	142.5	104.2	35	92.3	0.192	0.020	9.95
Process Variation ($3\sigma/\mu$)	**0.75**%	9.4%	4%	4.3%	18.4%	-	-	42%
Trimming used	**No**	No	No	No	No	Yes	Yes	Yes
Temperature Range (°C)	**-40 - 100**	-40 - 85	-45 - 85	-40 - 120	-40 - 85	-20 - 80	0 - 80	-20 - 80
TC (ppm/°C)	**378**	40	48	282	179.9	546	780	1190
Line Sensitivity (%/V)	**0.198**	1.45	1.9	3	7.5	0.51	0.58	0.046
Area (mm^2)	**0.074**	0.02	0.0031	0.017	0.0007	-	0.0484	0.12
Resistors/Amplifiers	**Not Used**	Not Used	Not Used	Not Used	Not Used	Not Used	Used	Not Used
Result Type	**Simulated**	Simulated	Simulated	Measured	Measured	Simulated	Measured	Measured

4.2.4 Duty-cycling of Proposed Current Reference

As shown in Fig. 4.4, the CTAT generator is designed to operate in a duty-cycled manner in order to conserve power. Without duty-cycling, the overall power consumption amounts to 52.8 nW, with the CTAT generator accounting for approximately 95% of this total. However, by implementing a duty-cycling scheme of 1.33% on the CTAT generator, a power saving of around 94% is achieved. In addition to employing this duty-cycling technique, a start-up circuit is needed for the bias circuit beta-multiplier to guarantee a correct output when duty-cycled switches are ON [55] whereas, always ON current reference core beta-multipliers require a single pulse startup circuit to generate the reference current.

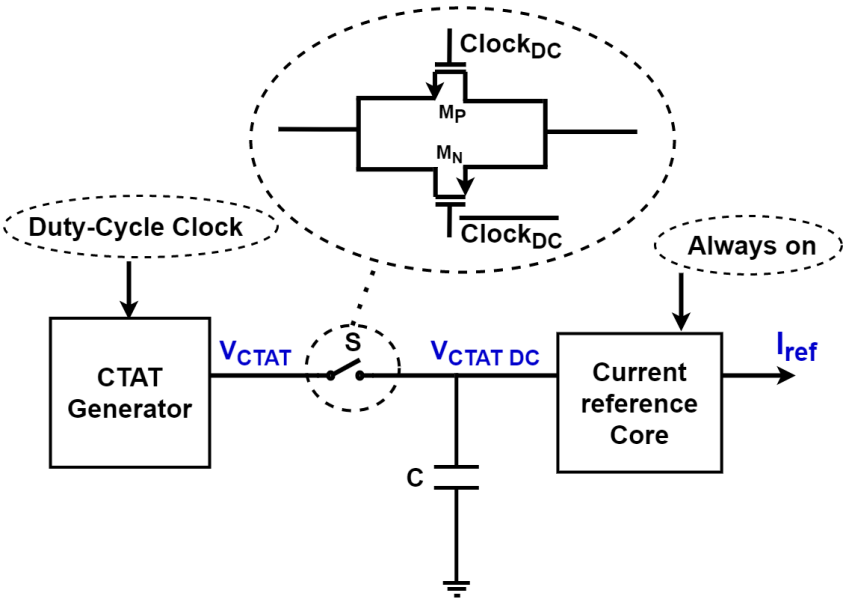

Figure 4.4: Duty-cycling schematic

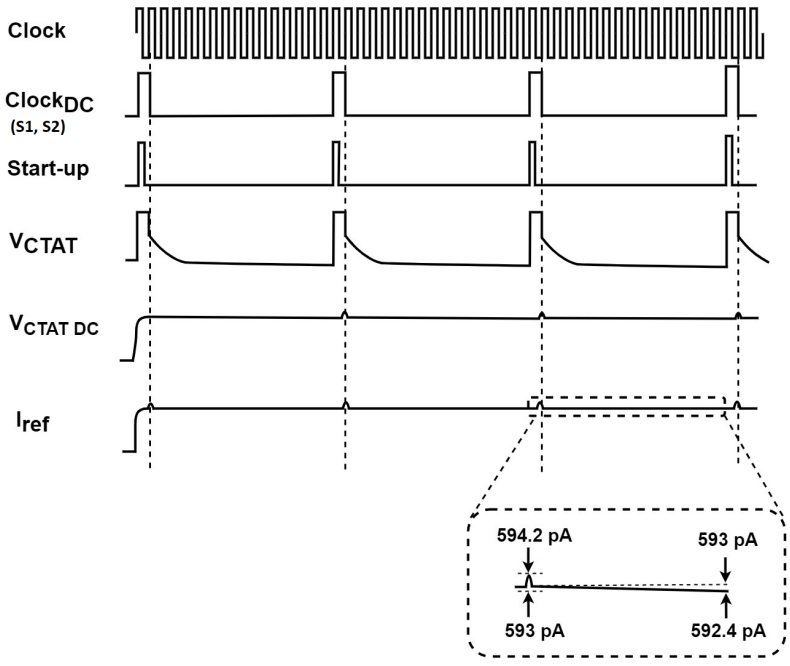

Figure 4.5: The timing waveform of the current reference

The timing diagram for the current reference operation is illustrated in Fig. 4.5. In the background, a real-time clock continuously operates to provide a low frequency, driven by a low-frequency oscillator [56]. Additionally, a duty-cycled clock with an active time of 1.33% is used to provide the necessary clock signal (Clock$_{DC}$) to the switch (S1, S2). As shown in Fig. 4.5 a startup pulse is generated by

using combinational logic with a duty-cycled clock. The start-up time in this work is approximately 1.5 ms. The retention time of the voltage on the capacitor depends on the leakage of the switch, which increases by more than 100 times at higher temperatures than at room temperature. However, since our switch is biased in the super-cutoff region, the sub-threshold leakage of our switch is drastically reduced by 1000 times. Also, higher t_{ox} devices make the gate leakage negligible. The drain-bulk leakage is not dominant for $< 125°$C temperature[57]. however, NMOS and PMOS in the transmission switch are sized to further reduce the impact of drain-to-bulk leakage by 5 times in the worst corner[58]. As a result, the dominating leakage present in our switch is sub-threshold leakage. The output of the CTAT generator ($V_{CTAT,DC}$) is stored on a capacitor, and this stored output serves as the input to the current reference core, which then generates the reference current. As shown in Fig. 4.5, the reference current (I_{ref}) shows an undesirable glitch of 1.2 pA while switching and leakage of only 0.6 pA during the hold state.

4.3 Result and discussion

The current reference design proposed in this work has been successfully implemented using a 90nm CMOS process. In Fig. 4.6(a), the temperature-compensated current reference plot is presented, demonstrating a temperature coefficient (TC) of 378 ppm/°C across a wide temperature range of -40° to 100°C. This indicates the ability of the current reference to maintain stability and accuracy despite changes in temperature. Furthermore, Fig. 4.6(b) showcases the supply sensitivity plot for the current reference, revealing an outstanding line sensitivity of 0.198%/V. This confirms the effectiveness of the subtraction methodology employed to enhance the circuit's performance in terms of line sensitivity, as discussed in the earlier sections of this thesis. In Fig. 4.7(a), the generated current reference is shown to have a process variation of 1.5% across the process corners and Fig. 4.7(b) presents the plot of $V_{GS} - V_{TH}$ versus temperature, showcasing the minimal variation in voltage across five different process corners. This variation ensures that the current remains nearly unaffected by process variations, resulting in reliable and consistent performance. Fig. 4.10(a) displays the Monte Carlo simulation results for the current reference (I_{ref}) over a temperature range of -40 to 100°C. The mean value and standard deviation obtained from these simulations are 593 pA and 1.501 pA respectively. These results demonstrate that the $\pm 3\sigma/\mu$ variation amounts to $\pm 0.75\%$ in the generated current reference. Similarly, Fig. 4.10(b) exhibits the Monte Carlo simulation results (based on 1000 data points) for the temperature coefficient (TC) of the current reference (I_{ref}). The mean and standard deviation observed for the TC is 430.08 ppm/°C and 57.1 ppm/°C respectively. Fig. 4.9 illustrates the layout of the proposed current reference occupies an area of 0.074 mm^2. Fig. 4.10 (a) & (b) depict the startup time and average power distribution of the proposed current reference respectively.

Table 4.1 presents a comprehensive overview of the performance metrics achieved by the proposed current reference circuit. It also includes a comparative analysis of these metrics in relation to the state-of-the-art designs. In comparison to the reference circuits [42] [43] [44], the proposed design

stands out for its utilization of a low-voltage power supply, excellent line sensitivity, and reduced power consumption. Furthermore, when compared to the design discussed in references [47] [48], which also focuses on low power consumption, the proposed design exhibits a smaller temperature coefficient and eliminates the need for an external calibration circuit. One of the key highlights of the proposed work is its exceptional performance in terms of process variation. With a process variation of 1.5% ($\pm 3\sigma/\mu$) without the need for trimming across different process corners, the proposed design outperforms the mentioned reference circuits based on the author's current knowledge.

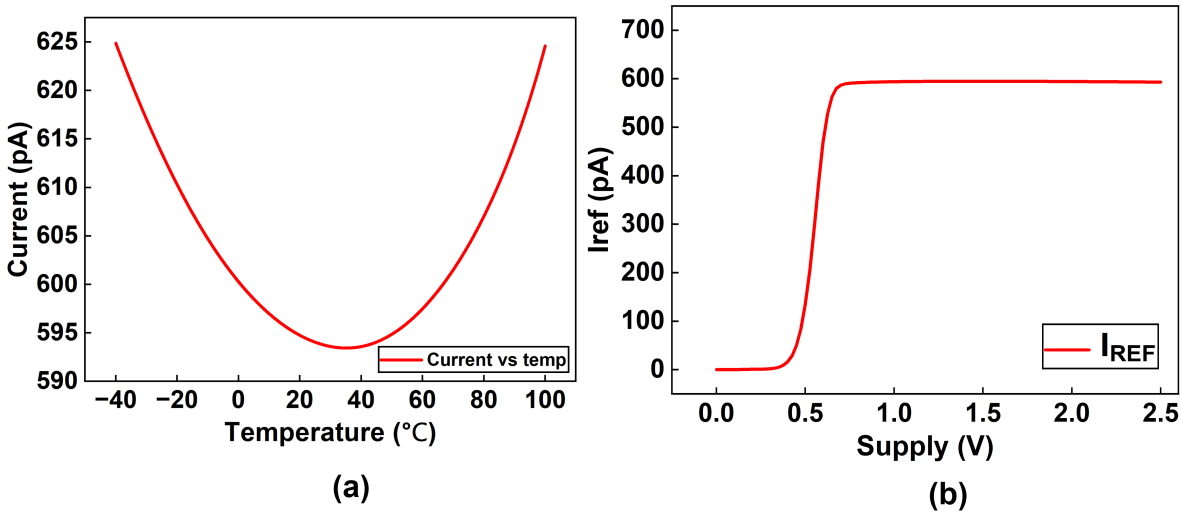

Figure 4.6: (a) I_{ref} vs Temperature (b) Supply sensitivity of I_{ref}

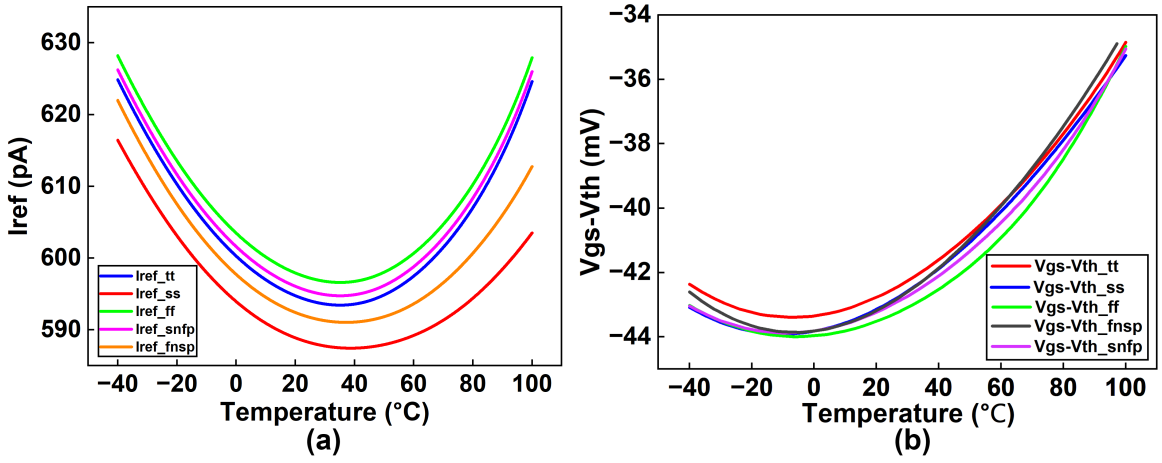

Figure 4.7: Process corner plots for (a) I_{ref} vs Temperature (b) V_{GS}-V_{TH} vs temperature

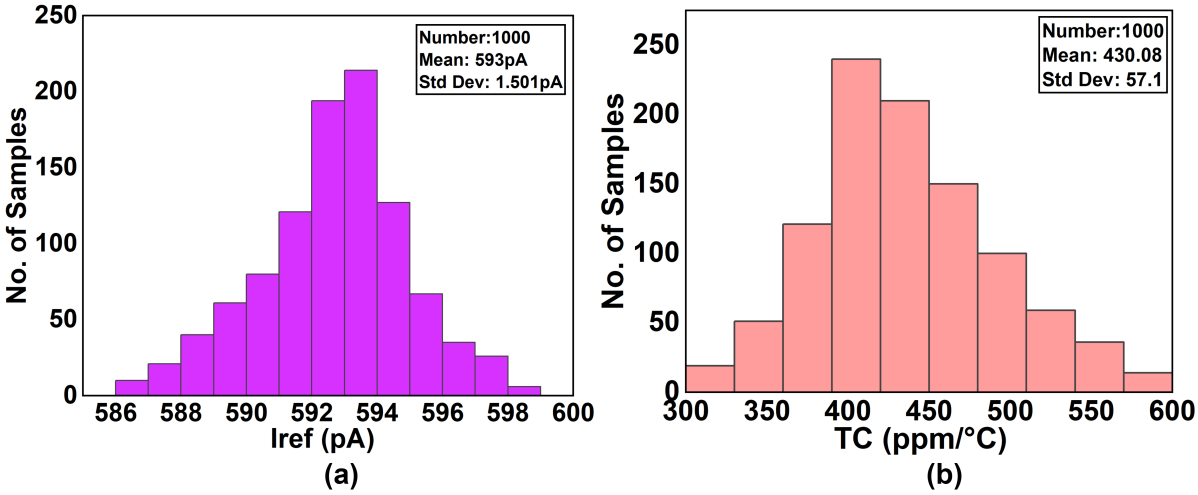

Figure 4.8: (a) Monte Carlo results for (a) I_{ref} @27°C (b) Temperature Coefficient of I_{ref}

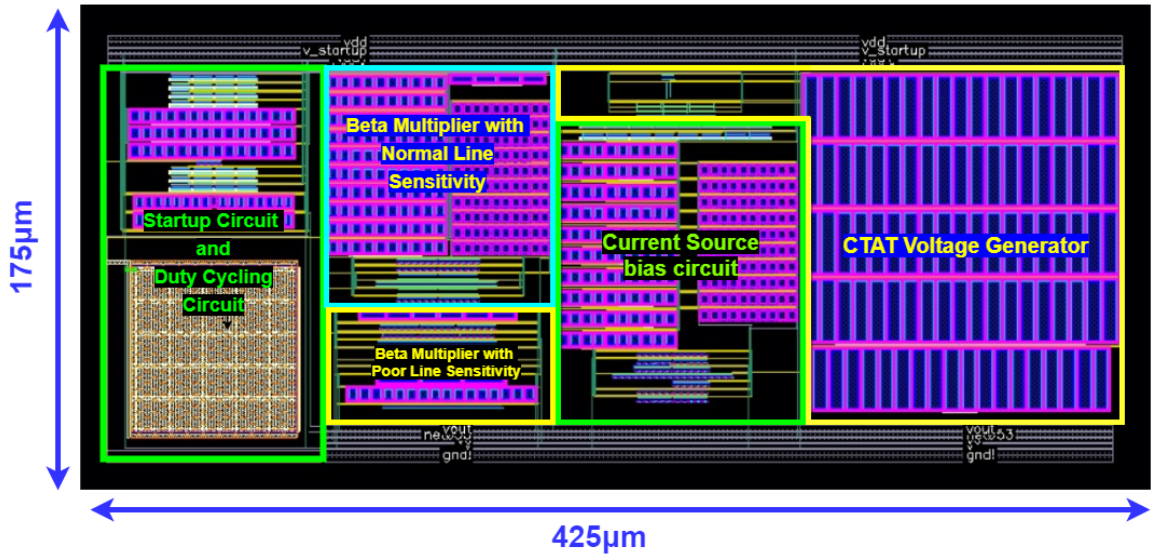

Figure 4.9: Layout of the proposed current reference

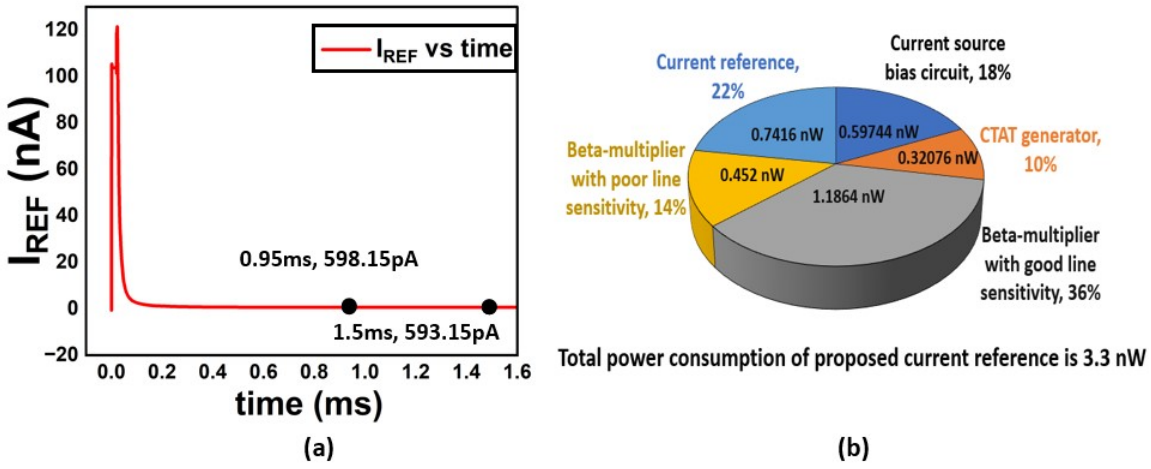

Figure 4.10: (a) Startup time of I_{ref} (b) The average power distribution of proposed current reference

4.4 Conclusion

This work presents a novel 0.8 V, 593 pA trim-free duty-cycled all CMOS-based current reference without using high-valued resistors, amplifiers, and thin oxide devices. Simulation results indicate that the design has a small variation in output current, with a deviation of 1.5% ($\pm 3\sigma/\mu$) across the process corners. Additionally, the design shows a line sensitivity of 0.198%/V and a temperature coefficient (TC) of 378 ppm/°C over a wide temperature range of -40 to 100°C. After incorporating duty cycling, which is an efficient power-saving technique, the circuit achieves a power consumption of only 3.3 nW. By using a transmission gate-based duty-cycling circuitry, the proposed design enables active operation with a duty cycle of 1.33%, significantly improving power efficiency. All the above specifications establish it as an attractive option for a diverse range of ultra-low power IoT and biomedical applications.

Chapter 5

A 0.6V, 13nW, 0.0012%/V Line Sensitivity PVT - Invariant Voltage Reference without using Resistors and Amplifiers

5.1 Introduction

A pivotal research area in semiconductor technology centres is on the advancement of ultra-low-power System-on-Chips (SoCs) and Large-Scale Integrations (LSIs) tailored for applications such as the Internet of Things (IoT), portable mobile devices, implantable medical devices, and wearables. These domains prioritize minimal power consumption. Designing voltage/current sources that are good enough to act as ideal source invariant to temperature, main supply, and FEOL corners in the fabrication process is challenging. Voltage/current references, integral to IoT systems, must align their power scalability with evolving requirements. A critical objective is to achieve operational proficiency over a wide temperature range, ensuring accuracy and line sensitivity without relying on external trimming circuits. Trim-free designs eliminate the need for external calibration, reduce manufacturing costs, and improve the circuit's reliability. Furthermore, it is beneficial to integrate both the reference circuitry (voltage and current) into a single block.

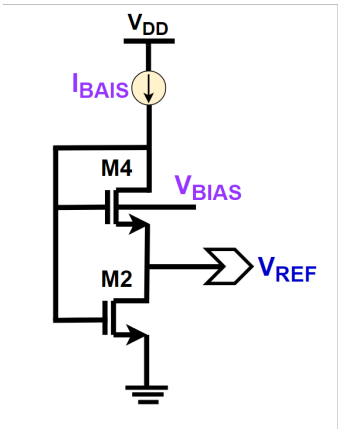

Figure 5.1: Basic Concept of Proposed voltage reference

The voltage reference is a main block in many Analog, Digital and Mixed-Signal integrated circuits, Socs, AD/DA converters, operational amplifiers, etc. The main need for Voltage reference is to design a customised voltage source independent of the supply voltage of the system and temperature. In contemporary research, numerous voltage references have been introduced and categorised according to their underlying operational principles as Band-Gap References (BGR) and CMOS-Voltage References (CVR).

The basic idea behind designing a voltage reference is to add up CTAT and PTAT voltages in the correct proportions. Basic BGR was implemented by adding a PTAT voltage to V_{BE} of BJT [59]. This basic design consists of many errors, which include improper current mirroring, error voltages in the clamping circuit, and device mismatches and is non-reliable because of high supply, high power consumption because of the use of BJT, large silicon area and high noise because of the use of Resistors(order of Mega ohms). Proper current mirroring and voltage clamping are achieved with the help of an operational amplifier in negative feedback, as explained in [60]. Though the errors were resolved, reliability has not been achieved yet.

The focus now shifted from BGR to CVR(CMOS-Voltage Reference)[61] which are designed without BJT's as it is one of the reason for high power consumption though better for process invariations. But still, power consumption is in the order of micro Watts, high supply voltage(¿1.4V), involves the use of large order resistors, and significant process variations as reference voltage value in this design depend on threshold voltages of NMOS and PMOS.[62] was designed with less supply voltage(0.75V), less power(250nW) but carries remaining concerns.[63] presents a resistor-less voltage reference with nW power consumption, but external trimming circuitry is required to correct the process variation of the design. Reference [64] introduces a trim-free voltage reference, sharing comparable specifications with [63] albeit with a trade-off in process variation amounting to 2.35%. Meanwhile, [65] exhibits an enhancement with lower process variation (0.9%) compared to [64], albeit at the expense of increased power consumption, reaching 300nW.

The proposed work is a low-power, low-voltage, All-MOSFET's PVT invariant voltage reference without using an extra calibration circuit that deals with all the above concerns, improving the specifications, which include temperature coefficient, line sensitivity, working temperature range, working supply range, process invariation($\frac{\sigma}{\mu}$) ratio.

Basic concept of proposed voltage reference is shown in Fig. 5.1. The remaining sections of this work are organized as follows: Section 5.2 provides an in-depth explanation of the design and analysis of the proposed voltage reference. In Section 5.3, we present the results of our study and engage in a discussion surrounding them. Finally, in Section 5.4, we draw conclusions based on the findings discussed earlier.

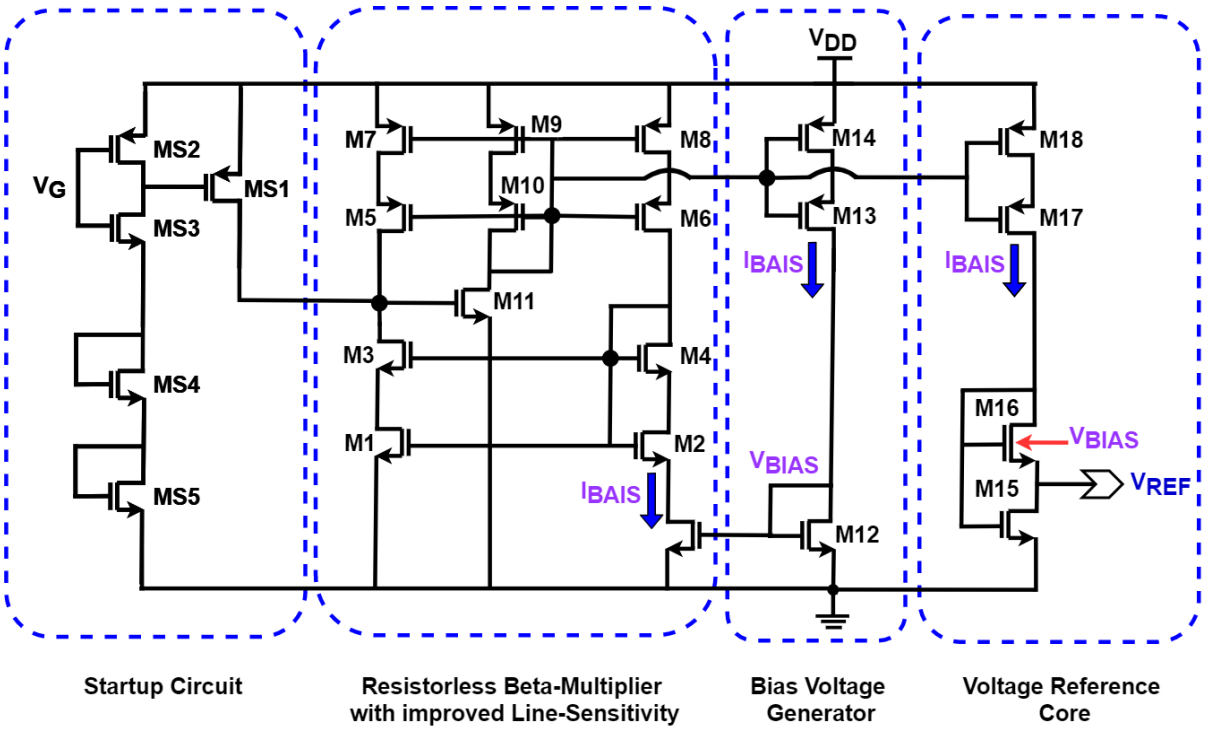

Figure 5.2: Proposed Voltage Reference

5.2 Design and Analysis of proposed voltage reference

The schematic of the proposed voltage reference is shown in Fig.2. The design consists of Current bias generator(I_{bias}) with excellent line sensitivity, voltage reference core with body bias ciruit. The body bias circuit helps to achieve temperature compensation by providing a bias voltage (V_{GSM12}, the gate-to-source voltage of MOSFET M12) at the bulk of MOSFET M16. The excellent line-sensitivity of proposed voltage reference is due to the Supply-independent bias current(I_{bias}) used in the design. To enhance the power supply rejection ratio (PSRR) at higher frequencies, a capacitor(C_{eq}=2.17pF) is integrated using a thick oxide device (M$L0$) and connected to the output terminal. Additionally, a start-up circuit is incorporated to ensure smooth initialization of the system and with an aim to mitigate any potential degenerative circumstances.

5.2.1 Current generator with improved line-sensitivity

Within the circuit, the current I_{BIAS} is produced through the utilization of MOS resistor M_{res}, employing gate-source voltage V_{BIAS} and drain-source voltage $V_{DS,M_{res}}$. When MOSFET M_{res} is in operation and functioning within the strong inversion and deep triode region (V_{BIAS} - $V_{TH} > V_{DS,M_{res}}$),

the current passing through M_{ref} can be determined by the following equation:

$$I_{BIAS} = K_n \left(\frac{W}{L}\right)(V_{BIAS} - V_{TH})V_{DS,M_{res}} \tag{5.1}$$

Where, K_n= $\mu_n C_{ox}$, $\frac{W}{L}$ is the aspect ratio of the MOSFET M_{res} and $V_{DS,M_{res}}$ = $V_{GS,M1}$ - $V_{GS,M2}$.

All the MOS except M_{res} in our improved beta multiplier are working under sub-threshold saturation and so the current equation will be

$$I_D = I_S \left(\frac{W}{L}\right) exp\left(\frac{V_{GS} - V_{TH}}{\eta V_t}\right) \tag{5.2}$$

and so

$$V_{GS} = V_{TH} + \eta V_T ln\left(\frac{I_D}{I_S \frac{W}{L}}\right) \tag{5.3}$$

$$V_{DS,M_{res}} = V_{GS,M1} - V_{GS,M2} = \eta V_t ln\left(\frac{I_{MN1} S_{MN2}}{I_{MN2} S_{MN1}}\right) \tag{5.4}$$

Substituting (4) in (1) and upon simplification we get bias current as

$$I_{BIAS} = K_n \left(\frac{W}{L}\right)(V_{BIAS} - V_{TH})\eta V_t ln\left(\frac{I_{MN1} S_{MN2}}{I_{MN2} S_{MN1}}\right) \tag{5.5}$$

Traditional beta multiplier with four MOS in positive feedback and loop gain less than 1, has less accuracy because of short channel effects and is highly sensitive to supply variations. Instead, cascode topology can be used, but it requires a high supply voltage. To ensure a high PSRR value, a high swing cascode topology in negative feedback is used. Without negative feedback, because of asymmetry and short channel effects, drain-source voltages of (M5, M6) and (M8, M9) cannot be equal, resulting in improper current mirroring. For that, an operational amplifier in negative feedback can be used to ensure equal drain voltages of M5 and M6, but an operational amplifier uses a large area, can add unnecessary poles to the system, results in excessive power consumption. Instead, a CS amplifier(M11) is used to ensure negative feedback and to equate drain-source voltages in the design. From Fig. 5.2, the feedback can be mathematically explained as follows:

$$i_{bias} = g_{m8}(v_{dd} - v_{g6}) \tag{5.6}$$

$$v_{g4} = v_{d6} \approx g_{m8} R_8 g_{m6} R_6 (v_{dd} - v_{g6}) \tag{5.7}$$

$$v_{g11} = v_{d3} \approx -g_{m1} R_1 g_{m3} R_3 (v_{g4}) \tag{5.8}$$

$$v_{g10} = v_{d11} = v_{g6} \approx -g_{m11} R_{11} (v_{g11}) \tag{5.9}$$

In the above set of equations, i_{bias} is the small variation in current because of the variation in supply. g_1,g_3,g_6,g_8,g_{11} are transconductance R_1,R_3,R_6,R_8,R_{11} are resistance of M1,M3,M6,M8,M11 respectively. Upon simplification of 6-9,

$$v_{g8} = v_{g6} \approx \left(\frac{g_{m1} R_1 g_{m3} R_3 g_{m6} R_6 g_{m8} R_8 g_{m11} R_{11}}{1 + g_{m1} R_1 g_{m3} R_3 g_{m6} R_6 g_{m8} R_8 g_{m11} R_{11}}\right) v_{dd} \tag{5.10}$$

Small variation in current i_{bias} will be

$$\begin{aligned} i_{bias} &= g_{m8}(v_{dd} - v_{g6}) \\ &\approx g_{m8}\left(\frac{1}{1 + g_{m1}R_1 g_{m3}R_3 g_{m6}R_6 g_{m8}R_8 g_{m11}R_{11}}\right) v_{dd} \end{aligned} \tag{5.11}$$

Above equation(11) clearly states that small variation in current is inversely proportional to the value of the order $(g_m r_o)^5$ which makes i_{bias} very small compared with v_{dd}.

5.2.2 Temperature Compensation of proposed Voltage reference

The Bias current I_{bias} passing through MOSFET's M15 and M16 and generated a temperature independent voltage at the drain of MOSFET M15.

$$\begin{aligned} V_{ref} &= V_{GS,15} - V_{GS,16} \\ &= V_{TH,15} - V_{TH,16} + \eta V_T \ln\left(\frac{K_{M16}}{K_{M15}}\right) \end{aligned} \tag{5.12}$$

Body effect is observed in MOSFET M16 because it's body is controlled by V_{BIAS}.Hence,

$$V_{ref} = \gamma(\sqrt{2\phi_F} - \sqrt{2\phi_F + V_{SB,16}}) + \eta V_T \ln\left(\frac{K_{M16}}{K_{M15}}\right) \tag{5.13}$$

Where, ϕ_F is the fermi potential and $V_{SB,16}$ is the source to bulk voltage of MOSFET M16 equal to $V_{ref} - V_{BIAS}$. V_{BIAS} is the gate-source voltage of the diode-connected MOSFET M12, which has negative tc because of the dominant CTAT nature of V_{th} compared with the PTAT nature of I_{BIAS}. Hence, the term $\gamma(\sqrt{2\phi_F} - \sqrt{2\phi_F + V_{ref} - V_{BIAS}})$ is CTAT in nature and the term $\eta V_T \ln\left(\frac{K_{M16}}{K_{M15}}\right)$ is PTAT in nature. Both can be compensated by choosing appropriate sizing ratio $\left(\frac{K_{M16}}{K_{M15}}\right)$.

5.2.3 Line sensitivity of voltage reference

Above in part A, expressions of i_{bias}, $(v_{dd} - v_{g6})$ are shown because of supply variations. Now let's see the variation in V_{BIAS} which is v_{bias}.

$$v_{dd} - v_{g6} \approx \left(\frac{1}{1 + g_{m1}R_1 g_{m3}R_3 g_{m6}R_6 g_{m8}R_8 g_{m11}R_{11}}\right) v_{dd} \tag{5.14}$$

$$v_{bias} = \left(\frac{g_{m14}}{g_{m12}}\right)(v_{dd} - v_{g6}) \tag{5.15}$$

V_{BIAS} is controlling body voltage of M16 to ensure less variation in threshold voltage of M16. Small signal analysis on Voltage reference core is implemented to find variation in V_{REF} which is v_{ref} which mainly includes finding short circuit current when node V_{REF} is AC grounded. Consider $v_{g16} = v_{g15} = v_{d16}$ be v_d.

$$v_d = \frac{g_{m18}(v_{dd} - v_{g6}) - g_{mb16}v_{bias}}{g_{m16}} \tag{5.16}$$

Here, g_{mb16} is the back gate transconductance due to body-source voltage. The short circuit current flowing through AC grounded node(V_{REF}) which is(say i_x

$$i_x = \left(\frac{g_{m15}g_{mb16}}{g_{m16}}\right)(v_{dd} - v_{g6}) \tag{5.17}$$

Output impedance is $\frac{1}{g_{m15}}$

$$v_{ref} \approx \left(\frac{g_{mb16}}{g_{m16}}\right)\left(\frac{v_{dd}}{1 + g_{m1}R_1g_{m3}R_3g_{m6}R_6g_{m8}R_8g_{m11}R_{11}}\right) \tag{5.18}$$

Variation in reference voltage(v_{ref}) is very less than variation in current(i_{bias}) as g_{mb16} is much less than g_{m16}.

5.3 Results and Discussion

The proposed voltage reference is designed in 180nm CMOS process. The proposed voltage/current reference is designed and implemented in a 90nm CMOS process. Fig. 5.2(b) shows the PSRR at DC for the voltage reference at 1V, 1.8V, and 3V are -48dB, -52dB, and -51dB respectively. Fig. 5.3(a) shows temperature-compensated voltage and current reference plots; it depicts temperature coefficients (TC) of 62ppm/°C and 332pm/°C respectively for the temperature range of -40 to 100°C. Fig. 5.3(b) shows the supply sensitivities of voltage and current references as 0.296%/V and 0.414%/V respectively for the supply range of 1 to 3.5V. As this architecture contains a self-biased loop, to avoid any degenerative conditions, a start-up circuit is added. Fig. 5.4 shows the 99% settling times for the voltage and current reference to be 11.73ms and 11.84ms, respectively. The statistical results for voltage and current reference are presented in Fig. 5.5 Using Monte Carlo simulation with 1000 samples the observed mean and standard deviation from Fig. 5.5(a) for the voltage reference are 820mV and 10.99mV respectively, which results in process variation (σ/μ) of 1.34%. Fig. 5.5(b) illustrates the Monte Carlo results for the current reference. The mean and standard deviation are 3.23nA and 56.52pA respectively, resulting in process variation (σ/μ) of 1.75%. Fig. 6(a) shows the Monte Carlo results for V_{ref} over the temperature range of -40 to 100°C, from which $\pm 3\sigma$ variation of $\pm 4.02\%$ can be observed. Similarly, from Fig. 6(b) $\pm 3\sigma$ variation of $\pm 5.25\%$ can be observed for the I_{ref} w.r.t temperature. Fig. 7(a) shows the Monte Carlo results (1000 points) for the TC of V_{ref}. The observed mean and the standard deviation are 64.55ppm/°C and 2.564ppm/°C, respectively. Similarly, Fig. 7(b) shows the Monte Carlo results (1000 points) for the TC of I_{ref}, which comes out to have a mean of 337.17ppm/°C and a standard deviation of 15.16ppm/°C. These results prove that we can avoid trimming in this architecture, considering the achieved nominal values and accuracies for both voltage and current reference.

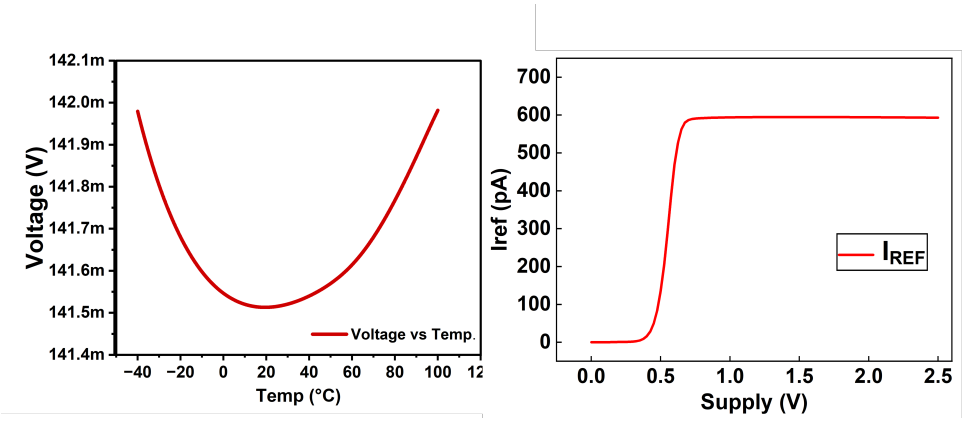

Figure 5.3: (a) V_{ref} & I_{ref} vs Temperature (b) Supply sensitivity of V_{ref} & I_{ref}

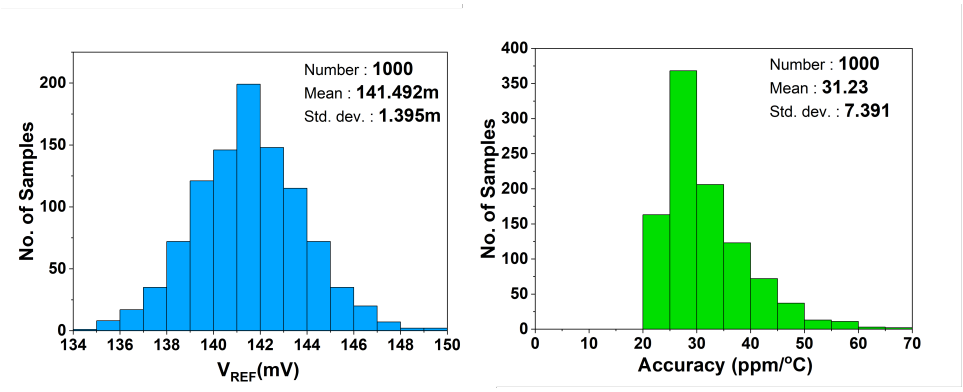

Figure 5.4: Monte Carlo results for (a) V_{ref} (b) I_{ref} value at 27°C

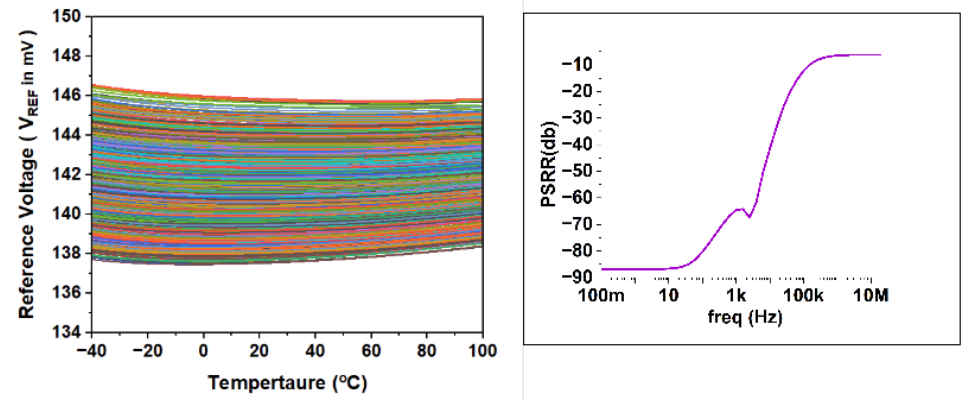

Figure 5.5: $\pm 3\sigma$ variation of (a) V_{ref} (b) I_{ref}

Table 5.1: Performance summary and comparison with other works

	This work	**[64]**	**[66]**	**[63]**	**[67]**	**[65]**	**[62]**	**[68]**
Technology(nm)	**180**	180	180	180	180	350	65	180
Type	**Vref**	Vref	Vref	Vref	Vref	Vref	Vref	Vref
V_{DD} (Supply range)	**0.6V - 2.1V**	0.85V-2.3V	0.45V-1.8V	0.8V-2.2V	0.7V-2V	1.4V-3V	0.75V-1.2V	0.85V-2.5V
Power(nW)	**14.2**	46	14.6	360	28	300	290	3300
V_{ref}(V)	**141.517mV**	0.681V	0.118V	0.489V	0.368V	0.745V	0.474V	0.221V
$\sigma/\mu(\%)$	**0.96**	2.35	0.6	0.5	-	0.94	0.9	-
Trimming used	**No**	No	Yes	Yes	Yes	No	No	No
Temperature Range(°C)	**-40 - 100**	-20 - 80	-40 - 125	-30 - 110	-40 - 125	-20 - 80	-40 - 90	20 - 120
TC (ppm/°C)	**23**	100	63.6	6.5	43.1	7	40	271
Line Sensitivity (%/V)	**0.0012**	0.02	0.12	0.076	0.027	0.002	0.2423	0.9
PSRR (db@DC)	**-48**	-75	-44.2	-75	-59	-45	-40	-
Area (mm^2)	**0.0112**	0.065	0.012	0.018	0.055	0.055	0.0198	0.0238
Resistors/Amplifiers/Thin oxide	**Not Used**	Not Used	Not Used	Used	Used	Used	Used	Used

Table 5.1 summarizes the performance of the proposed voltage reference circuit and compares it with the performance of state-of-the-art designs.

The specifications of [64] closely align with this work, with notable distinctions observed in line sensitivity, temperature coefficient (TC), and process variations—areas of primary emphasis in this work. Power consumptions of [67], [64], [66] are in the order of nano-Watts but in the remaining references mentioned, power consumption is in the order of micro Watts and the reasons are, design in [63] is implemented in saturation operation because of which current consumption is in the order of micro Amperes. Conversely, [65] proposed the idea containing bias voltage sub-circuit which consumes large current from supply contributing to high power consumption. Furthermore [68], [62] involves usage of large order P+ diffusion and poly resistors that lead to high power consumption. Designs [65] require high supply voltage(minimum of 1.4V), but the presented work requires a minimum voltage of 0.6V and does not require any external trimminig circuitry, differential or operational amplifiers. All the designs mentioned, predominantly focused on minimizing TC through various topologies, often neglecting line sensitivity. Designs in [63], [64], [65] and [67] implemented traditional beta multiplier in negative feedback. In contrast, our approach incorporates a beta multiplier with a high-swing cascode topology in negative feedback, enhancing line sensitivity from 0.02% to an impressive 0.0012%. While designs [63], [66], and [67] employ external trimming circuits to mitigate process variations, our proposed design achieves comparable invariance results (1.395mV/141.492mV) without the need for additional trimming circuitry. This underscores the robustness and efficiency of our approach in addressing key performance metrics, setting it apart from existing designs in the field. To the best of the

author's knowledge, this thesis presents a first and novel all-in-one trim-free, all-MOSFET V_{ref}/I_{ref} architecture.

5.4 Conclusion

This thesis presents a novel trim-free, low process variation, ultra-low power all CMOS voltage/current reference without using high-valued resistances, BJTs, NVT or DTMOS devices. As it does not incorporate subthreshold leakage behavior, it works over a wide temperature range of -40 to 100°C. The circuit consumes 14.2nW and works from a minimum supply of 1V over the wide supply range of 0.6V-2.1V. The proposed architecture is trim-free, as the variations of the temperature coefficients and the nominal values of both the voltage and current references are insignificant. All the above competitive specifications make it a desirable choice for various ultra-low power wearables and IoT applications.

Chapter 6

Conclusions and Future Work

This thesis has presented three innovative designs for ultra-low-power voltage and current references, each offering unique advantages and addressing specific challenges in IoT and biomedical applications.

The first design, a 37nW all-in-one trim-free voltage/current reference, demonstrates remarkable power efficiency and simplicity by eliminating the need for resistors and amplifiers. Implemented in 90nm CMOS technology, the circuit operates over a wide temperature range of -40 to 100°C. Utilizing a current-mode approach and a sub-threshold MOSFET-based voltage reference, it achieves high accuracy and stability, rendering it suitable for ultra-low-power IoT and biomedical applications. Notably, this circuit achieves a process variation of $1.34\%\sigma/\mu$ for the voltage reference and $1.75\%\sigma/\mu$ for the current reference, without requiring external trimming circuitry. These results significantly exceed the performance of current state-of-the-art solutions in terms of both power efficiency and design simplicity.

The second design, a 0.80V, 593pA trim-free duty-cycled current reference, offers a low-power solution for IoT applications requiring precise current generation. By leveraging duty-cycling techniques, this circuit achieves high accuracy while consuming minimal power, making it suitable for battery-powered devices with stringent energy requirements. The proposed design achieves a line sensitivity of 0.12% and a temperature coefficient (TC) of 378ppm/°C across a broad temperature range from -40°C to 100°C, with a power consumption of only 4nW after duty-cycling. The integration of duty cycling has emerged as a highly effective method for enhancing power efficiency while ensuring the accuracy and stability of reference current values. This work introduces the capability for active 2% duty-cycled operation through the use of transmission gate-based duty-cycling circuitry, resulting in significant improvements in power consumption. The aforementioned specifications make it a compelling choice for a wide array of ultra-low-power IoT and biomedical applications.

The third design, a 0.6V, 13nW PVT-invariant voltage reference, provides a solution for maintaining voltage stability across process, voltage, and temperature variations. This circuit achieves a remarkably low power consumption and line sensitivity, making it suitable for applications where maintaining voltage accuracy under varying conditions is essential. THe achieved specification for the above work make it suitable for ultra low power IoT and biomedical applications.

6.1 Future Works

While the designs presented in this thesis have demonstrated exceptional performance in terms of power efficiency and functionality, there are several avenues for further research and improvement.

- Process Invariant circuit : Process-Invariant Circuit: Utilizing a circuit known as a Vth extractor, we can monitor the threshold voltage of the MOSFET across process corners. This capability enables us to effectively mitigate the process variation effects attributed to Vth, minimizing their impact.
- Developing voltage and current references with a supply voltage of less than 0.4V is beneficial for applications that require lower supply voltages.

Related Publications

Accepted Publications

- **Chetan Mittal***, Arnab Dey*, Ashfakh Ali, Khanh lee and Zia Abbas "A 37nW, All-in-One Trim-free Voltage/Current Reference without using Resistors and Amplifiers,", 2023 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Phoenix, AZ, USA, 2023
*(*Equal contribution)*

- **Chetan Mittal**, Arnab Dey, Anubhab Banerjee, Ashfakh Ali, and Zia Abbas "A 0.8-V, 593-pA Trim-free Duty-cycled All CMOS Current Reference for Ultra-Low Power IoT Applications,", 37th International Conference on VLSI Design, 2024

Submitted Publication

- **Chetan Mittal**, J. Ramgopal and Zia abbas "A 0.6V, 13nW, 0.0012%/V Line Sensitivity PVT - Invariant Voltage Reference without using Resistors and Amplifiers" , 2024 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)

- Deepthi Amuru, **Chetan Mittal** and Zia Abbas "Towards Designing a Unified DNN Architecture for Analog and Mixed-Signal Circuit Characterization" IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS II), 2024

Bibliography

[1] *Global Market Size*. https://www.statista.com/statistics/254266/global-big-data-market-forecast/.

[2] K. Ueno et al. "CMOS smart sensor for monitoring the quality of perishables". In: *IEEE Journal of Solid-State Circuits* 42.4 (Apr. 2007), pp. 798–803.

[3] P. Fiorini et al. "Micropower energy scavenging". In: *Proc. of the 34th European Solid-State Circuits Conference (ESSCIRC)*. 2008, pp. 4–9.

[4] A. Wang, B. H. Clhoun, and A. P. Chandracasan. *Sub-threshold Design for Ultra Low-Power Systems*. Springer, 2006.

[5] A. P. Chandrakasan et al. "Next Generation Micropower Systems". In: *Proc. of IEEE Symposium on VLSI Circuits*. 2008, pp. 2–5.

[6] P. R. Gray and R. G. Meyer. *Analysis and Design of Analog Integrated Circuits*. 3rd ed. New York: Wiley, 1993.

[7] K. A. Bowman, S. G. Duvall, and J. D. Meindl. "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration". In: *IEEE Journal of Solid-State Circuits* 37.2 (Feb. 2002), pp. 183–190.

[8] H. Onodera. "Variability: Modeling and Its Impact on Design". In: *IEICE Transactions on Electronics* E89-C (2006), pp. 342–348.

[9] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers. "Matching properties of MOS transistors". In: *IEEE Journal of Solid-State Circuits* 24.5 (Oct. 1989), pp. 1433–1439.

[10] Y. Taur and T. H. Ning. *Fundamentals of Modern VLSI Devices*. Cambridge University Press, 2002.

[11] C.-H. Lee and H.-J. Park. “All-CMOS temperature-independent current reference”. In: *Electronics Letters* 32 (July 1996), pp. 1280–1281.

[12] I. M. Filanovsky and A. Allam. “Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits”. In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* (2001), pp. 876–884.

[13] W. M. Sansen, F. O. Eynde, and M. Steyaert. “A CMOS temperature-compensated current reference”. In: *IEEE Journal of Solid-State Circuits* 23.3 (June 1988), pp. 821–824.

[14] H. Banba et al. “A CMOS bandgap reference circuit with sub-1-V operation”. In: *IEEE Journal of Solid-State Circuits* 34.5 (May 1999), pp. 670–674.

[15] Guang Ge et al. “A Single-Trim CMOS Bandgap Reference With a 3σ Inaccuracy of $\pm 0.15\%$ From -40°C to 125°C”. In: *IEEE Journal of Solid-State Circuits* 46.11 (2011), pp. 2693–2701. DOI: 10.1109/JSSC.2011.2165235.

[16] C. M. Andreou, S. Koudounas, and J. Georgiou. “A Novel Wide-Temperature-Range, 3.9 ppm/^{o}C CMOS Bandgap Reference Circuit”. In: *IEEE Journal of Solid-State Circuits* 47.2 (2012), pp. 574–581. DOI: 10.1109/JSSC.2011.2173267.

[17] Xiao Liang Tan, Pak Kwong Chan, and Uday Dasgupta. “A Sub-1-V 65-nm MOS Threshold Monitoring-Based Voltage Reference”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 23.10 (2015), pp. 2317–2321. DOI: 10.1109/TVLSI.2014.2361766.

[18] Nashiru Alhasssan, Zekun Zhou, and Edgar Sánchez Sinencio. “An All-MOSFET Sub-1-V Voltage Reference With a —51 –dB PSR up to 60 MHz”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25.3 (2017), pp. 919–928. DOI: 10.1109/TVLSI.2016.2614438.

[19] Ken Ueno et al. “A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs”. In: *IEEE Journal of Solid-State Circuits* 44.7 (2009), pp. 2047–2054. DOI: 10.1109/JSSC.2009.2021922.

[20] Kai Yu et al. “A 23-pW NMOS-Only Voltage Reference With Optimum Body Selection for Process Compensation”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.11 (2022), pp. 4213–4217. DOI: 10.1109/TCSII.2022.3188451.

[21] Hui Wang and Patrick P. Mercier. “A 420 fW self-regulated 3T voltage reference generator achieving 0.47%/V line regulation from 0.4-to-1.2 V”. In: *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*. 2017, pp. 15–18. DOI: 10.1109/ESSCIRC.2017.8094514.

[22] Junghyup Lee and SeongHwan Cho. “A 1.4-µW 24.9-ppm/°C Current Reference With Process-Insensitive Temperature Compensation in 0.18-µm CMOS”. In: *IEEE Journal of Solid-State Circuits* 47.10 (2012), pp. 2527–2533. DOI: 10.1109/JSSC.2012.2204475.

[23] Arpan Jain et al. “A High PSRR, Stable CMOS Current Reference using Process Insensitive TC of Resistance for Wide Temperature Applications”. In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2019, pp. 1–5. DOI: 10.1109/ISCAS.2019.8702638.

[24] Tetsuya Hirose et al. “A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities”. In: *2010 Proceedings of ESSCIRC*. 2010, pp. 114–117. DOI: 10.1109/ESSCIRC.2010.5619819.

[25] Samriddhi Agarwal, Ashutosh Pathy, and Zia Abbas. “A 9.5nW, 0.55V Supply, CMOS Current Reference for Low Power Biomedical Applications”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.9 (2022), pp. 3650–3654. DOI: 10.1109/TCSII.2022.3183146.

[26] Nishant Maurya and Nijwm Wary. “Design and Analysis of PVT Invariant Current Reference in 65-nm CMOS”. In: *2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2022, pp. 1–4. DOI: 10.1109/MWSCAS54063.2022.9859372.

[27] H.J. Oguey and D. Aebischer. “CMOS current reference without resistance”. In: *IEEE Journal of Solid-State Circuits* 32.7 (1997), pp. 1132–1135. DOI: 10.1109/4.597305.

[28] Ashfakh Ali et al. “A Sub-nW, 8T Current Reference Consuming Constant Power w.r.t Process Temperature”. In: *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2020, pp. 730–733. DOI: 10.1109/MWSCAS48704.2020.9184679.

[29] Hui Wang and Patrick P. Mercier. “A 14.5 pW, 31 ppm/°C resistor-less 5 pA current reference employing a self-regulated push-pull voltage reference generator”. In: *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2016, pp. 1290–1293. DOI: 10.1109/ISCAS.2016.7527484.

[30] Dongwoo Lee, D. Blaauw, and D. Sylvester. “Gate oxide leakage current analysis and reduction for VLSI circuits”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 12.2 (2004), pp. 155–166. DOI: 10.1109/TVLSI.2003.821553.

[31] Lidan Wang and Chenchang Zhan. “A 0.7-V 28-nW CMOS Subthreshold Voltage and Current Reference in One Simple Circuit”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 66.9 (2019), pp. 3457–3466. DOI: 10.1109/TCSI.2019.2927240.

[32] Wenbin Huang, Lianxi Liu, and Zhangming Zhu. “A Sub-200nW All-in-One Bandgap Voltage and Current Reference Without Amplifiers”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 68.1 (2021), pp. 121–125. DOI: 10.1109/TCSII.2020.3007195.

[33] Abhishek Pullela et al. “A 156pW Gate-Leakage Based Voltage/Current Reference for Low-Power IoT Systems”. In: *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2022, pp. 1923–1927. DOI: 10.1109/ISCAS48785.2022.9937316.

[34] Lidan Wang et al. “A 0.9-V 33.7-ppm/°C 85-nW Sub-Bandgap Voltage Reference Consisting of Subthreshold MOSFETs and Single BJT”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 26.10 (2018), pp. 2190–2194. DOI: 10.1109/TVLSI.2018.2836331.

[35] Yuji Osaki et al. “1.2-V Supply, 100-nW, 1.09-V Bandgap and 0.7-V Supply, 52.5-nW, 0.55-V Subbandgap Reference Circuits for Nanowatt CMOS LSIs”. In: *IEEE Journal of Solid-State Circuits* 48.6 (2013), pp. 1530–1538. DOI: 10.1109/JSSC.2013.2252523.

[36] Alice Wang, Benton H Calhoun, and Anantha P Chandrakasan. *Sub-threshold design for ultra low-power systems*. Vol. 95. Springer, 2006.

[37] Junghyup Lee and SeongHwan Cho. “A 1.4-µW 24.9-ppm/°C Current Reference With Process-Insensitive Temperature Compensation in 0.18-µm CMOS”. In: *IEEE Journal of Solid-State Circuits* 47.10 (2012), pp. 2527–2533. DOI: 10.1109/JSSC.2012.2204475.

[38] Arpan Jain et al. “A High PSRR, Stable CMOS Current Reference using Process Insensitive TC of Resistance for Wide Temperature Applications”. In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2019, pp. 1–5. DOI: 10.1109/ISCAS.2019.8702638.

[39] Battu Balaji Yadav et al. “67ppm/°C, 66nA PVT Invariant Curvature Compensated Current Reference for Ultra-Low Power Applications”. In: *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2020, pp. 1–5. DOI: 10.1109/ISCAS45731.2020.9180857.

[40] Shailesh Singh Chouhan and Kari Halonen. "A 0.67- μW 177-ppm/°C All-MOS Current Reference Circuit in a 0.18- μm CMOS Technology". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 63.8 (2016), pp. 723–727. DOI: 10.1109/TCSII.2016.2531158.

[41] Samriddhi Agarwal, Ashutosh Pathy, and Zia Abbas. "A 9.5nW, 0.55V Supply, CMOS Current Reference for Low Power Biomedical Applications". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.9 (2022), pp. 3650–3654. DOI: 10.1109/TCSII.2022.3183146.

[42] Qing Dong et al. "A 1.02nW PMOS-only, trim-free current reference with 282ppm/°C from 40°C to 120°C and 1.6 within-wafer inaccuracy". In: *ESSCIRC 2017 - 43rd IEEE European Solid-State Circuits Conference*. 2017, pp. 19–22. DOI: 10.1109/ESSCIRC.2017.8094515.

[43] Ahmed Reda Mohamed, Mingyi Chen, and Guoxing Wang. "Untrimmed CMOS Nano-Ampere Current Reference with Curvature-Compensation Scheme". In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2019, pp. 1–4. DOI: 10.1109/ISCAS.2019.8702293.

[44] Dipesh C. Monga and Kari Halonen. "A Compact Untrimmed 48ppm/°C All MOS Current Reference Circuit". In: *2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2022, pp. 1–5. DOI: 10.1109/MWSCAS54063.2022.9859347.

[45] Nishant Maurya and Nijwm Wary. "Design and Analysis of PVT Invariant Current Reference in 65-nm CMOS". In: *2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2022, pp. 1–4. DOI: 10.1109/MWSCAS54063.2022.9859372.

[46] Tetsuya Hirose et al. "A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities". In: *2010 Proceedings of ESSCIRC*. 2010, pp. 114–117. DOI: 10.1109/ESSCIRC.2010.5619819.

[47] Indranil Bhattacharjee and Gajendranath Chowdary. "A 0.7-V, 192 pA Current Reference with 0.51/V Line Regulation for Ultra-Low Power Applications". In: *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2020, pp. 1–5. DOI: 10.1109/ISCAS45731.2020.9180858.

[48] Myungjoon Choi et al. "A 23pW, 780ppm/°C resistor-less current reference using subthreshold MOSFETs". In: *ESSCIRC 2014 - 40th European Solid-State Circuits Conference (ESSCIRC)*. 2014, pp. 119–122. DOI: 10.1109/ESSCIRC.2014.6942036.

[49] Ashfakh Ali et al. “A Sub-nW, 8T Current Reference Consuming Constant Power w.r.t Process Temperature”. In: *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2020, pp. 730–733. DOI: 10.1109/MWSCAS48704.2020.9184679.

[50] Hui Wang and Patrick P. Mercier. “A 14.5 pW, 31 ppm/°C resistor-less 5 pA current reference employing a self-regulated push-pull voltage reference generator”. In: *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2016, pp. 1290–1293. DOI: 10.1109/ISCAS.2016.7527484.

[51] Dongwoo Lee, D. Blaauw, and D. Sylvester. “Gate oxide leakage current analysis and reduction for VLSI circuits”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 12.2 (2004), pp. 155–166. DOI: 10.1109/TVLSI.2003.821553.

[52] H.J. Oguey and D. Aebischer. “CMOS current reference without resistance”. In: *IEEE Journal of Solid-State Circuits* 32.7 (1997), pp. 1132–1135. DOI: 10.1109/4.597305.

[53] Ken Ueno et al. “A 300 nW, 7 ppm/°C CMOS voltage reference circuit based on subthreshold MOSFETs”. In: *2009 Asia and South Pacific Design Automation Conference*. 2009, pp. 95–96. DOI: 10.1109/ASPDAC.2009.4796449.

[54] Bhartipudi Sahishnavi et al. “A 0.5V, pico-watt, 0.06/V / 0.03/V low supply sensitive current/voltage reference without using amplifiers and resistors”. In: *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2023, pp. 1–5. DOI: 10.1109/ISCAS46773.2023.10181479.

[55] Maoqiang Liu et al. “A106nW 10 b 80 kS/s SAR ADC With Duty-Cycled Reference Generation in 65 nm CMOS”. In: *IEEE Journal of Solid-State Circuits* 51.10 (2016), pp. 2435–2445. DOI: 10.1109/JSSC.2016.2587688.

[56] Phillip M. Nadeau, Arun Paidimarri, and Anantha P. Chandrakasan. “Ultra Low-Energy Relaxation Oscillator With 230 fJ/cycle Efficiency”. In: *IEEE Journal of Solid-State Circuits* 51.4 (2016), pp. 789–799. DOI: 10.1109/JSSC.2016.2521886.

[57] Youngwoo Ji et al. “A Second-Order Temperature-Compensated On-Chip R-RC Oscillator Achieving 7.93ppm/°C and 3.3pJ/Hz in -40°C to 125°C Temperature Range”. In: *2022 IEEE International Solid- State Circuits Conference (ISSCC)*. Vol. 65. 2022, pp. 1–3. DOI: 10.1109/ISSCC42614.2022.9731730.

[58] Bo Wang, Man-Kay Law, and Amine Bermak. "A BJT-Based CMOS Temperature Sensor Achieving an Inaccuracy of $\pm 0.45°C(3\sigma)$ from -50°C to 180°C and a Resolution-FoM of 7.2pJ.K2 at 150°C". In: *2022 IEEE International Solid- State Circuits Conference (ISSCC)*. Vol. 65. 2022, pp. 72–74. DOI: 10.1109/ISSCC42614.2022.9731647.

[59] Karel E Kuijk. "A precision reference voltage source". In: *IEEE Journal of Solid-State Circuits* 8.3 (1973), pp. 222–226.

[60] Philip KT Mok and Ka Nang Leung. "Design considerations of recent advanced low-voltage low-temperature-coefficient CMOS bandgap voltage reference". In: *Proceedings of the IEEE 2004 Custom Integrated Circuits Conference (IEEE Cat. No. 04CH37571)*. IEEE. 2004, pp. 635–642.

[61] Ka Nang Leung and Philip KT Mok. "A CMOS voltage reference based on weighted ΔV/sub GS/for CMOS low-dropout linear regulators". In: *IEEE Journal of Solid-State Circuits* 38.1 (2003), pp. 146–150.

[62] Xiao Liang Tan, Pak Kwong Chan, and Uday Dasgupta. "A sub-1-V 65-nm MOS threshold monitoring-based voltage reference". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 23.10 (2014), pp. 2317–2321.

[63] Nashiru Alhasssan, Zekun Zhou, and Edgar Sánchez Sinencio. "An all-MOSFET sub-1-V voltage reference with a—51–dB PSR up to 60 MHz". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25.3 (2016), pp. 919–928.

[64] Ashutosh Pathy, Banthi Adithya, and Zia Abbas. "A 0.85 V Supply, High PSRR CMOS Voltage Reference without Resistor and Amplifier for Ultra-Low Power Applications". In: (2021), pp. 995–998.

[65] Ken Ueno et al. "A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs". In: *IEEE Journal of Solid-State Circuits* 44.7 (2009), pp. 2047–2054. DOI: 10.1109/JSSC.2009.2021922.

[66] Yutao Wang et al. "A 0.45-V, 14.6-nW CMOS subthreshold voltage reference with no resistors and no BJTs". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 62.7 (2015), pp. 621–625.

[67] Lidan Wang and Chenchang Zhan. “A 0.7-V 28-nW CMOS Subthreshold Voltage and Current Reference in One Simple Circuit”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 66.9 (2019), pp. 3457–3466. DOI: 10.1109/TCSI.2019.2927240.

[68] P-H Huang, Hongchin Lin, and Y-T Lin. “A simple subthreshold CMOS voltage reference circuit with channel-length modulation compensation”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 53.9 (2006), pp. 882–885.