Low Supply Voltage, Low Quiescent Current, High PSRR Reference Current And Reference Voltage Generation Circuits for Low Power Applications

Thesis submitted in partial fulfillment
of the requirements for the degree of

Master of Science
In

Electronics and Communication Engineering
by Research

Ashutosh Pathy

2019702007

Ashutosh.pathy@research.iiit.ac.in

International Institute of Information Technology
Hyderabad - 500 032, INDIA

MAY-2024

International Institute of Information Technology
Hyderabad, India

CERTIFICATE

It is certified that the work contained in this thesis, titled "Low Supply Voltage, Low Quiescent Current, High PSRR Reference Current and Reference Voltage generation Circuits for Low Power Applications" by Ashutosh Pathy, has been carried out under my supervision and is not submitted elsewhere for a degree.

Date

Advisor: Dr. Zia Abbas

To my Beloved Parents, Grandmother and Brother

Acknowledgements

I acknowledge that the knowledge I gained from my advisor Dr. Zia Abbas is invaluable. I am grateful beyond words for his constant support through-out my MS journey. I will recollect and cherish the experience I had under his guidance for the rest of my life. I thank him from the bottom of my heart for believing in me.

I wish to thank my family for their unconditional support. Their sacrifices are the main reason why I am in a position to write this thesis.

Abstract

This thesis focuses on designing voltage and current reference circuits keeping high PSRR, low IQ and low supply voltage operation in mind. These circuits are one of the most critical blocks of a power management IC as they bias the LDOs and oscillators in any system. High PSRR makes the reference robust to noise at the supply. Low IQ enables the reference to operate in an energy harvesting system. Low supply voltage operation enables the reference to act as a voltage reference for crude power-on-reset comparator. Negative feedback arrangements are put to use to get good PSRR, subthreshold operation of MOSFETs is chosen to generate low bias current and low supply voltage. Although CMOS voltage and current references have great area and IQ specifications but they struggle when it comes to having good accuracy. Therefore, a hybrid voltage reference consisting of BJTs and MOSFETs is also proposed to improve the accuracy of the published voltage reference. Furthermore, having 2 different circuits for generating a reference voltage and a reference current can result in area overhead. Therefore, a 2-in-1 voltage + current reference circuit is also presented in this thesis.

CONTENTS

List of Figures

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

In the past decade the demand for low power analog circuits have increased many folds due to rise in the usage of Internet of Things (IoT) devices which generally work with low power. It is forecasted that by the year 2030 there will be over 30 billion IoT devices in use. IoT devices are often powered by energy harvesters. Solar energy, piezoelectric energy and thermal energy are some of the forms of energy which can be harvested. The energy harvester stores such energy in a rechargeable battery and provides a small amount of energy for low power applications. This creates a huge opportunity for analog designers to contribute in the field of low power IC design.

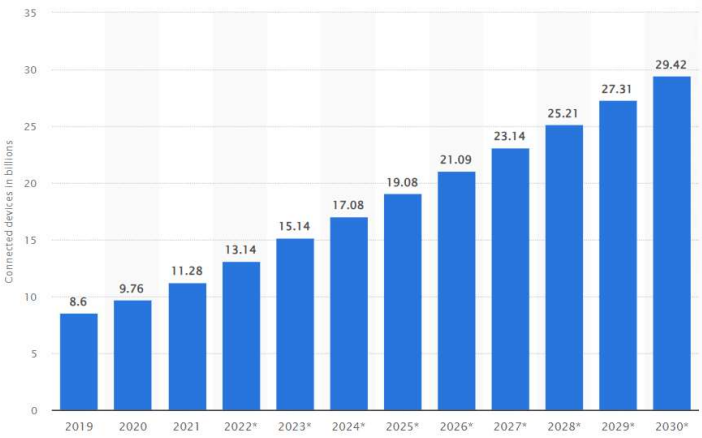

Fig. 1.1. Projected market for IoT devices vs Year (Source: www.statista.com)

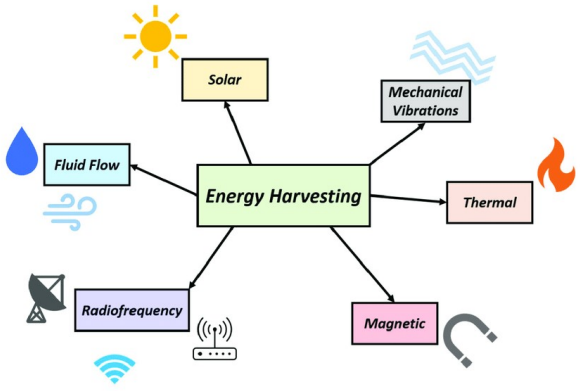

Fig. 1.2. Forms of energy that can be harvested [1]

The analog components used in these IoT devices consume nano-amps of quiescent current and often work with sub 1V of supply voltage for limiting the power consumption. Furthermore, a duty cycling technique is used in which the active mode is short-term and sleep more is long term. However, certain analog components like current reference, voltage reference, sub-regulator etc must work in both active mode and sleep mode with good accuracy.

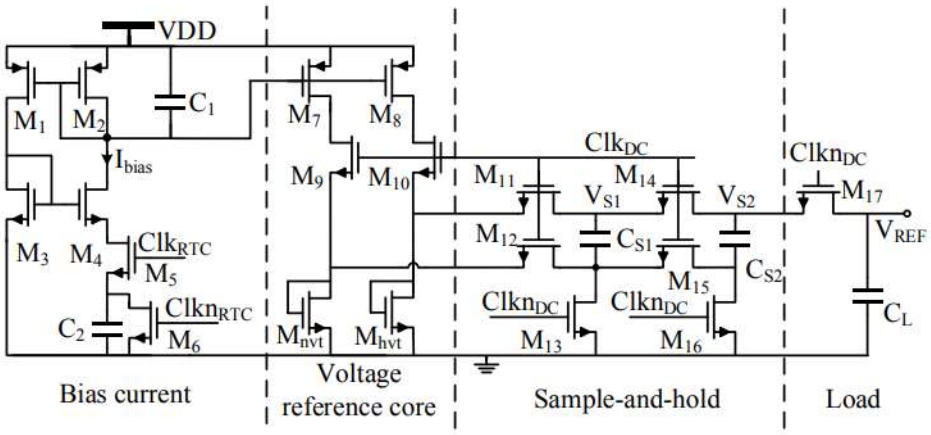

Fig. 1.3. Example circuit of a duty cycled voltage reference [2]

The controllers used in DC-DC converters like flyback often use a resistor-capacitor based charging for powering up the Internal Voltage (VINT) block in the start-up process. The value of the resistor is kept rather high to limit the start-up current of the controller. The quiescent current of the VINT is limited to few micro-amps to make the start-up process faster. A stable, PVT invariant voltage reference is one of the most critical analog blocks present inside the VINT block. This voltage reference signal is used to detect the Under-Voltage-Lock-Out (UVLO) and Power-on-Reset (POR) thresholds of the controller. Therefore, a sub micro-amp, highly accurate voltage reference is required for fast controller start-up and accurate UVLO/POR threshold detection.

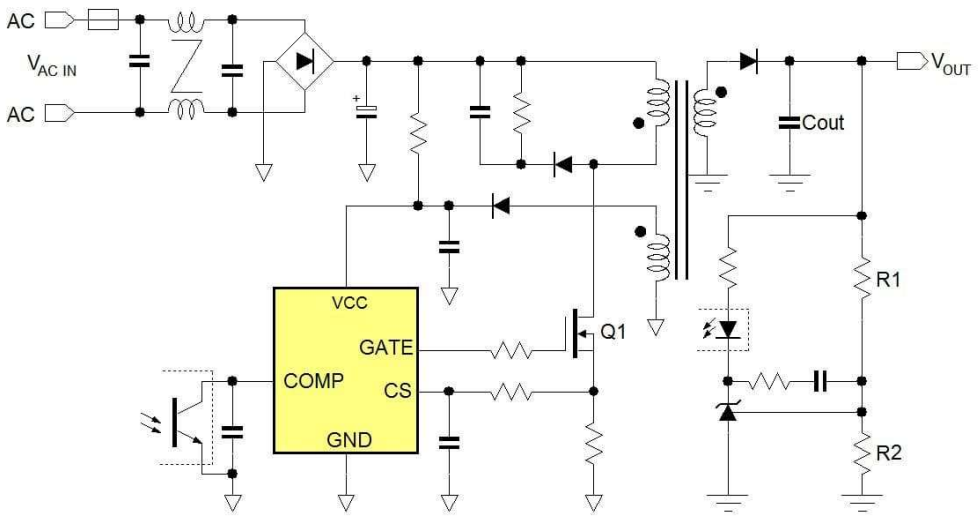

Fig. 1.4. An RC start-up based flyback controller (source: Richtek.com)

Limiting the quiescent current of an analog block increases the on-chip area. Therefore, it becomes a challenge for analog designers to keep both area and quiescent current specification in mind before designing any circuit. Going with smaller technologies for area optimization is not always the best way to design a circuit as accuracy is compromised. Therefore, the designer often tries to design his/her circuit without high area consuming components like capacitors. resistors, amplifiers. Furthermore, lowering the operating supply voltage to sub 1V enables the designer to use smaller MOSFETs.

All three factors, Low quiescent current, sub 1V operation and low area are kept in mind in designing the reference circuits presented in this thesis. A sub 1V CMOS only voltage reference, a 9.5nW current reference are presented. Furthermore, a hybrid circuit consisting of a current reference and a voltage reference is presented in this thesis.

1.2 WHAT IS A VOLTAGE REFERENCE?

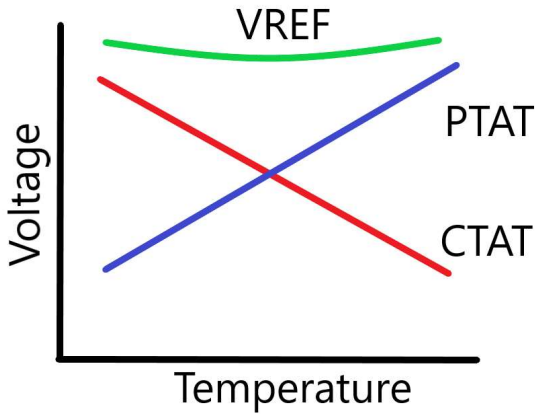

Fig. 1.5. Reference voltage generated using PTAT and CTAT reference voltages

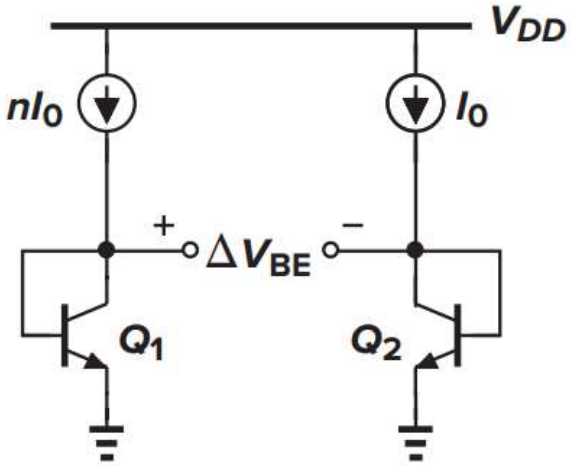

Fig. 1.6. Generation of PTAT voltage

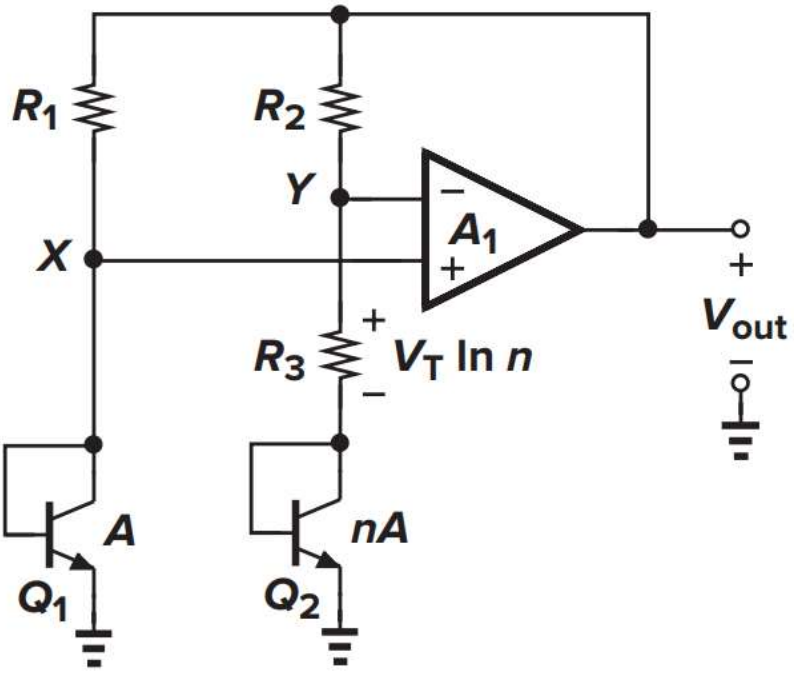

Fig. 1.7. Circuit level implementation of a Bandgap reference (uses BJTs, OP-AMP and resistors)

A voltage reference is a widely used analog circuit which provides a constant (DC) voltage across temperature, process and a wide range of supply voltages. A constant voltage finds many uses in analog circuits. It can be used to (a) define the common mode levels in op-amps (b) define the LDO's output voltage (c) detect supply (VCC) thresholds for UVLO/POR detection (d) generate a reference current etc.

To generate a quantity which is constant with temperature, two different voltage quantities (V_{PTAT} and V_{CTAT}) which have opposite behaviour with temperature are added proportionately. For example, $VREF = \alpha_1 V_{PTAT} + \alpha_2 V_{CTAT}$. Where, VREF is the required reference voltage; V_{CTAT} is generated such that is it complementary to temperature; V_{PTAT} is generated such that it is proportional to temperature. Therefore, a temperature independent voltage VREF is generated. Among various device parameters present in semiconductor technologies, bipolar transistors are considered ideal to generate V_{PTAT} and V_{CTAT}. The forward voltage drop of base-emitter junction of a BJT gives a rather process invariant CTAT voltage. The temperature coefficient of the VBE is approximately equal to -1.5mV/K and the nominal value of VBE is approximately 700mV. To generate V_{PTAT}, the difference of VBE (ΔVBE) of two differently sized BJTs (1: n) is considered. Therefore, the constant voltage generated by using bipolar devices can be mathematically written as: (Fig. 1.7.)

$$VREF = VBE + \Delta VBE$$

$$= VBE + V_T \ln (n)$$

To generate a voltage which is invariant to the changes in the supply, a supply invariant current is generated with a circuit which is self-biased. The bipolar devices are biased with this supply invariant current. Specifications like temperature coefficient of the reference voltage, ability of the circuit to reject the noise at supply (PSRR), quiescent current, minimum supply voltage, area consumption are judged to evaluate the performance of a voltage reference circuit.

Temperature Coefficient: It is defined as the measure of change in the reference voltage over a temperature range. Mathematically, it can be defined as:

$$\text{TC} = \frac{VREF_{max} - VREF_{min}}{VREF_{nom} * \text{Temperature Range}} * 10^6$$

PSRR (Power Supply Rejection Ratio): PSRR is the ability of the circuit to stay immune to the noise present at the supply. Mathematically, it's the ratio of change in VREF to change in supply. It's defined in dB.

Minimum Supply Voltage: Nano-watt application require sub-1V operation of the voltage reference. Therefore, voltage reference circuits which are used for nano-watt application operate with supply voltage <1V.

Quiescent Current (IQ): IQ is the total steady state current consumed by the voltage reference.

1.3 EVOLUTION OF VOLTAGE REFERENCE (BIPOLAR TO CMOS)

The Brokaw's bandgap reference is one of the oldest and still widely used bandgap structures (fig. 1.8.). The original structure uses only bipolar transistors and resistors to generate the reference voltage. Subsequently, several adaptations of the Brokaw have been published (Fig.1.9 and Fig. 1.10) The primary advantage of the Brokaw is that it does not require any extra op-amp and the reference voltage is taken from a high impedance node. The high impedance node allows the architecture to be extended into a current reference as well.

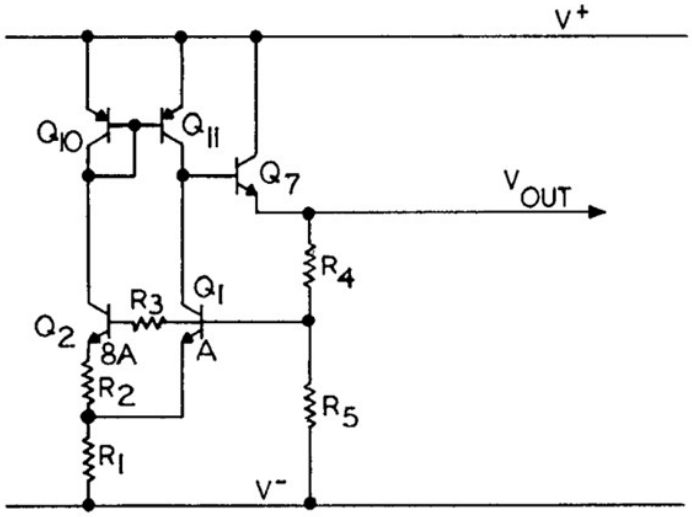

Fig. 1.8. A Brokaw Bandgap Reference [3]

The use of op-amp in bandgap reference circuit is avoided as much as possible to eliminate the DC offset errors [4]. Although, use of op-amp becomes rather necessary for designing sub 1V bandgap references [5]. Several bandgap structures use PNP bipolar transistors instead of NPN (Fig. 11-12]. PNP or NPN bipolar transistor-based architectures are chosen based on their availability in the foundry.

Although, use of bipolar devices give best results accuracy wise, it does have its drawbacks. Firstly, bipolar devices take significantly larger area than MOSFETs. Secondly, the quiescent current of bandgap reference circuits is rather large compared to that of CMOS voltage reference circuits. These factors make the traditional BJT based bandgap reference futile for IoT/low power applications where

area and quiescent current take precedence over accuracy. Although, research is on-going for improving the accuracy of modern-day CMOS voltage reference circuits.

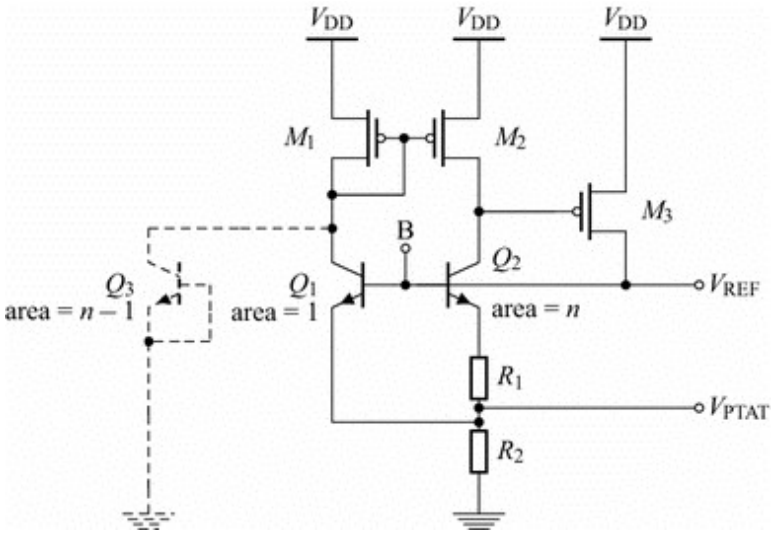

Fig. 1.9. Modified Brokaw Bandgap reference without PNP BJTs [6]

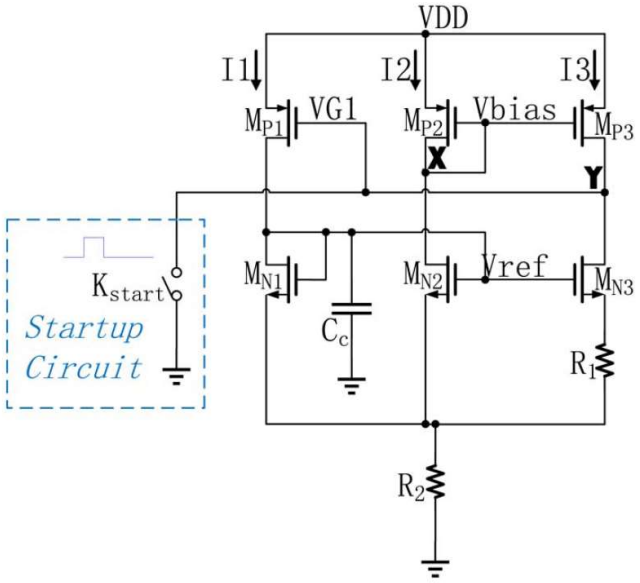

Fig. 1.10. Modified Brokaw Bandgap reference without using BJT [7]

Recently, many papers have been published on CMOS voltage reference circuits which operate with nano-amps of current [8-16]. All these papers operate the MOSFETs in subthreshold region instead of operating the MOSFET in saturation region. Reason being, it is possible to make the MOSFET behave as a BJT when it is biased in subthreshold region.

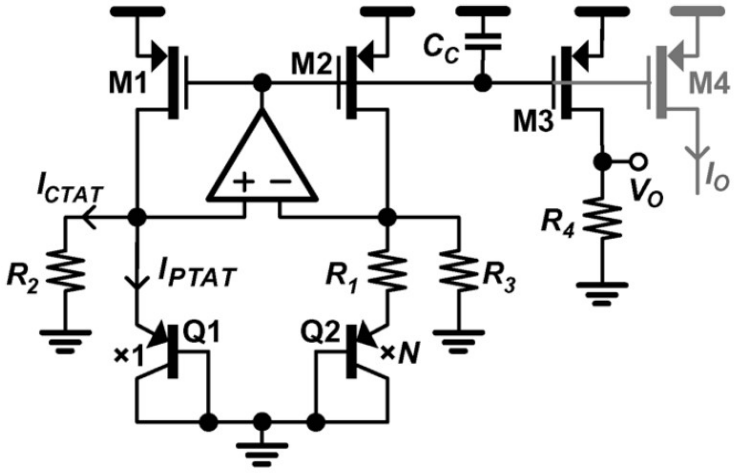

Fig. 1.11. An op-amp based BGR for sub 1V application

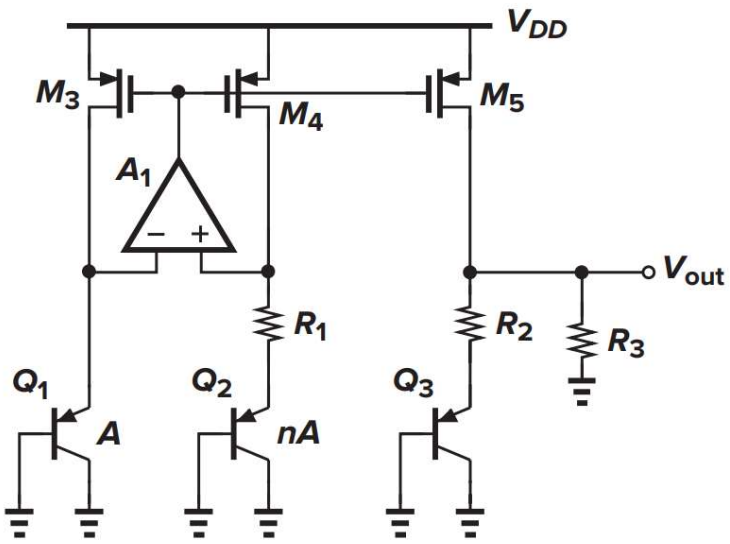

Fig. 1.12. An alternate way to design a sub-1V voltage reference

ΔVBE characteristics of bipolar can be emulated by ΔVGS characteristics of two MOSFETs operating in subthreshold region. Where, ΔVGS is the difference of gate-source voltage of two MOSFETs operating in subthreshold region. This has given rise to a whole new range of voltage reference architectures that operate with nano-watts to pico-watts of power consumption. The Brokaw which used resistors and BJTs operated with micro-amps of current and consumed a lot of area but it could give a 6-sigma accuracy of 2% for the reference voltage. Modern day CMOS voltage reference circuits can operate with few nano-amps of current and consume a fraction of on-chip area which was consumed by the Brokaw for approximately 20% 6-sigma accuracy for the reference voltage. Therefore, trimming arrangements are necessary for CMOS voltage references. Although several papers have been published on pico-watt voltage references (Fig. 1.13) [17-20], its usage is not always possible since the leakage currents are not always well modelled in many technologies.

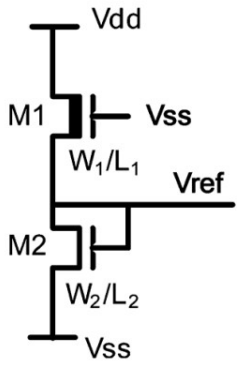

Fig. 1.13. A 2-Transistor, pico-watt voltage reference [17]

1.4 PERFORMANCE REVIEW OF EXISTING CMOS VOLTAGE REFERENCES

As for the previously designed CVRs, [8-10] have used an amplifier to improve the PSRR. The amplifier demands excessive current from the supply; therefore, the voltage reference circuits with amplifier are more power-hungry. Guo *et al* [11] have stacked MOSFETs to ameliorate the line sensitivity of the reference voltage. Such technique compels the designer to go for a higher supply voltage (> 1V). Wang *et al* [12] have used a resistor to generate a temperature and supply independent current but a large resistor is used to scale the current to nA range. Huang *et al* [13] have used different *Vth* NMOS transistors. This requires an additional fabrication mask which results in extra manufacturing cost. Parisi *et al* [14] have used a loop to generate supply independent current but the circuit suffers from poor line sensitivity of 2%/V. Zhou *et al* [15] have achieved an excellent PSRR of 75 dB at DC without using any amplifier but the design uses BJTs which makes it power inefficient.

1.5 OP-AMP FREE VOLTAGE REFERENCE CIRCUITS

As for Recently, various types of op-amp free voltage reference circuits have been published (Fig. 14-16). The primary advantage of eliminating the op-amp is that it eliminates the offset introduced by the op-amp. Also, removing the op-amp makes circuit power and area efficient.

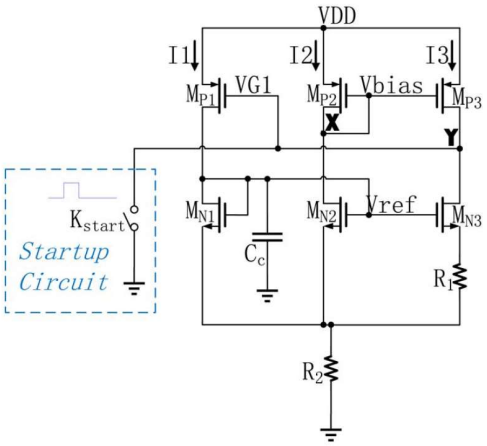

Fig. 1.14. OP-AMP free, negative feedback-based voltage reference implementation [7]

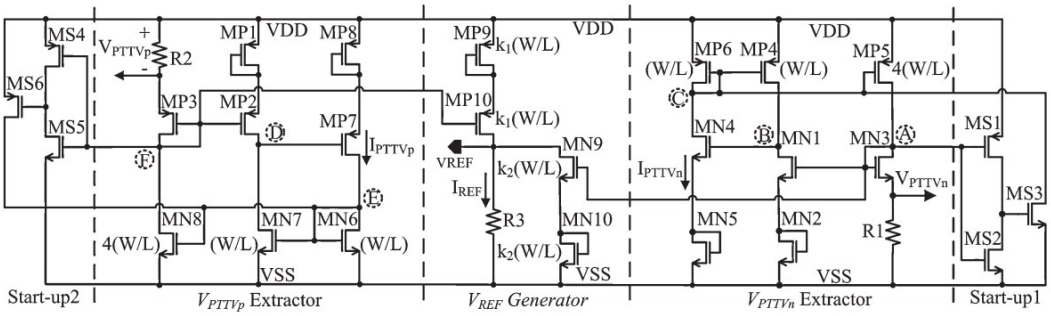

Fig. 1.15. OP-AMP free, negative feedback-based voltage reference implementation [21]

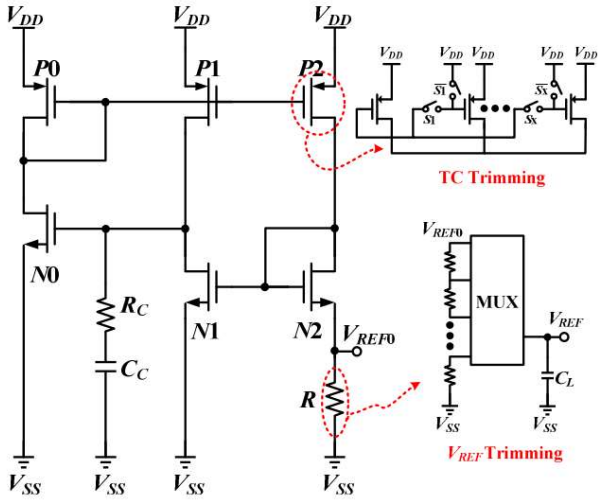

Fig. 1.16. OP-AMP free, negative feedback-based voltage reference implementation [22]

Although, the recent works on op-amp free voltage reference deliver reasonable performance, they use BJTs, resistors. These components consume a significant power on the chip which defeats the purpose of not using an op-amp.

1.6 WHAT IS A CURRENT REFERENCE?

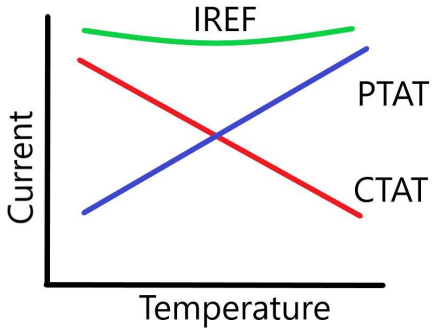

Fig. 1.17. Reference Current Generated using PTAT and CTAT Reference Currents

A current reference is a widely used analog circuit which either sources or sinks a constant (DC) current to bias subsequent modules on the chip like amplifiers, voltage references, regulators, oscillators etc. Current reference finds its application in oscillators as well where the reference current is used to

charge the capacitor in a relaxation oscillator. Essentially, the reference current needs to be (a) supply voltage independent (b) temperature independent (c) process independent.

Although, it is possible to generate a sinking current with an arrangement as shown in Fig. 1.18. But the generated current will vary with changes in the supply. Therefore, for a supply independent current generation, it is ensured that the circuit must bias itself. The goal is to ensure, IREF is independent of VDD. This kind of circuits are known as self-biased circuits (Fig. 1.19).

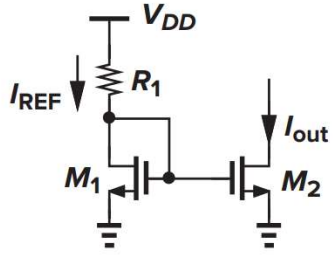

Fig. 1.18. A crude current reference circuit

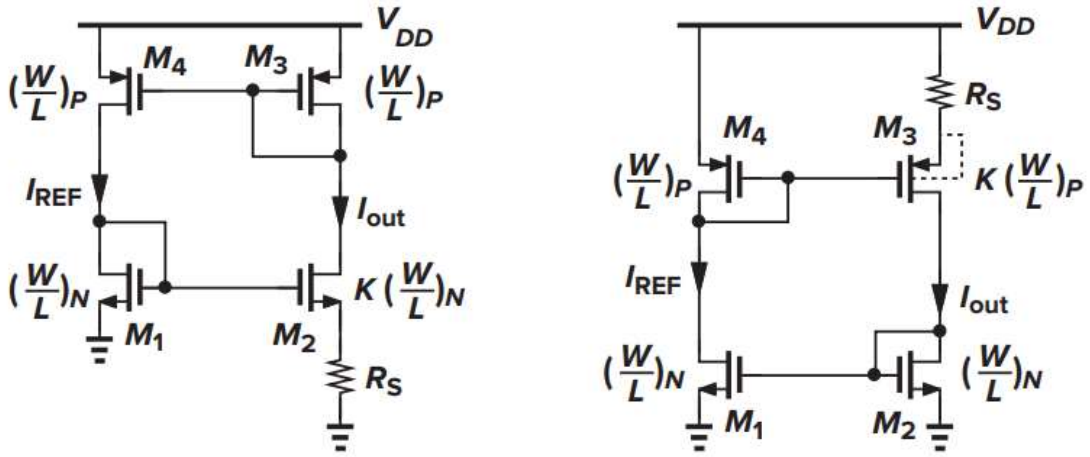

Fig. 1.19. Self-Biased current source example circuits

1.7 EVOLUTION OF CURRENT REFERENCE

Traditionally, there are 4 different types of current references: (1) ΔVBE based current reference [23-26] (2) Beta-multiplier based current reference [27-31] (3) Zero Temperature coefficient (ZTC) based current reference [32-34] (4) Division based current reference [35-40].

In ΔVBE based current reference, the PTAT current is generated by dropping ΔVBE across a resistor (Fig. 1.20.). The CTAT current is generated by dropping VBE across a resistor. The PTAT and CTAT currents are added proportionately to generate a reference current. Such architecture has similar drawbacks as the bandgap reference. That is, it consumes large area and quiescent current. A large resistor, often 10s of Mega-Ohms is required to limit the CTAT current to nano-amps.

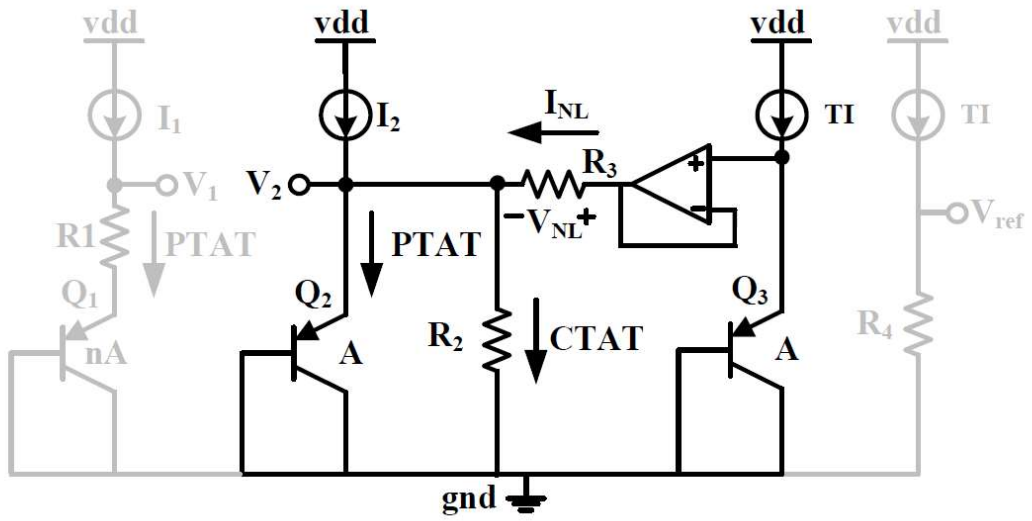

Fig. 1.20. PTAT current generation using ΔVBE and CTAT current generation using VBE

Beta-multiplier based current reference circuits (Fig. 1.21.) operate the MOSFETs in subthreshold region. In such circuits, the ΔVBE characteristics of NPN or PNP is emulated by the NMOS or PMOS in subthreshold to generate ΔVGS. The generated PTAT voltage (ΔVGS) is dropped across a resistor to generate a PTAT current. The CTAT current is generated by dropping VGS across a resistor and the reference current is generated by adding the PTAT and CTAT current proportionately. This method has two major disadvantages. Firstly, the CTAT voltage varies significantly with process. Secondly, a large resistor (in the order of 10s of Mega-Ohms) is required to limit the CTAT current to nano-amps.

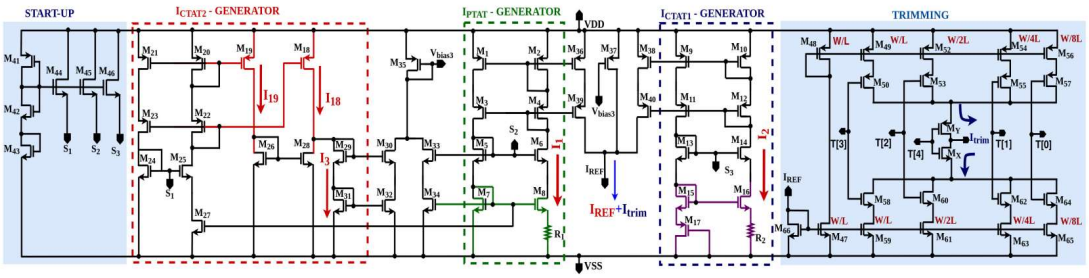

Fig. 1.21. PTAT current generation using ΔVGS and CTAT current generation using VGS [41]

In ZTC based current reference (Fig. 1.22.), the gate voltage of a source follower NMOS is biased such that the drain current of the NMOS has minimum variation with respect to temperature. This method also has 2 drawbacks. The process variation in the generated reference current is rather large. Also, a large length has to be chosen for the source-follower NMOS to limit the reference current. Finally, reference current can be reliably generated by dropping a constant voltage across a constant (Fig. 1.23). The resistor used is rather large to limit the reference current to the order of nano-amps.

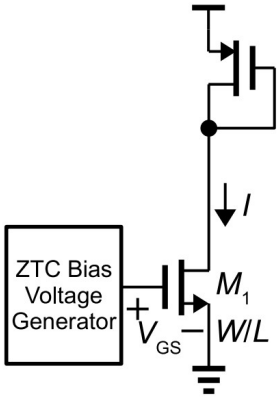

Fig .1.22. ZTC based current reference

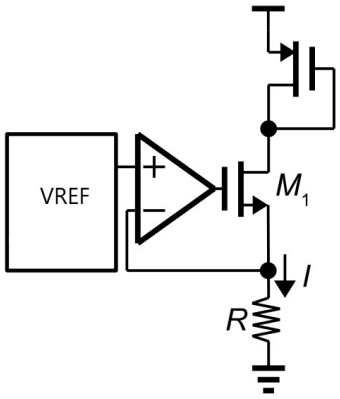

Fig 1.23. VREF/R based current reference

1.8 PERFORMANCE REVIEW OF EXISTING CURRENT REFERENCES

The most recently reported current reference uses the sum of CTAT and PTAT currents [41], [42], [43]. For instance, design introduced in [41] used curvature compensated technique to achieve low TC, but the power consumption and minimum supply voltage are considerably high (>1V). Authors in [44] proposed a resistor-less CMOS current reference but has a poor TC. Authors in [32] proposed zero temperature coefficient (ZTC) biasing to generate temperature compensated current reference but has a limited minimum supply voltage (>1.5V), and the line regulation is also influenced due to second-order effects. One of the possible designs for current reference circuits is based on peaking current source [45]. Authors in [46] proposed a modification in the conventional peaking current source for temperature compensation by adding an n-well resistor but has a poor TC and the line regulation which is unacceptable in some applications due to short channel effects. in [35] process insensitive temperature compensation is achieved by taking the ratio of compensated voltage and on-chip resistance, but at the cost of higher supply voltage and power consumption.

1.9 SUB-BANDGAP REFERENCE

Traditional Bandgap reference circuits (BGR) use BJTs and resistors for providing a constant voltage with +/- 2% six sigma trim-free accuracy. Despite their excellent accuracy, these BGR circuits have the following disadvantages:

1. The power consumption is rather large (in 10s of micro-watts).
2. The use of 1:8 BJTs (9 BJTs) for the PTAT current generation takes up significant on-chip area.
3. They tend to require an op-amp to achieve proper operation at low supply voltage.
4. The op-amp takes up extra on-chip area and quiescent current.
5. Furthermore, it adds inaccuracy to the reference voltage due to its DC offset.

Existing CMOS based voltage references (which use threshold voltage of a MOSFET for CTAT voltage generation) are highly inaccurate (+/- 20% six sigma trim-free accuracy) due to the process variations in the threshold voltage. These voltage references are still widely used for low area applications.

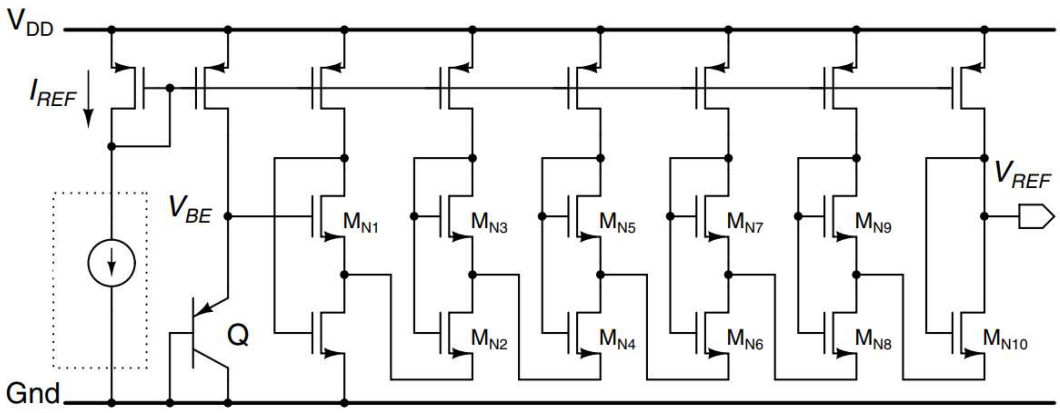

Fig. 1.24. A sub-BGR architecture as published in [47]

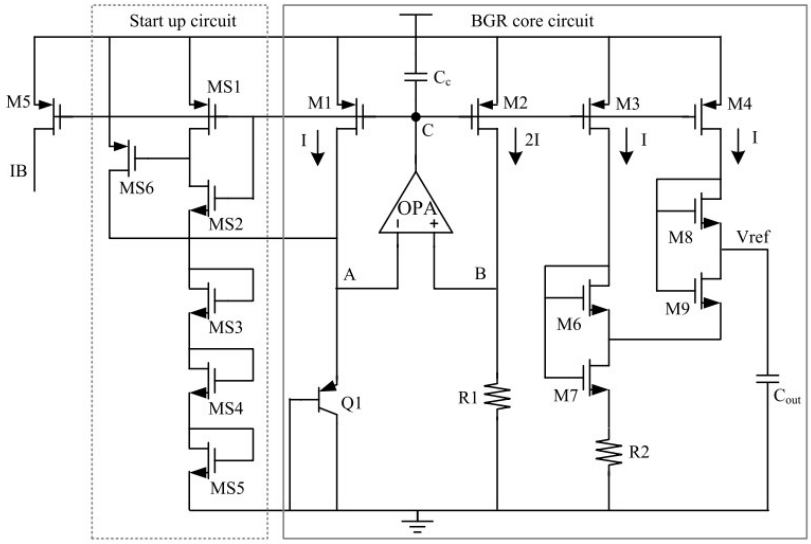

Fig. 1.25. A sub-BGR architecture published in [4]

In the recent years, a new category of voltage reference circuits has emerged. Such circuits generate the PTAT characteristics using CMOS transistors and the CTAT characteristics using BJT (vice versa). Such hybrid structure is known as sub-Bandgap reference. They are power efficient as well as area efficient.

1.10 THESIS ORGANIZATION

This thesis is organized as follows: Chapter 2 explains the CMOS only voltage reference. Chapter 3 explains the CMOS current reference. Chapter 4 explains the sub-bandgap reference circuit. Chapter 4 explains the hybrid reference circuit consisting of both voltage and current reference. Conclusion and future scope are explained in chapter 5.

CHAPTER 2

ULTRA LOW POWER CMOS VOLTAGE REFERENCE

A novel CMOS voltage reference (CVR) is presented in this chapter. The CVR architecture (Fig. 2.1) consists of a current generator circuit and a temperature compensation circuit. The current generator circuit provides a supply independent current to bias the active load in the temperature compensation circuit. The active load generates a PTAT voltage and a CTAT voltage.

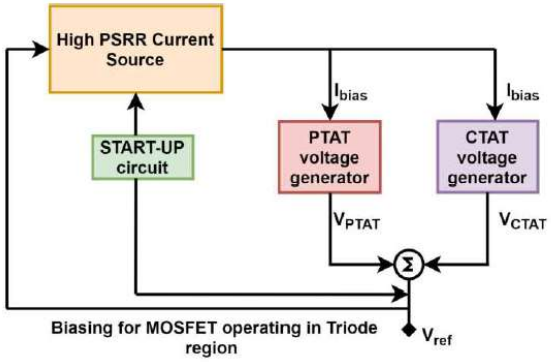

Fig. 2.1. Concept of the designed CVR

2.1 SCHEMATIC AND WORKING OF THE CMOS VOLTAGE REFERENCE

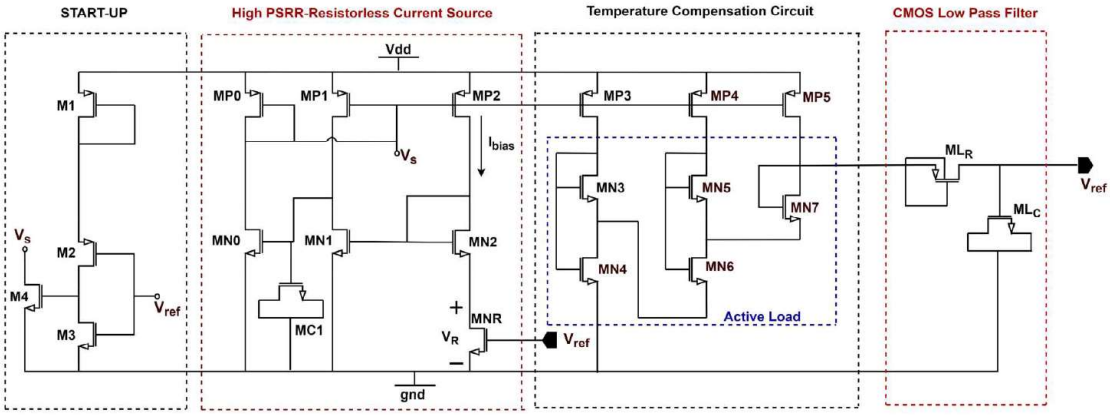

Fig. 2.2. Schematic of the CMOS voltage reference

Current through a MOSFET biased in the subthreshold region is given by:

$$I_D = Is\ (\frac{W}{L})\ exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right)\left\{1 - exp\left(\frac{-V_{DS}}{V_T}\right)\right\} \tag{2.1}$$

For $V_{DS} > 4V_T$, I_D is almost independent of V_{DS} and is given by:

$$I_D = Is\ (\frac{W}{L})\ exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right) \tag{2.2}$$

From (2.2), gate-source voltage (V_{GS}) can be written as:

$$V_{GS} = V_{th} + \eta V_T\, ln\left(\frac{I_D}{I_S \frac{W}{L}}\right) \tag{2.3}$$

Where, $Is = \mu_n(\eta - 1)C_{ox}V_T^2$; V_{th} is the threshold voltage of the transistor which has a CTAT nature, V_T is the thermal voltage which has a linear temperature dependency, μ_n is mobility, η is the subthreshold slope factor. As per Fig. 2.2, drain-source voltage (V_R) of transistor MNR can be written as:

$$V_R = V_{GS}^{MN1} - V_{GS}^{MN2} \tag{2.4}$$

V_{GS}^{MN1} and V_{GS}^{MN2} are the gate-source voltages of MN1 and MN2. Using (2.3) and (2.4), V_R can be written as:

$$V_R = \eta V_T ln\left(\frac{I_{MN1}\, S_{MN2}}{I_{MN2}\, S_{MN1}}\right) \tag{2.5}$$

I_{MN1} and I_{MN2} are the currents in transistors MN1 and MN2, S_{MN1} and S_{MN2} are the aspect ratios of MN1 and MN2, Current (I_{bias}) through the MOSFET MNR is given by:

$$I_{bias} = \frac{V_R}{R_{ds}} \tag{2.6}$$

$$= \frac{\eta V_T}{R_{ds}}\, ln\left(\frac{I_{MN1}\, S_{MN2}}{I_{MN2}\, S_{MN1}}\right) \tag{2.7}$$

R_{ds} is the resistance of the MOSFET MNR which operates in deep triode region. MNR is biased with the reference voltage. R_{ds} is mathematically written as:

$$R_{ds} = \frac{1}{\mu_n C_{OX}\left(\frac{W_R}{L_R}\right)\left(V_{GS}^{MNR} - V_{th}^{MNR}\right)} \tag{2.8}$$

Substituting (2.8) in (2.7), upon simplification, we get the current (*Ibias*) as:

$$I_{bias} = \eta V_T \mu_n C_{OX}\left(\frac{W_R}{L_R}\right)\left(V_{ref} - V_{th}^{MNR}\right) \times ln\left(\frac{I_{MN1}\, S_{MN2}}{I_{MN2}\, S_{MN1}}\right) \tag{2.9}$$

$$I_{bias}\, \alpha\ \mu_n T^2 \tag{2.10}$$

Without the feedback, due to asymmetry in the circuit, the drain-source voltage of MOSFETs MP1 and MP2 vary unequally with change in supply voltage. Therefore, currents in MP1 and MP2 are not exactly equal due to short channel effects. As a result of this, I_{bias} varies with supply. Therefore, the drain-source

voltage of MP1 and MP2 must be made equal to accurately match the currents I_{MN1} and I_{MN2}. Traditional voltage reference circuits use an amplifier to equate the drain-source voltages, which results in excessive power consumption. A feedback circuit consisting of MN0 and MP0 is used to equate the drain-source voltages in the proposed CVR. From Fig. 2.2, the feedback can be mathematically explained as following:

$$i_{bias} = g_m^{MP2} \, (v_{dd} - v_g^{MP2}) \tag{2.11}$$

$$v_g^{MN1} \approx \; - g_m^{MP2} R_{MP2} \, (v_g^{MP2} - v_{dd}) \tag{2.12}$$

$$v_g^{MN0} \approx - g_m^{MN1} R_{MN1} \, v_g^{MN1} \tag{2.13}$$

$$v_g^{MP2} \approx - g_m^{MN0} R_{MN0} \, v_g^{MN0} \tag{2.14}$$

In 2.11-2.14, i_{bias} is the small signal current. g_m^{MN0}, g_m^{MN1} and g_m^{MP2} are the transconductance of MN0, MN1, MP2. v_{dd} is the small signal supply voltage. v_g^{MN0}, v_g^{MN1} and v_g^{MP2} are the small signal gate voltage of MOSFETs. R_{MN0}, R_{MN1} and R_{MP2} are the resistance seen at the drain of MOSFETs MN0, MN1, MP2. From (2.12), (2.13), (2.14), v_g^{MP2} can be written as:

$$v_g^{MP2} \approx \frac{g_m^{MP2} R_{MP2} \, g_m^{MN1} R_{MN1} \, g_m^{MN0} R_{MN0}}{1 + g_m^{MP2} R_{MP2} \, g_m^{MN1} R_{MN1} \, g_m^{MN0} R_{MN0}} \, v_{dd} \tag{2.15}$$

$$Loop\ Gain_{\text{-ve feedback}} = g_m^{MP2} R_{MP2} \, g_m^{MN1} R_{MN1} \, g_m^{MN0} R_{MN0} \tag{2.16}$$

The gain achieved by the negative feedback formed by MN0, MP0, MP2, MN2, R_{ds}, MN1 is much larger than the gain achieved by the positive feedback formed by MN0, MP0, MP1, MN1 due to common-source amplification. Therefore, (2.11-2.15) are approximated and v_g^{MP2} can be written as follows:

$$v_g^{MP2} \approx v_{dd} \tag{2.17}$$

From (2.11) and (2.17), it can be concluded that the current is insensitive to change in supply voltage This results in an excellent PSRR of –75dB at DC for the reference voltage. A MOSFET (MC1) is used as a capacitor to ensure the stability of the generated current. Temperature compensation is achieved with the help of the CTAT nature of gate-source voltage of MN7 and PTAT nature of ΔV_{GS} of MN3-MN4 and MN5-MN6 (Fig. 2.2). MN3-MN7 are operated in the subthreshold region. Temperature compensation is mathematically explained below:

From (2.3), V_{GS}^{MN7} can be written as:

$$V_{GS}^{MN7} = V_{th}^{MN7} + \eta V_T \, ln\left(\frac{I_{bias}}{I_S \, S_{MN7}}\right) \tag{2.18}$$

The temperature dependency of V_{th} can be approximated as:

$$V_{th} = V_{th}(T_0) - \alpha_T (T - T_0) \tag{2.19}$$

$V_{th}(T_0)$ is the threshold voltage of the MOSFET at room temperature and α_T is the first derivative of threshold voltage with respect to temperature. The first term in (2.18) is dominant. Therefore, V_{GS}^{MN7} provides a CTAT voltage. From Fig. 2.2, the reference voltage (V_{ref}) can be written as:

$$V_{ref} = V_{GS}^{MN7} + \Delta V_{GS}^{MN3,4} + \Delta V_{GS}^{MN5,6} \tag{2.20}$$

$$= V_{GS}^{MN7} + \eta V_T ln \left(\frac{S_{MN5}\, S_{MN3}}{S_{MN6}\, S_{MN4}}\right) \tag{2.21}$$

The temperature dependency of V_T can be written as:

$$V_T = \frac{kT}{q} \tag{2.22}$$

In (2.20), $\Delta V_{GS}^{MN3,4}$ is the difference between gate-source voltage of MN3 and MN4, $\Delta V_{GS}^{MN5,6}$ is the difference between gate-source voltage of MN5 and MN6, k is Boltzmann's constant. The first term in (2.21) has a CTAT nature and the second term has a PTAT nature. Therefore, the reference voltage (V_{ref}) is temperature compensated.

2.2 RESULTS AND DISCUSSION

The proposed CVR is designed in TSMC 180nm technology. The variation of reference voltage with respect to supply voltage is plotted in Fig. 2.4. A line sensitivity of 0.02%/V is achieved for the reference voltage for a supply voltage range of 0.9V to 2.3V. The variation of reference voltage with respect to temperature is shown in Fig. 2.5. A TC of 84 ppm/˚C is noted at the typical corner for a temperature range of -20 ˚C to 80 ˚C. The proposed circuit can deliver a reference voltage around 680mV from a supply as low as 0.85 V. The feedback consumes 11nW of power. A decent phase margin of 55 degrees is noted for the feedback in the simulation. The branch consisting of MP1 consumes 13nA of current and 5.2nA of current flows through MP3-MP5. Monte-Carlo simulations for TC and reference voltage are performed to test the circuit for mismatch and process variations (Fig. 2.6). The reference voltage has a mean of 681mV and a standard deviation of 16mV. A spread (σ/μ) of 2.3% is noted for the proposed CVR which is better than [8] which has a spread of about 5%. TC takes a maximum value of 184 ppm/˚C and a minimum value of 69 ppm/˚C in the Monte-Carlo simulation. An average TC of 100 ppm/˚C is noted. An excellent PSRR of -75dB is noted for the circuit at 10Hz (Fig. 2.7). Furthermore, the included CMOS LPF [16] improves the PSRR at higher frequencies. A PSRR of -46 dB is noted at 10MHz. The power consumption of the CVR across the temperature range is plotted in Fig. 2.8. The circuit consumes less than 50nW of power across the temperature range in typical corner. Layout for the CVR occupies an area of 0.065mm^2 (Fig. 2.9). The proposed CVR is compared with the state of the art in Table 1.

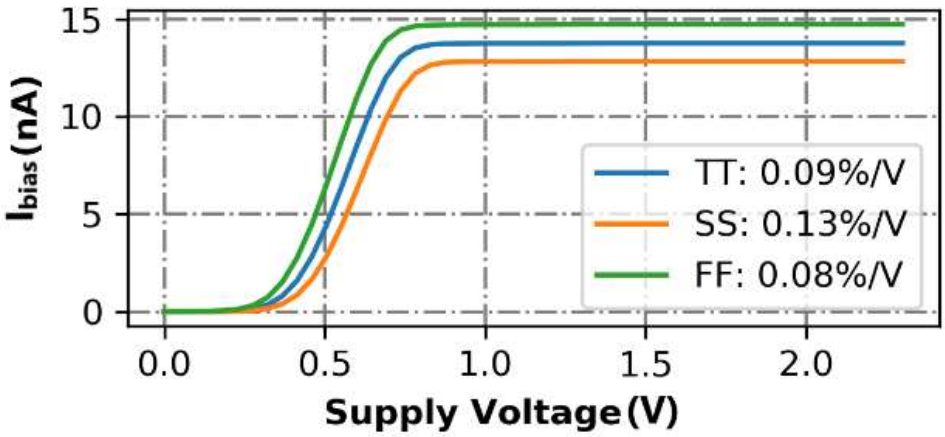

Fig. 2.3. I_{bias} vs Supply Voltage (V_{dd})

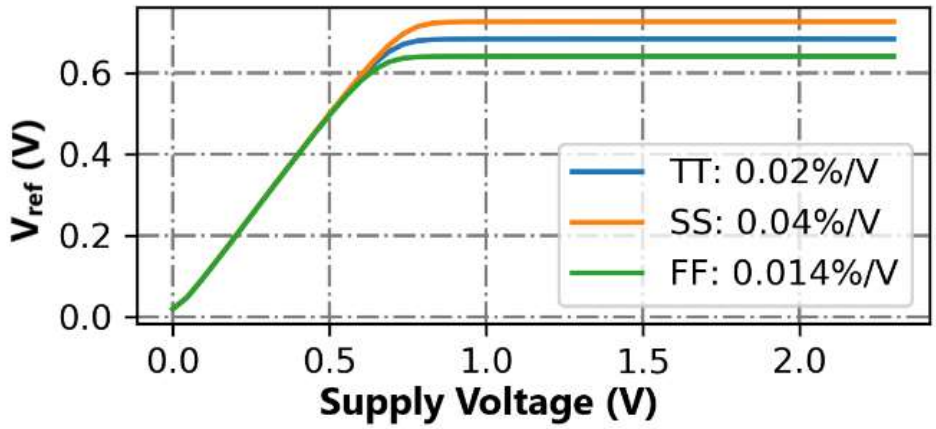

Fig. 2.4. V_{ref} vs Supply Voltage (V_{dd})

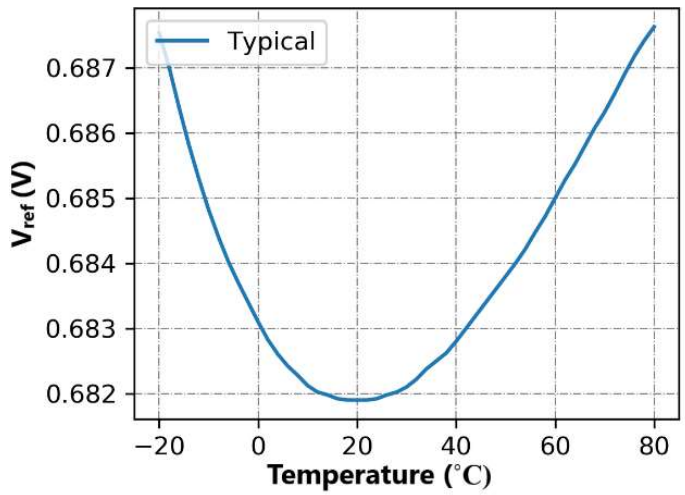

Fig. 5. V_{ref} vs Temperature

Table 1: Performance summary and comparison

SPECIFICATIONS	This Work	[8]	[14]	[15]	[16]
Technology (nm)	**180**	65	130	180	180
V_{ref} (mV)	**681**	460	800	630	893
V_{dd} (V)	**0.85-2.3**	0.9-2.6	1.1-2.4	1.35-1.8	1.1-2
Temperature Range (˚C)	**-20 to 80**	-40 to100	-40 to 85	-20 to 80	-30 to 80
Power (nW)	**46**	480	27.5	1188	550
TC (max) **TC (min) (ppm/ ˚C)** **TC (avg)**	**184** **69** **100**	55 4.2 13.9	450 30 100	44.4 14 14.1	NA NA 19
LS (%/V)	**0.02**	2.29	2	0.105	0.09
PSRR (dB) @10Hz **@10MHz**	**-75** **-46**	-38 -61	-36 NA	-75.6 NA	-75 -50

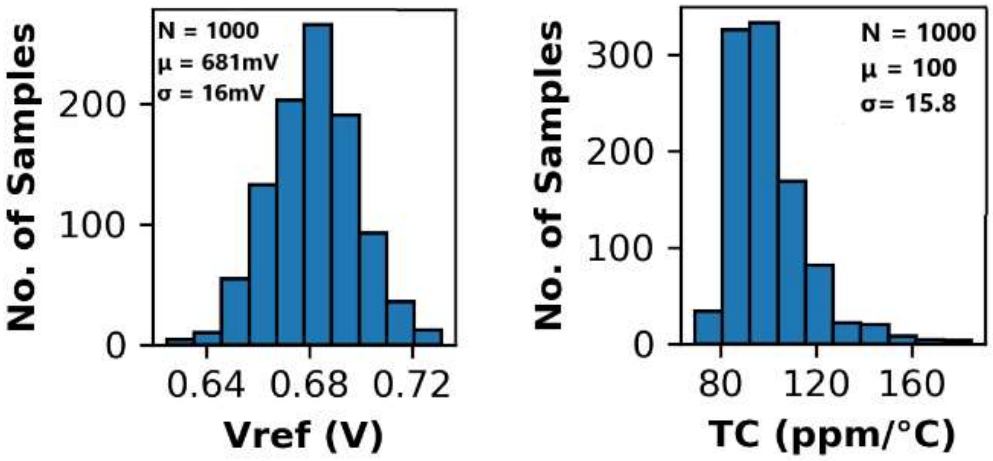

Fig. 2.6. Monte-Carlo for V_{ref} and TC

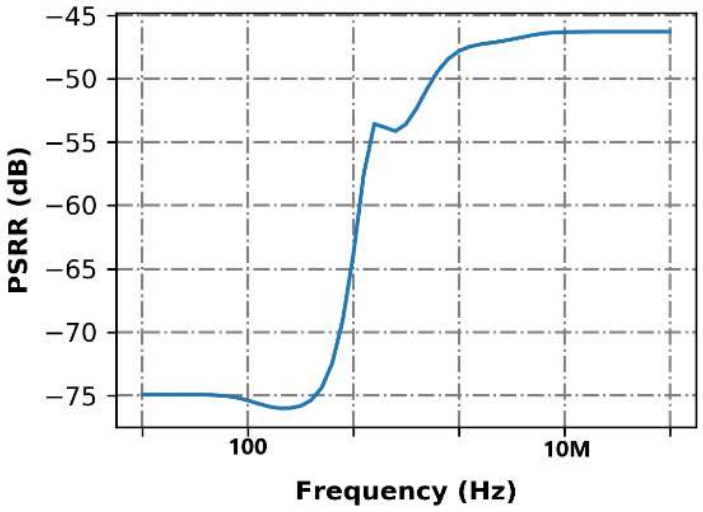

Fig. 2.7. PSRR of the Proposed Circuit

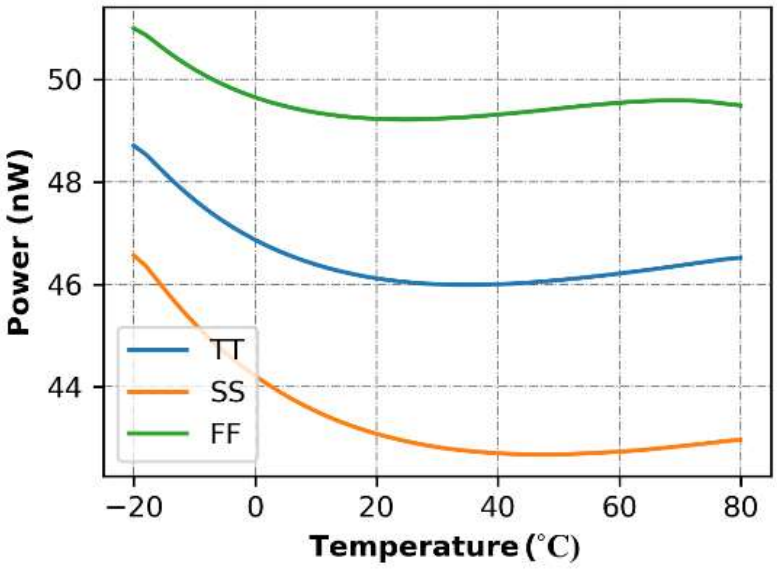

Fig. 2.8. Power Consumption (nW) in Various Process Corners

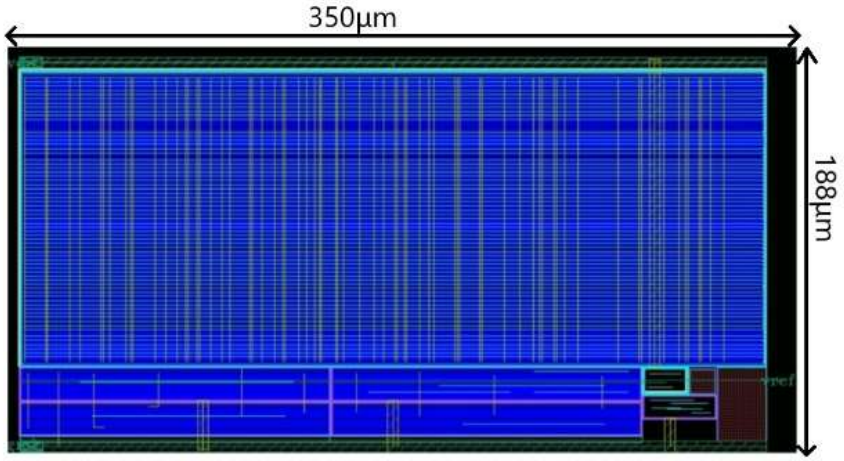

Fig. 2.9. layout of the proposed CMOS voltage reference

2.3 CONCLUSION

A CVR is presented in this chapter which delivers a reference voltage around 680mV. The proposed CVR works from a supply voltage as low as 0.85V and achieves a high PSRR of -75dB at 10 Hertz and -46 dB at 10 Mega Hertz. A line sensitivity of 0.02%/V is noted for the proposed CVR. The circuit consumes only 46nW of power at 0.85V supply, which makes it suitable for ultra-low power applications.

CHAPTER 3

ULTRA LOW POWER CMOS CURRENT REFERENCE

A highly stable CMOS current reference using a peaking current source is proposed in this chapter. The advantage of the proposed work is that the temperature compensation of reference current is achieved by taking the ratio of compensated voltage (Vcomp) and on-chip resistance without using an opamp. Where Vcomp is a temperature compensated voltage. The minimum supply voltage achieved is 0.55V, which makes it suitable for low voltage applications. The proposed architecture uses a similar VTH MOSFET to avoid additional masks. The conceived CMOS current reference uses PD-AMP to suppress second order effects such as channel length modulation (CLM) and drain induced-barrier-lowering (DIBL) and achieves remarkably low line sensitivity of 0.022%/V. Additionally, the results shows the power consumption is remarkably reduced to 9.5nW.

3.1 SCHEMATIC AND WORKING OF THE CMOS CURRENT REFERENCE

The proposed current reference is illustrated in Fig. 3.1. The PTAT voltage is generated from the supply independent peaking current block by taking the difference of the gate to source voltage of the MOSFET. The CTAT voltage is generated by exploiting the dependence of threshold voltage on the body to source voltage of MOSFET. Transistors MR1 and MC1 are used for frequency compensation. All the MOSFETs operate in the sub-threshold region, which results in low power consumption. Transistors M1-M4 consist of the start-up circuit that brings out the core circuit from a dead operating point (zero current) to its normal operating point. When the circuit reaches the desired operating point, the start-up operation gets over.

Considering the supply independent peaking current block shown in Fig. 3.1:

$$I_{in} = \frac{VGS_{MP3} - VGS_{MP4}}{R} \tag{3.1}$$

When the drain-source voltage of a transistor (VDS) is more than 4VT , the well-known subthreshold current equation can be written as: (well-illustrated in [7])

$$I_D = Is \left(\frac{W}{L}\right) exp\left(\frac{V_{GS} - V_{th}}{\eta V_T}\right) \tag{3.2}$$

Where, $Is = \mu_n(\eta - 1)C_{ox}V_T^2$; (W/L) is the ratio of transistor's width and length, VGS is the gate to source voltage of the MOSFET, Vth is the threshold voltage of the transistor, VT = KT/q is the thermal voltage which has a linear temperature dependency, μ_n is mobility and η is the subthreshold slope factor. From Eq. (3.1) and Eq. (3.2), I_{in} can be written as shown in Eq. (3.3):

$$I_{in} = \frac{Vth_{MP3} - Vth_{MP4} + \eta VT\ ln\left(\frac{Iin\ K4}{Iref\ K3}\right)}{R} \tag{3.3}$$

where, $K4/K3 = (W/L)_{MP4}/(W/L)_{MP3}$. MP3 and MP4 being similar Vth MOSFET, Iref can be written as:

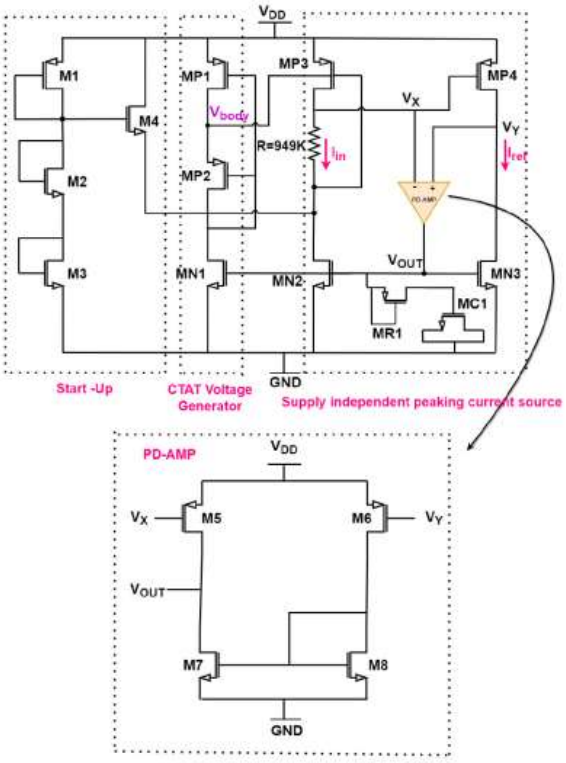

Fig. 3.1. Schematic of the proposed current reference

$$I_{ref} = I_{in}\frac{K4}{K3}exp(\frac{-Iin\,R}{\eta VT}) \tag{3.4}$$

Considering the current mirror, and assuming m = $(W/L)_{MN3}/(W/L)_{MN2}$ and MP3 and MP4 being similar Vth MOSFET, Eq. (4) can be written as shown in Eq. (5):

$$I_{ref} = \frac{\eta mVT}{R}\,ln(\frac{K4}{m\,K3}) \tag{3.5}$$

From Eq. (5) temperature coefficient of the output current is derived as:

$$TC_{Iref} = \frac{\partial Iref}{T\,\partial T} = -TC_R + TC_{VT} \tag{3.6}$$

In which, TC_R and TC_{VT} are temperature coefficients of thermal voltage and R, respectively. From Eq. (3.6), the reference current of a peaking current source cannot be made temperature independent (well-illustrated in [13]). The proposed architecture of peaking current source is made supply independent by pseudo-differential amplifier shown in Fig. 1. For VDS ≥ 4VT the drain current of a MOSFET becomes almost independent of drain voltage Eq. (3.2). Such current saturation is observed in long channel MOSFET where DIBL effect is negligible. In short channel MOSFET due to DIBL, drain current depends on VDS since the threshold voltage becomes a function of VDS (well-illustrated in [14]). Therefore, currents in MP3 and MP4 are not exactly equal and vary with supply. A PD-AMP is used instead of a traditional op-amp to make the node voltage at VX and VY equal so that the effects of DIBL is compensated. A MOSFET MC1 is used as a capacitor and MR1 is used as a resistor for frequency compensation. The PD-AMP consumes a current of 0.62nA which makes it suitable for ultra-low power

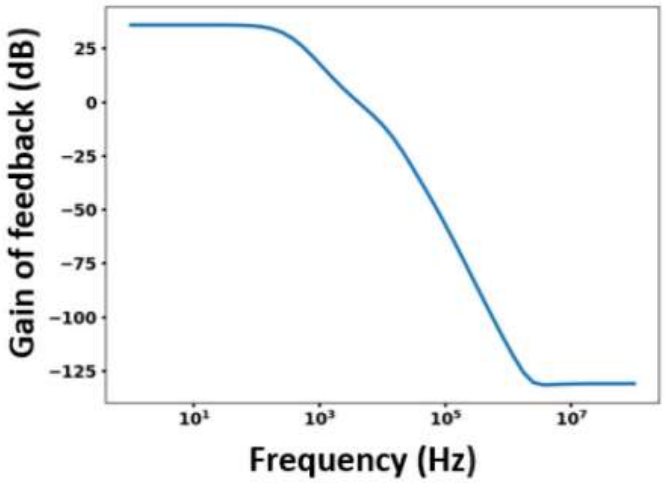

Fig. 2. Loop gain noted in the core of the current reference

applications. A phase margin of 37.50◦ is achieved for the feedback and loop gain of feedback is 39.5dB Fig. 3.2 which is good enough to ensure low line regulation of 0.022%/V.

CTAT voltage generator block is depicted in Fig. 3.1. MP1 and MP2 are similar Vth MOSFET. MP1, MP2 and MN1 are kept in subthreshold region. Since the current through MP1 and MP2 is equal, V_{body} can be expressed as:

$$V_{body} = Vth_{MP1} - Vth_{MP2} + \eta VT\ ln\left(\frac{K2}{K1}\right) + VDD \tag{3.7}$$

$$\Delta Vth_{1,2} = Vth_{MP1} - Vth_{MP2} \tag{3.8}$$

The term VDD − ηVT lnK2/K1 in Eq. (8) generates a CTAT voltage. $\Delta Vth_{1,2}$ is a very small value and MP1 and MP2 are similar type of MOSFET, so it can be neglected. By proper sizing of MP1 and MP2, the CTAT term can be controlled. The generated V_{body} can track VDD making a constant V_{body} −VDD with respect to supply. As shown in Fig. 3.1, we use V_{body} to bias the body terminal of MOSFET MP3. Since V_{body}−VDD is constant, |VBS| of MP3 is supply insensitive as shown in Fig. 3.3.

The key idea of the architecture is to generate temperature independent current reference by taking the ratio of compensated voltage (Vcomp) and on-chip resistance R as shown in Eq. (3.9)

$$I_{ref} = \frac{V_{COMP}}{R} = \frac{V_{COMP0}(1+\alpha_{COMP}\,\Delta T)}{R0\,(1+\alpha_R\,\Delta T)} \tag{3.9}$$

where, V_{comp0} and R_0 are the voltage and the resistance at nominal temperature T0, and α_{comp}, α_R are their TCs, respectively. By making the TC of V_{comp} equal to the TC of the resistance, I_{ref} can be made temperature independent. As MP3 and MP4 are the same type of MOSFET, the CTAT voltage is generated from the body bias effect on the Vth of MP3. From Eq. (3.3), I_{ref} can be expressed as:

$$I_{ref} = \frac{\sqrt{2\,\Phi_F - \eta VT\ ln\left(\frac{K2}{K1}\right)} - \sqrt{2\,\Phi_F} + \eta VT\ ln\left(\frac{Iin\,K4}{Iref\,K3}\right)}{R} \tag{3.10}$$

The term 2φF − ηVT ln(K2/K1) in Eq. (3.10) generates a CTAT voltage, where K2/K1 = $(W/L)_{MP2}/(W/L)_{MP1}$ and the second term generates a PTAT voltage. Taking derivative of Eq. (3.10) with

Device	Width (μm)	Length (μm)	Multiplier
MN1-MN3	1	10	50
MP1	1	10	16
MP2	1	10	60
MP3	1	10	15
MP4	1	10	27
M5-M8	0.5	10	3

Table. 3.1. Design values

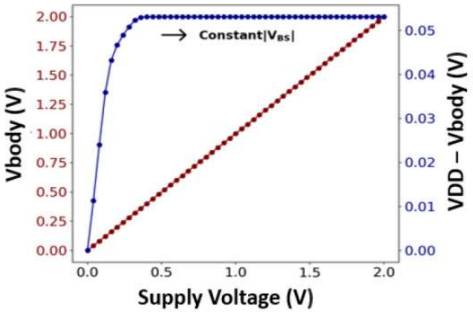

Fig. 3.3. V_{body} tracks VDD change and creates constant |VBS| for MP3.

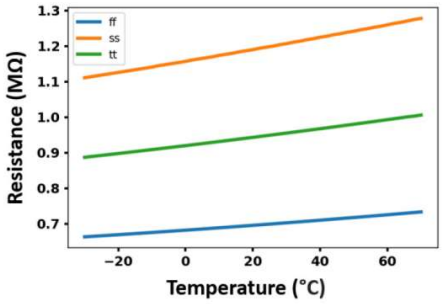

Fig. 3.4. R at different process corners.

respect to temperature and equating it with zero, we come to a relation between the TC of on-chip resistance (α_R) and the aspect ratio of MOSFETs MP1-MP4. The TC of on-chip resistance can be written as shown in Eq. (11):

$$TC_R = \frac{\partial R}{T\,\partial T} \tag{3.11}$$

Temperature independence of I_{ref} can be achieved by proper choice of on-chip resistance and proper sizing of the aspect ratio of MOSFET MP1-MP4. The process dependence of the on-chip resistance depends upon how R and α_R are related to process variation. Fig. 4 illustrates the value of R in various process corner (TT, FF, SS). The plot of I_{ref} at different process corners is shown in Fig. 9. The component parameters used in the proposed circuit is shown in Table I.

3.2 RESULTS AND DISCUSSION

The proposed current reference is designed in TSMC 180nm technology, and the simulation results are demonstrated. The resistor is implemented using a p-poly resistor. All MOSFETs operate in sub-threshold region. The circuit consumes only 9.5nW of power from a 0.55V supply. This current reference reduces the power in orders of 3 compared to the existing low power designs at typical conditions (minimum supply voltage and room temperature). A line sensitivity of 0.022%/V is achieved for a supply voltage range of 0.55V to 1.9V, as shown in Fig. 3.5. The variation of Iref with respect to temperature is shown in Fig. 3.6. A TC of 162ppm/◦C is achieved at typical corner for the temperature range of -30◦C to 70◦C. Fig. 3.7 shows the dependence of I_{ref} on supply and temperature variation.

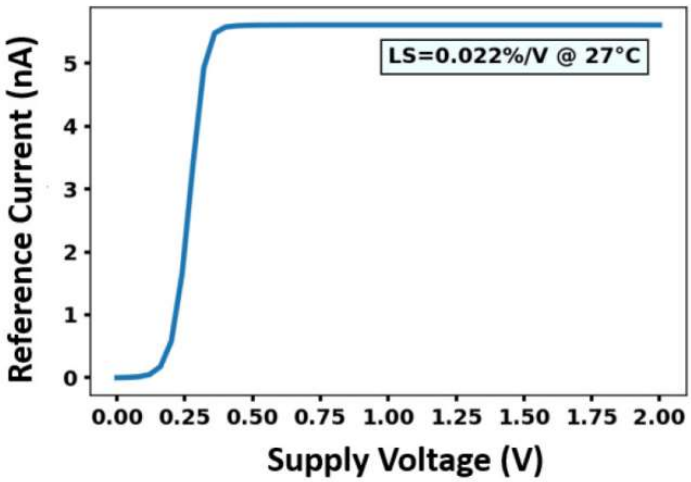

Fig. 3.5. Influence of supply variations on I_{ref} @ TT corner.

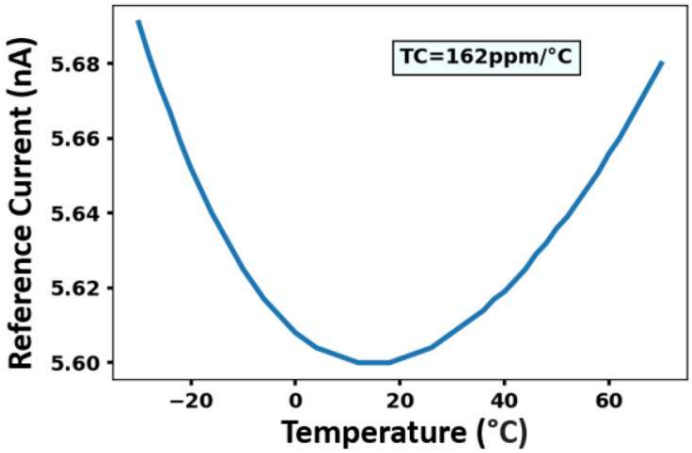

Fig. 3.6. Influence of temperature variations on I_{ref}.

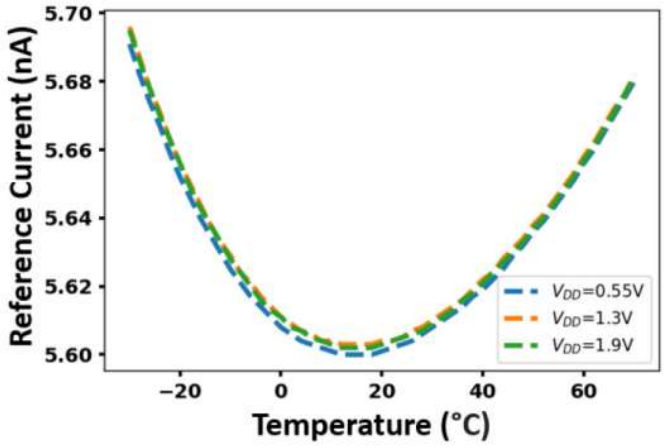

Fig. 3.7. I_{ref} at different values of supply voltage.

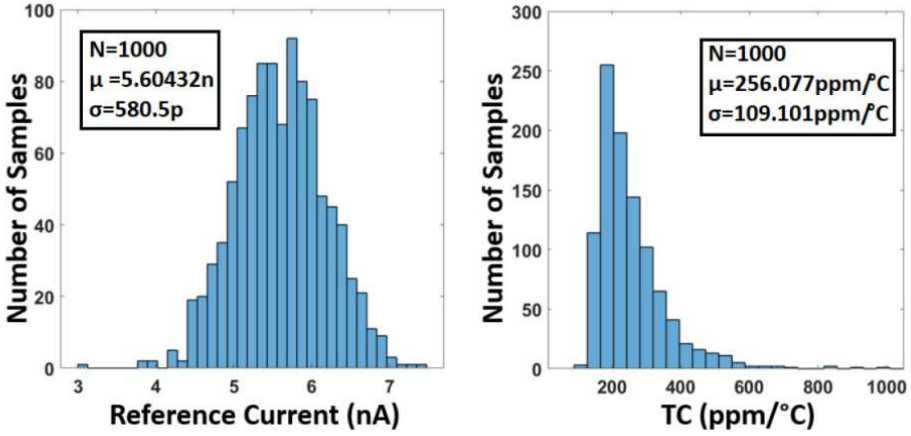

Fig. 3.8. Monte Carlo for I_{ref} and TC.

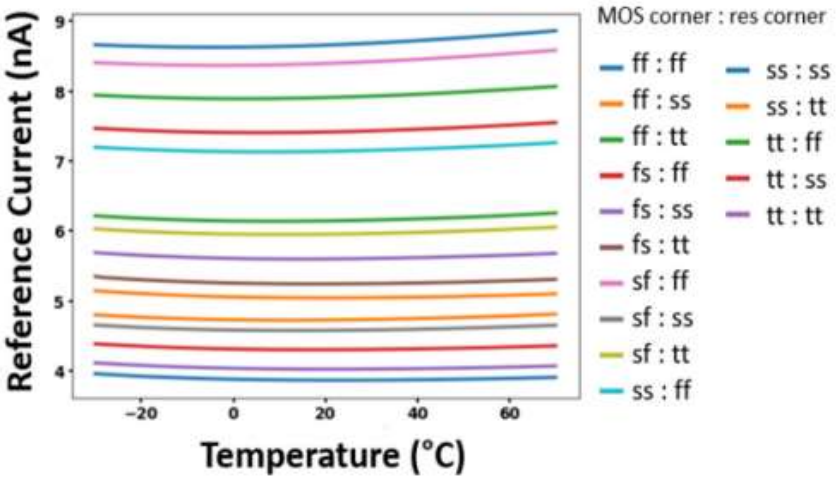

Fig. 3.9. I_{ref} vs temperature at different corners.

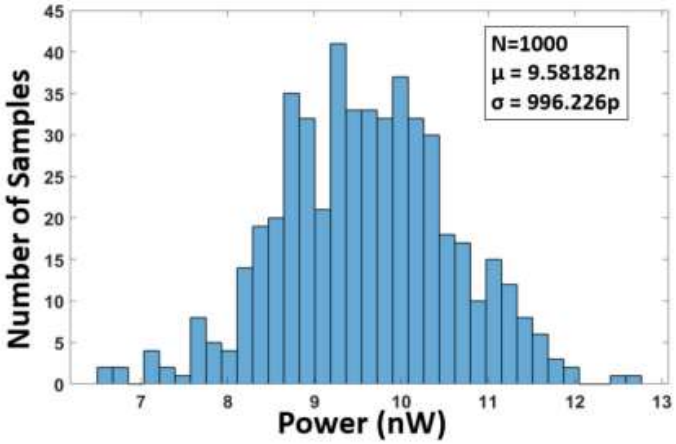

Fig. 3.10. Monte Carlo simulation for power.

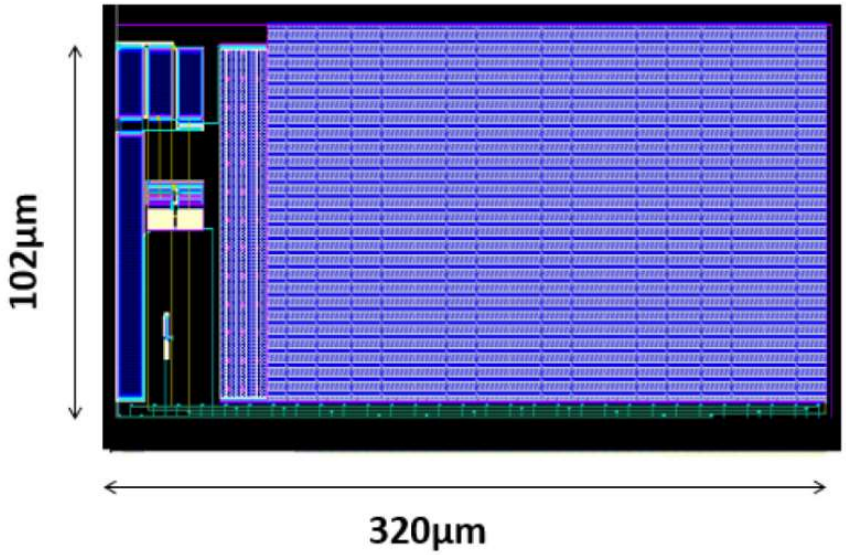

Fig. 3.11. Layout of the proposed design

In order to look into the effect of process variations on reference current and its TC, Monte-Carlo simulations are performed Fig. 3.8 for 1000 samples. The reference current has a mean (µ) of 5.6nA and the standard deviation (σ) is 580.5pA. An average TC of 256.07ppm/◦C and standard deviation (σ) of 109.1ppm/◦C is noted. To prove the property of the circuit for ultra-low-power applications, Monte Carlo simulations is performed for power consumption on 1000 samples and the obtained plot with a mean (9.58nW) and standard deviation (996.2pW) is shown in Fig. 3.10. Layout for the circuit is done and occupies an active area of 0.0326mm2 as shown in Fig. 3.11. It can be seen that the proposed current reference achieves the lowest supply voltage of 0.55V and lowest line sensitivity of 0.022%/V. All results are shown for post layout simulations.

3.3 CONCLUSION

Low power and low voltage CMOS current reference with a 0.55V supply and is herein presented. A peaking current source is proposed which cancels out the ratio of the compensated voltage and on-chip resistance by employing a CTAT voltage generator which exploits the threshold voltage dependence on the body to source voltage of the MOSFET, while consuming only 9.5nW of power and generating 5.6nA of reference current. The design enhances the performance of line regulation with the adopted PD-AMP which consumes only 0.62nA of current. The performance of the proposed circuit makes it suitable for biomedical applications that require low-supply voltage and power consumption.

CHAPTER 4

SUB-BANDGAP VOLTAGE REFERENCE

The Proposed sub-BGR (Fig. 4.1.) consists of a supply independent current source, a voltage divider, cascaded PTAT voltage generator blocks and a low pass filter. The emitter-base voltage of a BJT present in the current source generates a CTAT voltage. The slope of the CTAT voltage is adjusted with the voltage divider circuit and PTAT voltage generators are cascaded to generate the PTAT voltage for temperature compensation of the reference voltage. A low pass filter is included to improve the PSRR at higher frequencies.

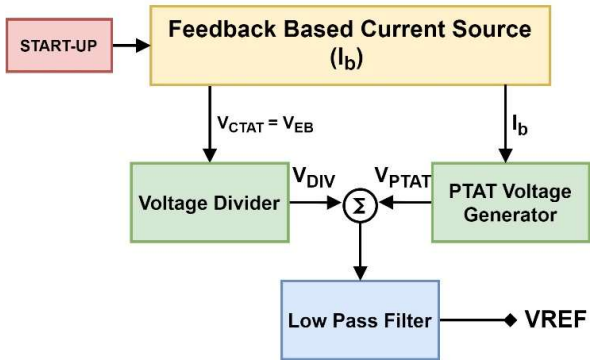

Fig. 4.1. Concept of the sub-Bandgap Reference

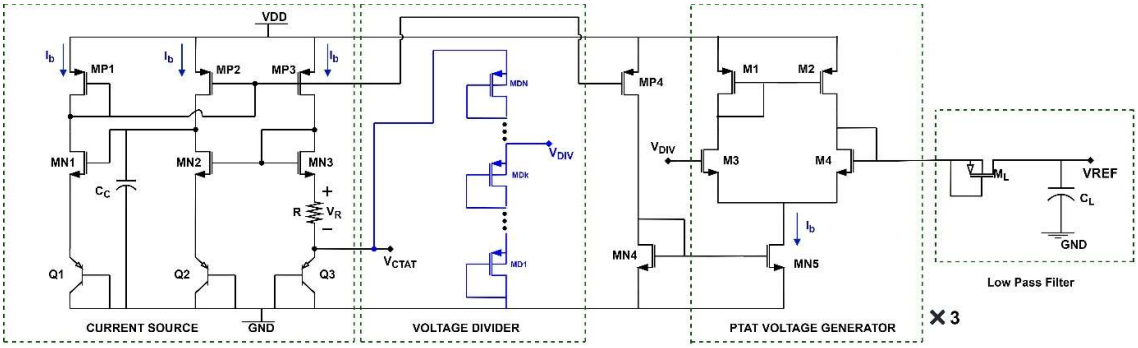

Fig. 4.2. Schematic of the proposed Sub-Bandgap Reference

4.1 WORKING OF THE PROPOSED SUB-BGR

Current through a MOSFET biased in the subthreshold region is given by:

$$I_D = Is\left(\frac{W}{L}\right) exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right)\left\{1 - exp\left(\frac{-V_{DS}}{V_T}\right)\right\} \quad (4.1)$$

For $V_{DS} > 4V_T$, I_D is almost independent of V_{DS} and is given by:

$$I_D = Is\left(\frac{W}{L}\right) exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right) \tag{4.2}$$

From (2), gate-source voltage (V_{GS}) can be written as:

$$V_{GS} = V_{th} + \eta V_T \, ln\left(\frac{I_D}{I_S \frac{W}{L}}\right) \tag{4.3}$$

Where, $Is = \mu_n(\eta - 1)C_{ox}V_T^2$; V_{th} is the threshold voltage of the transistor which has a CTAT nature, V_T is the thermal voltage which has a linear temperature dependency, μ_n is mobility, η is the subthreshold slope factor. As per Fig. 4.2, keeping the emitter areas of Q2 and Q3 same, the voltage across the resistor (V_R) can be written as:

$$V_R = V_{GSMN2} - V_{GSMN3} \tag{4.4}$$

V_{GSMN2} and V_{GSMN3} are the gate-source voltages of MN2 and MN3. Using (4.3) and (4.4), V_R can be written as:

$$V_R = \eta V_T ln\left(\frac{I_{MN2}\, S_{MN3}}{I_{MN3}\, S_{MN2}}\right) \tag{4.5}$$

I_{MN2} and I_{MN3} are the currents in transistors MN2 and MN3, S_{MN2} and S_{MN3} are the aspect ratios of MN2 and MN3, current (I_b) through the resistor (R) is given by:

$$I_b = \frac{V_R}{R} \tag{4.6}$$

$$I_b = \frac{\eta V_T}{R} ln\left(\frac{I_{MN2}\, S_{MN3}}{I_{MN3}\, S_{MN2}}\right) \tag{4.7}$$

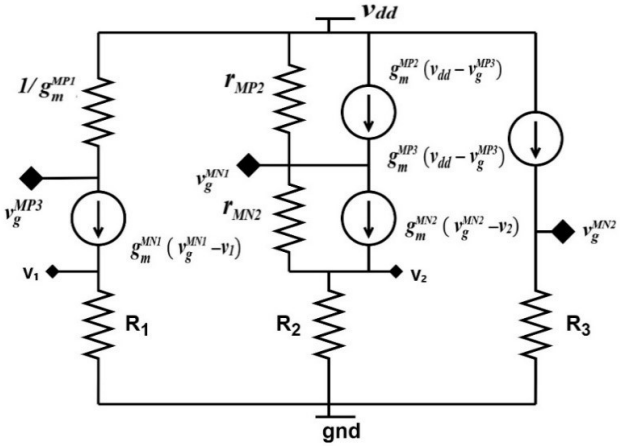

Fig. 4.3. Small Signal model for Feedback Analysis

Without the feedback (*MP1, MN1, Q1*), the drain-source voltage of *MP2* and *MP3* vary unequally with supply due to asymmetry in the circuit. Therefore, currents I_{MN2} and I_{MN3} are not exactly equal due to short channel effects. The drain-source voltage of *MP2* and *MP3* must be made equal to ensure good line regulation of the generated current (I_b). The core of the current source circuit consists of a negative feedback loop (*MP3, MN3, MN2, MN1, MP1*) and a positive feedback loop (*MP2, MN2, MN1, MP1*). From Fig. 4.2, the feedback can be mathematically explained as following:

$$i_b \approx g_m^{MP3} \left(v_{dd} - v_g^{MP3}\right) \tag{4.8}$$

$$v_g^{MN2} \approx -g_m^{MP3} R_3 \left(v_g^{MP3} - v_{dd}\right) \tag{4.9}$$

$$v_g^{MN1} \approx -\frac{g_m^{MN2} r_{MP2} r_{MN2}}{R_2 + r_{MN2} + r_{MP2} + r_{MN2} g_m^{MN2} R_2} \; v_g^{MN2} \tag{4.10}$$

$$v_g^{MP3} \approx v_{dd} - \frac{g_m^{MN1} v_g^{MN1}}{(1 + g_m^{MN1} R_1)\, g_m^{MP1}} \tag{4.11}$$

In 4.8-4.11, i_b is the small signal current. g_m^{MN1}, g_m^{MN2} and g_m^{MP3} are the transconductance of MN1, MN2, MP3. v_{dd} is the small signal supply voltage. v_g^{MN1}, v_g^{MN2} and v_g^{MP3} are the small signal gate voltage of MOSFETs. $R_1 = 1/g_{Q1}$; $R_2 = 1/g_{Q2}$; $R3 \approx 1/g_m^{MN3} + 1/g_{Q3} + R$; g_m an g_Q are the transconductance of the MOSFET and BJT respectively. From (4.8-4.11), v_g^{MP3} can be written as:

$$v_g^{MP3} \approx v_{dd} \tag{4.12}$$

$$Dominant\ Pole = \frac{1}{2\pi\{(R_2 + r_{MN2} + r_{MN2} g_m^{MN2} R_2) || r_{MP2}\} C_C} \tag{4.13}$$

The gain of the negative feedback is larger than the gain of the positive feedback due to the common-source (degenerated) amplification at *MN2*. From (4.12), it can be noted that the gate of $MP_{1\text{-}3}$ closely tracks any change in supply. This ensures the stability of the current generator circuit and a supply independent current (I_b) is generated (Fig. 4.5). A capacitor C_C is used for frequency compensation. A decent phase margin of 56 degrees is achieved for the feedback and the loop gain of the feedback is 35dB (Fig. 4.4) which is good enough to accurately match the drain-source voltage of MOSFETs *MP2* and *MP3*.

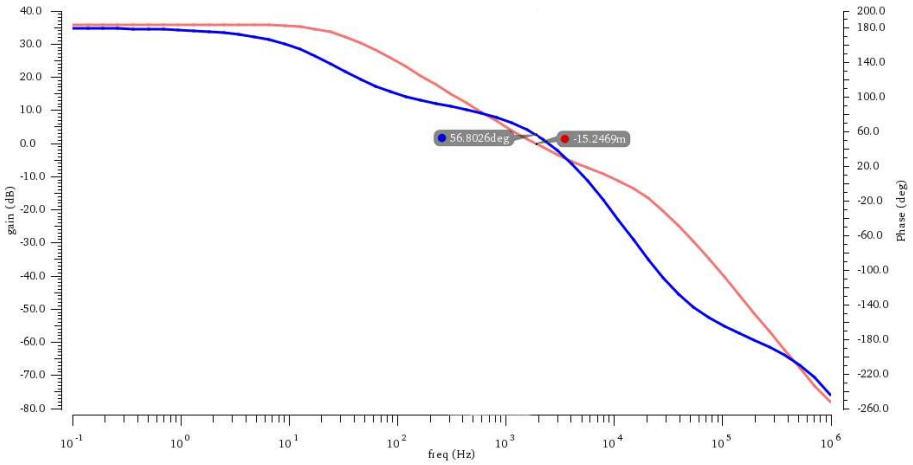

Fig. 4.4. Loop Gain of the Current Source Feedback loop

The generated reference voltage is the sum of the CTAT emitter-base voltage of the BJT (Q3) and the PTAT voltage generated by the differential cell (M1-M4, MN5). For nanoamps of bias current, the absolute value of the TC of the emitter-base voltage is very high. Therefore, a voltage divider [9] consisting of PMOS transistors (MD1-MDN) is used for adjusting the slope of the CTAT voltage. V_{DIV} can be written as:

$$V_{DIV} = \frac{k}{N} V_{CTAT} \tag{4.14}$$

Where, $V_{CTAT} = V_{EB}$ of Q3; N is the total number of PMOS transistors present in the voltage divider circuit. The voltage divider draws negligible current ($gm_{D1\text{-}DN} << g_{Q3}$). Differential cell-based PTAT voltage generators are used instead of NMOS composite pairs [10] since the differential cell offers high input impedance, thus, the operating point of the MOSFETs present in the voltage divider circuit are not disturbed. The reference voltage (VREF) can be written as:

$$VREF = \frac{k}{N} V_{CTAT} + 3\eta V_T ln\left(\frac{S_{M2}\, S_{M3}}{S_{M1}\, S_{M4}}\right) \tag{4.15}$$

The temperature dependency of V_T can be written as:

$$V_T = \frac{kT}{q} \tag{4.16}$$

The first term in equation (4.15) is CTAT in nature and the second term is PTAT in nature. Sizes of M1-M4, k and N are adjusted such that the reference voltage is temperature compensated. Although, temperature compensation can be achieved with a single stage of the differential cell by having short channel devices for $M_{2,3}$; such approach leads to excessive size ratio between $M_{2,3}$ and $M_{1,4}$. Therefore, three such differential stages are used for reducing the area at the cost of increased power dissipation.

Process variations in the generated PTAT current (I_b) due to the resistor (R) introduce process variations in the CTAT voltage (V_{EB}). The current (I_b) varies from 3.86nA (resistor in slow corner) to 5.2nA (resistor in fast corner), thereby, varying the CTAT voltage from 564mV to 572mV which translates to a σ/μ of 0.32% for the reference voltage in the Monte-Carlo simulation for process variations. A LPF is included in the proposed sub-BGR to improve the PSRR at higher frequencies. The resistor is implemented with a PMOS transistor in cut-off, thereby, making the LPF area efficient. The LPF's cut-off frequency (f_c) can be written as:

$$f_c = \frac{1}{r_{dsML}\,(C_{gdML} + C_{bdML} + C_L)} \tag{4.17}$$

$$r_{dsML} = Is\left(\frac{W}{L}\right)_{ML} exp\left(\frac{-|V_{th}|}{\eta V_T}\right) exp\left(\frac{-V_{ds}}{V_T}\right) \tag{4.18}$$

4.2 Results and Discussion

The proposed voltage reference is designed in TSMC 180nm technology. The reference voltage achieves a line sensitivity of 1%/V in the supply range of 1.2V to 2.2V (Fig. 4.7). The behavior of the generated PTAT current with respect to temperature for various process corners of resistor (R) is shown in Fig. 4.8. The process variations in the PTAT current are due to the "rphripoly" resistor R (20μm x 200μm). The behavior of the reference voltage with respect to temperature (when R is in TT, SS and FF) is shown in Fig.4.9. The reference voltage achieves a TC of 10ppm/˚C in the typical corner. The proposed voltage reference consumes a total of 31nA of current from supply at room temperature. A PSRR of 40dB is noted at DC for the reference voltage (Fig. 4.10). The reference voltage takes an

average value of 839mV and the standard deviation is 2.68mV in the Monte-Carlo simulation for 1000 samples resulting in a spread σ/μ of 0.32% (Fig. 4.11). An average TC of 16 ppm/˚C is noted in the Monte-Carlo simulation for process variations (Fig. 4.11).

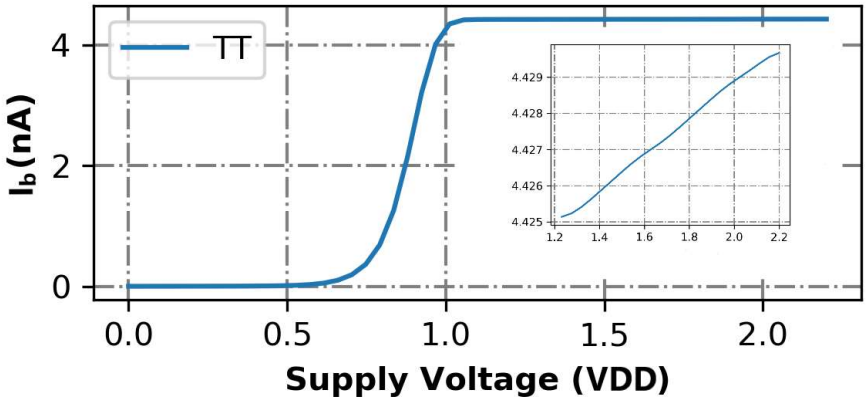

Fig. 4.5. I_b vs supply VDD

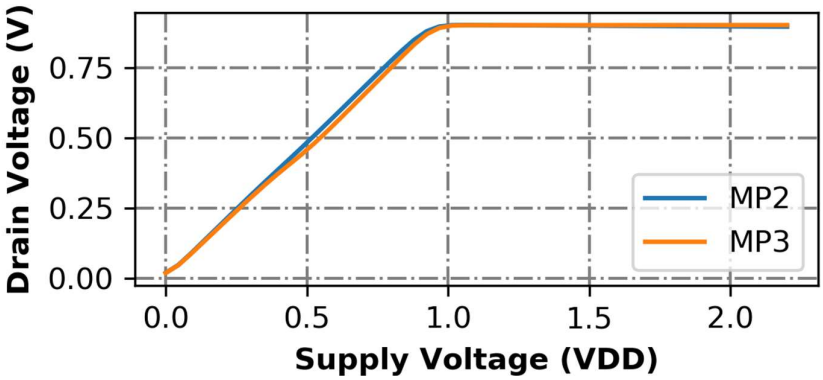

Fig. 4.6. Drain Voltage of MP2 and MP3 vs supply VDD

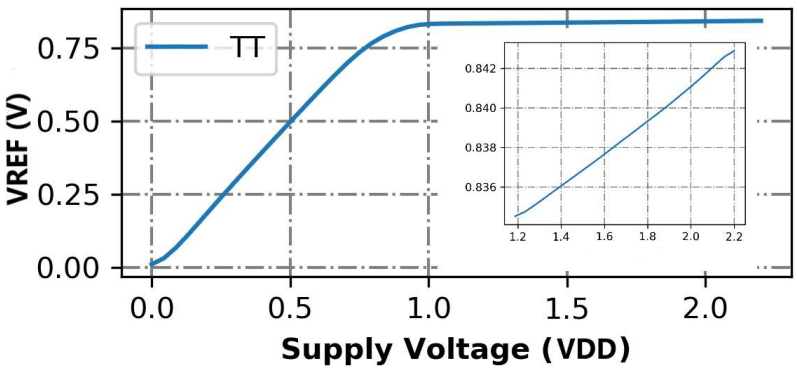

Fig. 4.7. VREF vs supply (VDD)

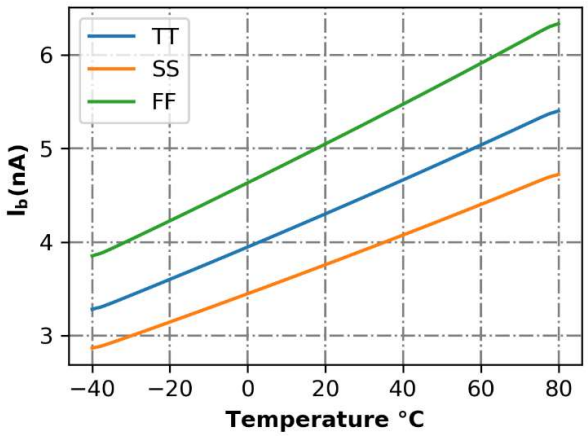

Fig. 4.8. I_b vs Temperature when R is in TT, SS, FF

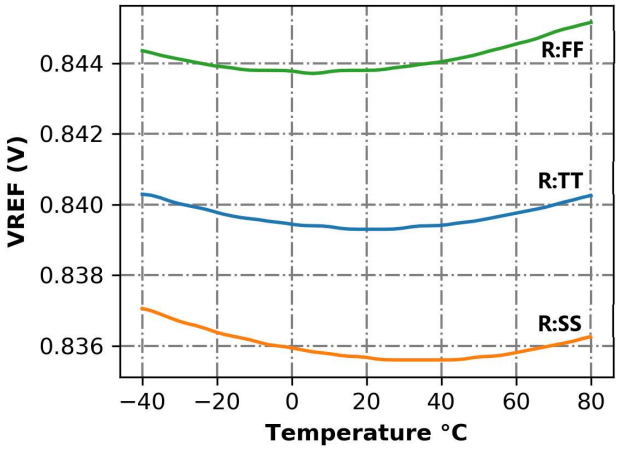

Fig. 4.9. VREF vs Temperature when R is in TT, SS, FF

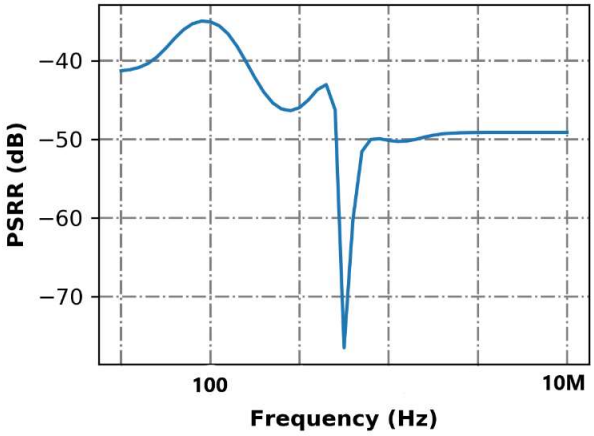

Fig. 4.10. Power Supply Rejection Ratio of VREF

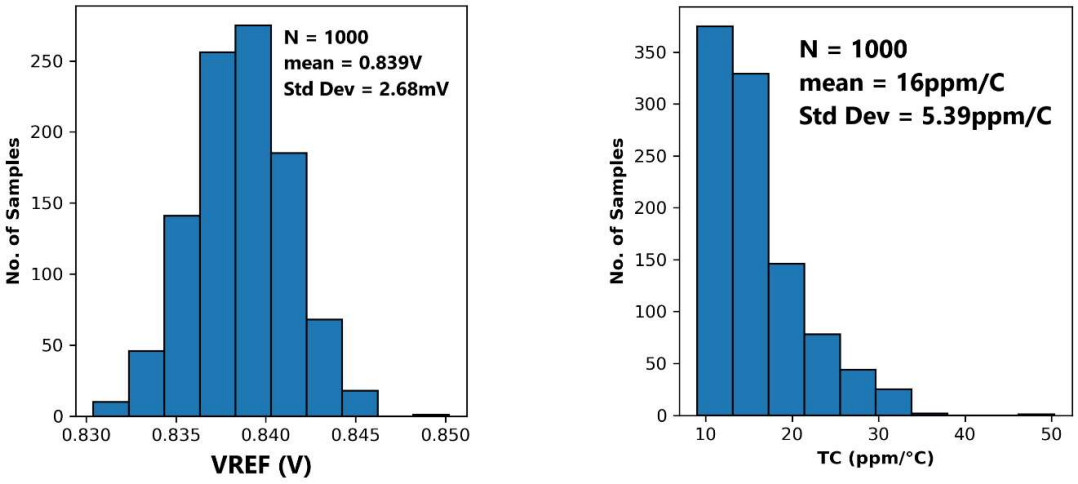

Fig. 4.11. Monte-Carlo simulation for 1000 samples for VREF and TC at 1.8V Supply

4.3 CONCLUSION

A low power sub-BGR without operational amplifier is presented in this chapter. The proposed circuit achieves an average TC of 16 ppm/˚C and a spread (σ/μ) of 0.35% for the reference voltage. A voltage divider is used to reduce the slope of the CTAT voltage, thus, allowing the designer to scale down the bias current to few nanoamps.

CHAPTER 5

VOLTAGE AND CURRENT REFERENCE IN ONE CIRCUIT

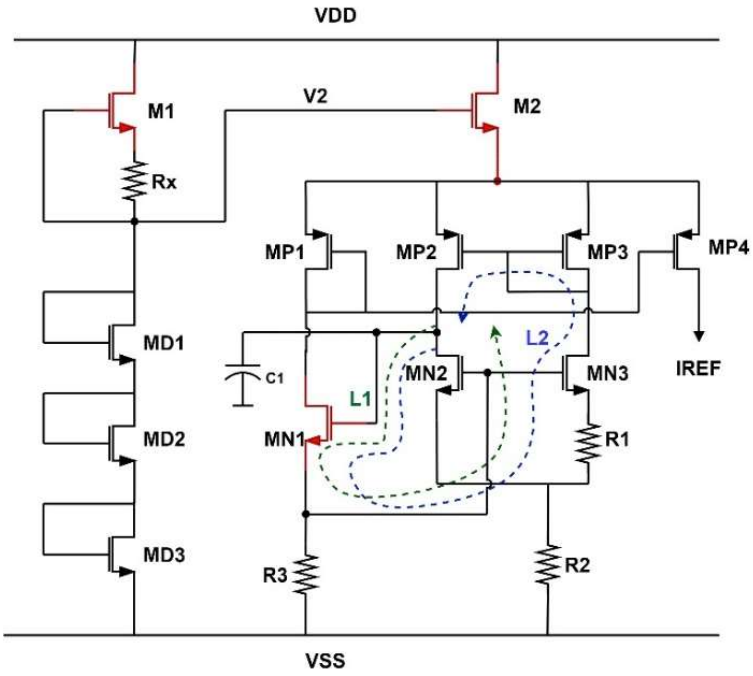

Fig. 5.1. Schematic of the proposed all-in-one reference circuit

The CTAT voltage required for the reference voltage is generated with the gate-source voltage of a MOSFET. To generate the required PTAT voltage, either a NMOS composite pair is used or the $\Delta V_{GS}/R$ PTAT current of a beta- multiplier is allowed to flow through a larger resistor which is a scaled version of the resistor used in the beta-multiplier circuit. Furthermore, there are two mainstream methods to generate a reference current for low power applications. In the first method, an OTA is used to generate a voltage drop across a resistor. In the second method, PTAT currents and CTAT currents are generated separately and then added up to generate a temperature independent current. The former method results in a wider variance of the reference current due to OTA's offset and the latter method is power hungry. The proposed circuit uses the second method to generate the PTAT voltage while avoiding the mentioned mainstream methods of generating the reference current. Instead, the circuit uses a negative feedback loop inside the circuit's core to generate the reference current. Therefore, the reference current achieves low variance and low power operation. For improving the supply regulation, the proposed circuit makes use of native NMOS transistors. One significant benefit of using native MOSFET is its zero-threshold voltage which enables the circuit to always start. The proposed reference circuit (Fig. 5.1) consists of a PSRR enhancement circuit and the reference core. The operating principle of the circuit is explained as follows:

5.1 WORKING OF THE PROPOSED 2-IN-1 VOLTAGE AND CURRENT REFERENCE CIRCUIT

In subthreshold region, a MOSFET can work analogously to a BJT and its current in the subthreshold region is given by:

$$I_D = Is\ (\frac{W}{L})\ exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right)\left\{1 - exp\ \left(\frac{-V_{DS}}{V_T}\right)\right\} \tag{5.1}$$

For $V_{DS} > 4V_T$, I_D is almost independent of V_{DS} and is given by:.

$$I_D = Is\ (\frac{W}{L})\ exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right) \tag{5.2}$$

From (2), gate-source voltage (V_{GS}) can be written as:

$$V_{GS} = V_{th} + \eta V_T\, ln\left(\frac{I_D}{I_S \frac{W}{L}}\right) \tag{5.3}$$

where, $Is = \mu_n(\eta - 1)C_{ox}V_T^2$; V_{th} is the threshold voltage of the transistor which has a CTAT nature, V_T is the thermal voltage , μ_n is mobility, η is the subthreshold slope factor. The proposed voltage reference circuit is a modified Brokaw cell where the BJTs have been replaced with the MOSFETs (MN2 and MN3). All the MOSFETs in the circuit operate in the subthreshold region. From Fig.5.1, the voltage across the resistor R1 is given by:

$$V_{R1} = V_{GS}^{MN2} - V_{GS}^{MN3} \tag{5.4}$$

V_{GS}^{MN2} and V_{GS}^{MN3} are the gate-source voltage of MN2 and MN3. Using (5.3) and (5.4), V_{R1} can be written as:

$$V_{R1} = \eta V_T ln\left(\frac{I_{MN2}\, S_{MN3}}{I_{MN3} S_{MN2}}\right) \tag{5.5}$$

$$V_T = \frac{KT}{q} \tag{5.6}$$

From equation (5.5-5.6) it can be noted that the voltage across the resistor R1 is PTAT in nature. Also, the voltage (V_{R2}) across the resistor R2 can be written as:

$$V_{R2} = 2\,\frac{VR1}{R1}\,R2 \tag{5.7}$$

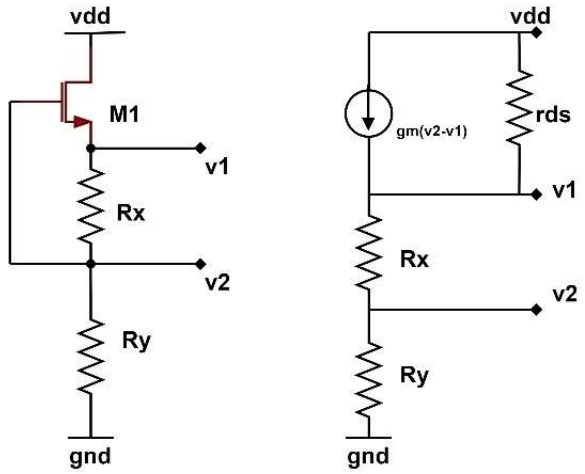

Fig. 5.2. Equivalent small signal circuit for the biasing circuit

The required reference voltage (*VREF)* is the sum of VR2 and the gate-source voltage of the MOSFET MN2. VR2 is PTAT in nature and V_{GS}^{MN2} is CTAT in nature. The size of the resistor R2 is adjusted such that VREF is temperature independent (Fig. 5.3).

The proposed all-in-one reference circuit does not follow the mainstream method of using an OTA to generate the reference current. Instead, it employs a feedback loop consisting of MN1 to drop the reference voltage across a resistor (R3). Such technique is power and area efficient. Furthermore, one can avoid the variation of generated current due to offset which comes with the usage of an OTA. The working of the feedback loops can be explained as follows: the circuit (Fig. 5.2.) consists of a positive feedback loop (L2) and a negative feedback loop (L1). The gain of the positive feedback loop is rather small compared to the gain of the negative feedback loop due to degeneration at the source of MN3. Also, there is only one high impedance node (drain of MN2). Therefore, a small capacitor (C1) at the drain of MN2 is good enough to ensure the stability of the loop.

PSRR is one of the most critical specs for a voltage reference since it provides the reference signal to a low drop-out regulator under which many critical blocks operate in a power management IC. If the supply of the voltage reference is connected directly to the source of MP2 and MP3, any disturbance at the supply will directly affect the reference voltage. Therefore, it is necessary to isolate the supply from the source of PMOS transistors. A native MOSFET (M2) is used to isolate the supply in the proposed architecture.

In our proposed circuit, the gate of the native MOSFET (M2) is biased with an auxiliary circuit consisting of a native MOSFET (M1) and the diode connected devices (MD1-MD3). The native MOSFET M1 acts as a current source when a resistor is connected between its gate and source. The biasing circuit provides a voltage which is equal to $3V_{GS}$. In order for the reference core to have good PSRR, the biasing circuit has to be robust to changes in supply. Since the gate of the MOSFET M1 is isolated from the supply, the biasing circuit has a high PSRR of 50dB. The DC PSRR (ratio of v2 and supply) of the biasing circuit can be derived from its small signal equivalent circuit (Fig. 5.2.) as follows:

$$PSRR = 20\log\left(\frac{R_y}{R_x + R_y + rds + gm*rds*R_x}\right) \tag{5.8}$$

Where, Ry is the resistance offered by the diode connected MOSFETs (MD1-MD3). The primary advantage of using a native device (M2) is that it does not incur the unnecessary gate-source voltage drop like that of a higher threshold voltage device [13]. Therefore, the reference circuit can work closer to the supply. The minimum supply voltage required for proper operation of the proposed circuit can be expressed as:

$$V_{DD,min} \approx V_{REF} + V_{GS} + 2*V_{dsat} \tag{5.9}$$

From equation (5.7), it can be seen that the reference voltage does not vary with mismatch and process variations in the resistors. Furthermore, it can be noted that the reference voltage is a strong function of the gate-source voltage of the MOSFET MN2. Therefore, process variations in the threshold voltage of the MOSFET MN2 introduce

process variations in the reference voltage. Mismatch error in the reference voltage is due to the mismatch in the PMOS current mirrors, which is minimized with choosing large dimensions for the current mirror. The reference current is affected by the process variation in resistor (R3) and the VGS of MN2. A trimming arrangement [4] could be used for the resistor R3 to minimize the spread in the reference current.

5.2 RESULTS AND DISCUSSION

The proposed all-in-one reference is designed in 130nm technology. Monte-Carlo simulation was performed for the proposed circuit to check its robustness with respect to process and mismatch variations. The reference voltage has a mean value of 706.62mV and a spread (sigma/mean) of 1.6% (Fig. 5.5). The reference current has a mean value of 95.74nA and a spread of 3.6% (Fig. 5.6). Furthermore, the reference voltage as an average TC of 100ppm/C and the reference current has an average TC of 108 ppm/C (Fig. 5.7 and Fig. 5.8). The proposed circuit achieves a PSRR of 70dB at DC (Fig. 5.9). The feedback loop is frequency compensated by placing a 1pF capacitor at the high impedance node. The DC loop gain is 35dB and the phase margin for the feedback is 90 degrees (Fig. 5.10.). The branch consisting of MP1 consumes 96nA of current.

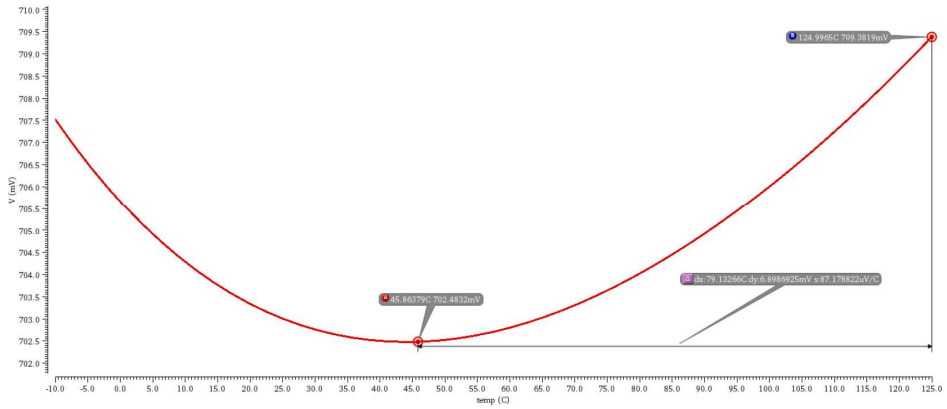

Fig. 5.3. Reference voltage (VREF) across temperature in nominal corner

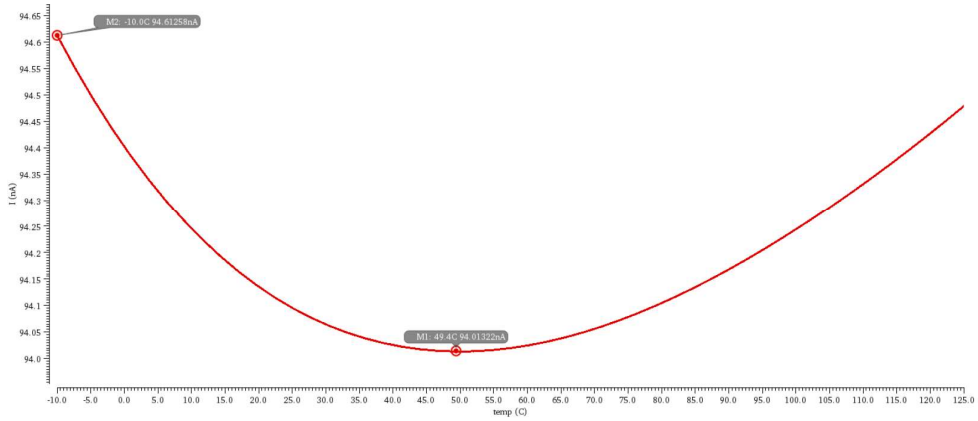

Fig. 5.4. Reference current (IREF) across temperature in nominal corner

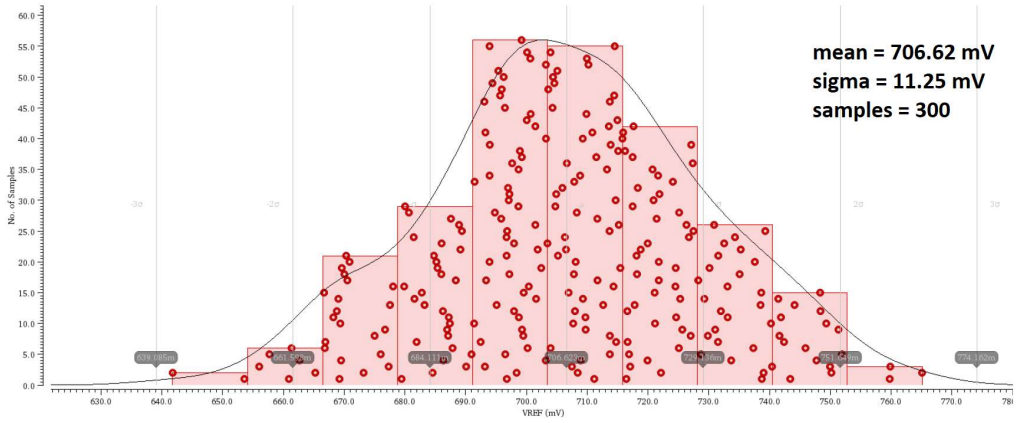

Fig. 5.5. Reference voltage (VREF) as noted in the Monte-Carlo simulations

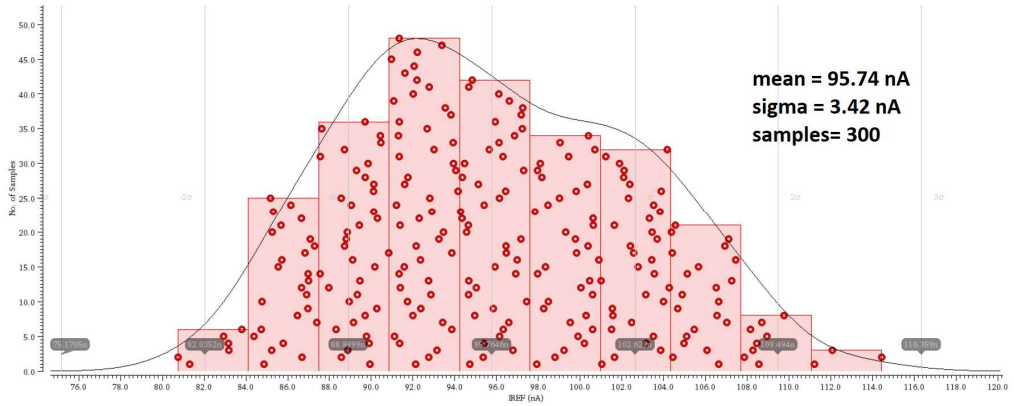

Fig. 5.6. Reference current (VREF) as noted in the Monte-Carlo simulations

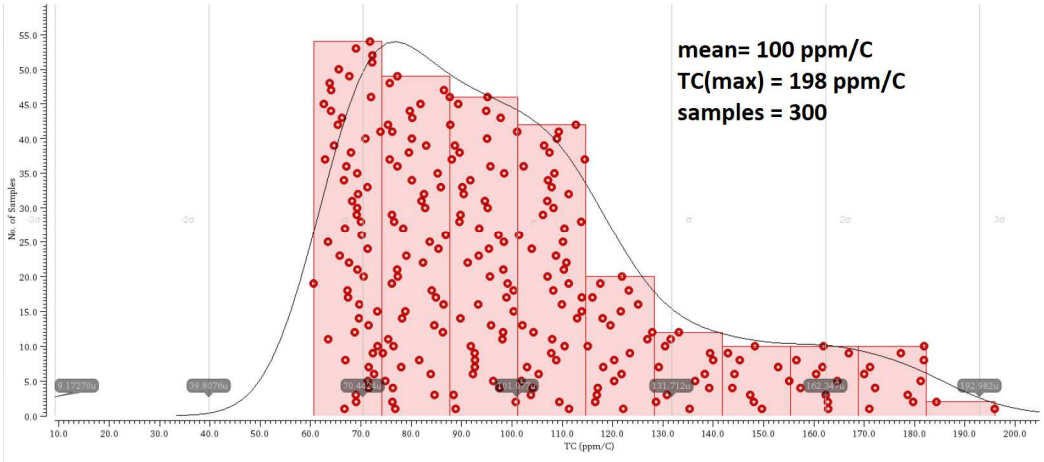

Fig. 5.7. TC of the reference voltage as noted in the Monte-Carlo simulations

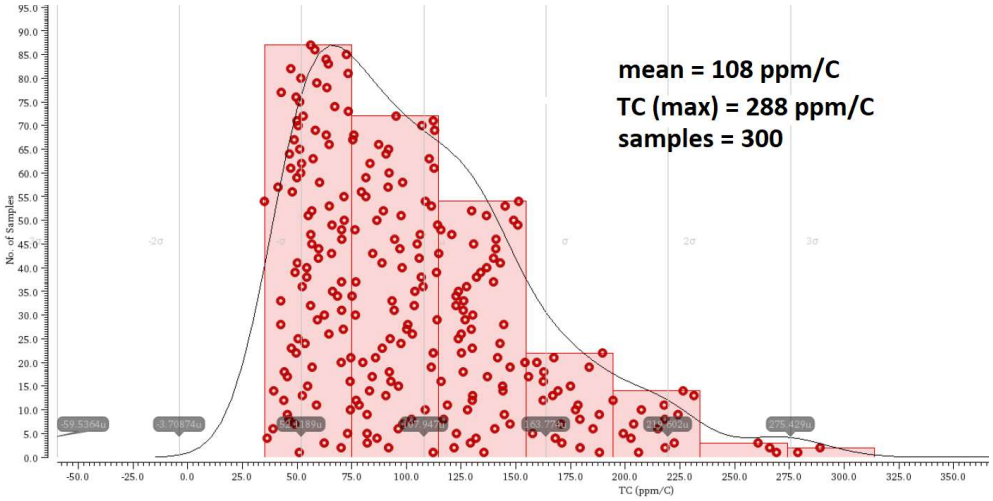

Fig. 5.8. TC of the reference current as noted in the Monte-Carlo simulations

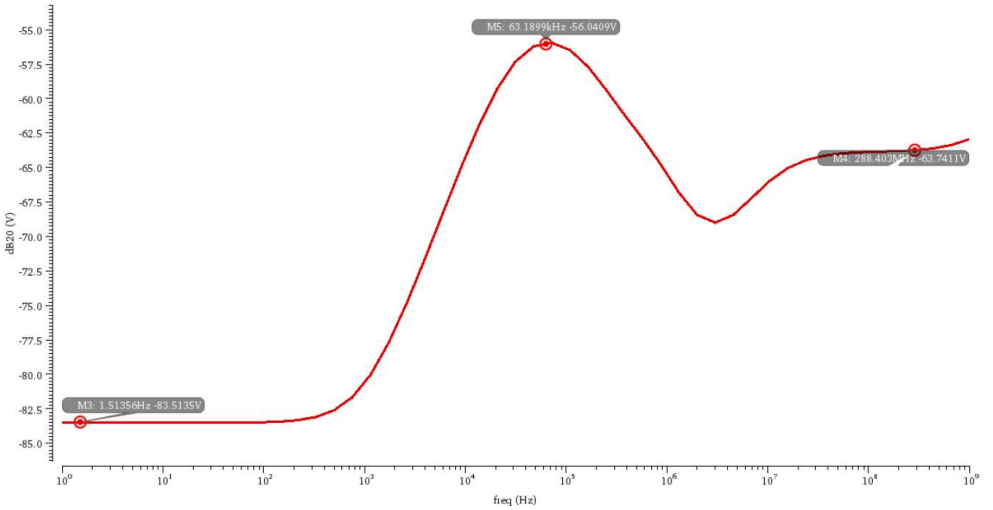

Fig. 5.9. PSRR of the voltage reference as noted in nominal corner

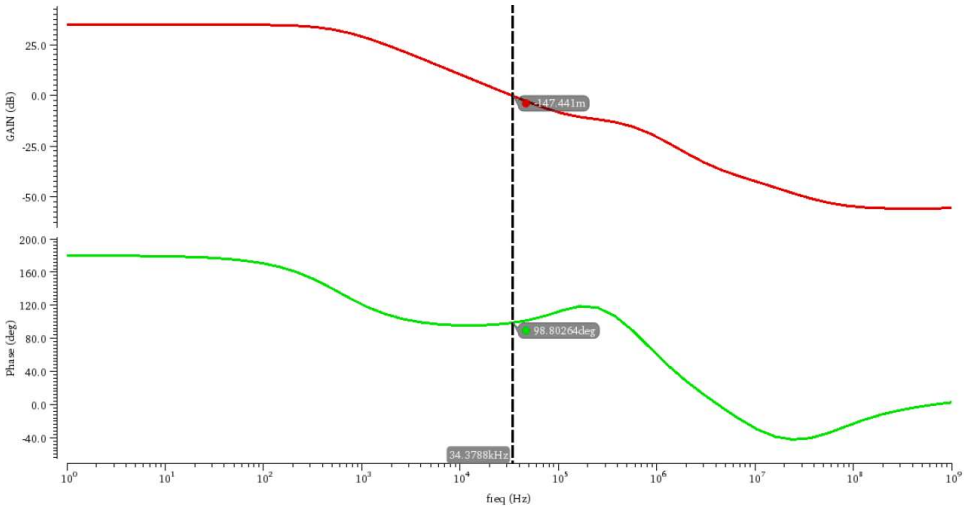

Fig. 5.10. Stability analysis (loop gain and phase of the feedback loop)

5.3 CONCLUSION

An all-in-one current and voltage reference circuit is presented in this chapter which achieves a high PSRR of 83dB at DC. The proposed circuit avoids the usage of OTA. A feedback arrangement is used instead of a traditional OTA to generate the temperature independent reference current. The circuit uses an auxiliary circuit consisting of native MOSFET for isolating the supply from the core. The circuit consumes only 240nW of power at 1.2V supply, therefore, making it suitable for low power applications.

CHAPTER 6

CONCLUSION AND FUTURE WORK

Various types of voltage references such as bandgap references, nano-watt CMOS voltage references, pico-watt voltage references, sub-bandgap references, op-amp free nano-watt voltage references and current references were studied during the architecture survey of the course. Although each type of architecture has its own merits and demerits, the primary focus was to come up with novel architectures which stood out in their respective category. For example, we were able to publish circuits which could operate from sub-1V onwards.

The voltage reference [A], uses all similar Vth MOSFETs, it does not use any op-amp, it does not use any design component other than MOSFETs. The current reference [B] is designed based on a novel method of generating a temperature independent voltage. Furthermore, the current reference work from 0.55V on-wards. A sub-bandgap is also proposed which mitigates the rather low 6-sigma accuracy of [A]. In area critical applications, it is often not possible to have both voltage reference and current reference circuits in the power management. Therefore, keeping this in mind, we were able to integrate the current reference into the voltage reference in the 2-in-1 reference generator circuit.

Future works include improving the accuracy of the published current reference circuit [B]. The proposed 2-in-1 voltage-current reference generator circuit needs 2 trimming arrangements for the reference voltage trimming and the reference current trimming. The voltage reference [A] can be extended into an accurate VCC threshold detection circuit to detect UVLO and POR thresholds during a controller's start-up operation.

RELATED PUBLICATIONS

[A] A. Pathy, B. Adithya and Z. Abbas, "A 0.85V Supply, High PSRR CMOS Voltage Reference without Resistor and Amplifier for Ultra-Low Power Applications," 2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Lansing, MI, USA, 2021, pp. 995-998, doi: 10.1109/MWSCAS47672.2021.9531826.

[B] S. Agarwal, A. Pathy and Z. Abbas, "A 9.5nW, 0.55V Supply, CMOS Current Reference for Low Power Biomedical Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 9, pp. 3650-3654, Sept. 2022, doi: 10.1109/TCSII.2022.3183146.

REFERENCES

[1] A. J. Williams, M. F. Torquato, I. M. Cameron, A. A. Fahmy and J. Sienz, "Survey of Energy Harvesting Technologies for Wireless Sensor Networks," in IEEE Access, vol. 9, pp. 77493-77510, 2021, doi: 10.1109/ACCESS.2021.3083697.
[2] M. Liu, A. van Roermund and P. Harpe, "A 0.9V-VDD sub-nW resistor-less duty-cycled CMOS voltage reference in 65nm for IoT," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, 2017, pp. 1-4, doi: 10.1109/ISCAS.2017.8050287.
[3] A. P. Brokaw, "A simple three-terminal IC bandgap reference," in IEEE Journal of Solid-State Circuits, vol. 9, no. 6, pp. 388-393, Dec. 1974, doi: 10.1109/JSSC.1974.1050532.
[4] L. Wang, C. Zhan, J. Tang, Y. Liu and G. Li, "A 0.9-V 33.7-ppm/°C 85-nW Sub-Bandgap Voltage Reference Consisting of Subthreshold MOSFETs and Single BJT," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 26, no. 10, pp. 2190-2194, Oct. 2018, doi: 10.1109/TVLSI.2018.2836331.
[5] H. Banba et al., "A CMOS bandgap reference circuit with sub-1-V operation," in IEEE Journal of Solid-State Circuits, vol. 34, no. 5, pp. 670-674, May 1999, doi: 10.1109/4.760378.
[6] Nilsson, Joakim & Borg, Johan & Johansson, Jonny. (2017). High-temperature characterisation and analysis of leakage-current-compensated, low-power bandgap temperature sensors. Analog Integrated Circuits and Signal Processing. 93. 10.1007/s10470-017-1011-6.
[7] H. Zhuang, Z. Zhu and Y. Yang, "A 19-nW 0.7-V CMOS Voltage Reference With No Amplifiers and No Clock Circuits," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 61, no. 11, pp. 830-834, Nov. 2014, doi: 10.1109/TCSII.2014.2345298.
[8] K. Ma, Y. Cao and X. Zhao, "A Compact 65nm CMOS Sub-1-V All-MOSFET Voltage Reference with Low Average Temperature Coefficient of 13.9ppm/°C," *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, ON, Canada, 2018, pp. 186-189, doi: 10.1109/MWSCAS.2018.8623908.
[9] K. Ueno, T. Hirose, T. Asai and Y. Amemiya, "A 300 nW, 15 ppm/C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs," in IEEE Journal of Solid-State Circuits, vol. 44, no. 7, pp. 2047-2054, July 2009, doi: 10.1109/JSSC.2009.2021922.
[10] Y. Zeng, X. Zhang and H. Tan, "A 86 nA and sub-1 V CMOS voltage reference without resistors and special devices," *2017 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Abu Dhabi, 2017, pp. 1-5, doi: 10.1109/VLSI-SoC.2017.8203480.
[11] J. Guo et al., "A 70-nA 13-ppm/°C All-MOSFET Voltage Reference for Low-Power IoT Systems," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018, pp. 1-4, doi: 10.1109/ISCAS.2018.8351792.
[12] L. Wang and C. Zhan, "A 0.7-V 28-nW CMOS Subthreshold Voltage and Current Reference in One Simple Circuit," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 9, pp. 3457-3466, Sept. 2019, doi: 10.1109/TCSI.2019.2927240.
[13] C. Huang, C. Zhan, L. He, L. Wang and Y. Nan, "A 0.6-V Minimum-Supply, 23.5 ppm/°C Subthreshold CMOS Voltage Reference With 0.45% Variation Coefficient," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 10, pp. 1290-1294, Oct. 2018, doi: 10.1109/TCSII.2018.2846808.
[14] A. Parisi, A. Finocchiaro, G. Papotto and G. Palmisano, "Nano-Power CMOS Voltage Reference for RF-Powered Systems," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 10, pp. 1425-1429, Oct. 2018, doi: 10.1109/TCSII.2018.2857626.
[15] Z. Zhou *et al*., "A Resistorless Low-Power Voltage Reference," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 7, pp. 613-617, July 2016, doi: 10.1109/TCSII.2016.2530096.
[16] N. Alhassan, Z. Zhou and E. Sánchez-Sinencio, "An All-MOSFET Voltage Reference With −50-dB PSR at 80 MHz for Low-Power SoC Design," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 8, pp. 892-896, Aug. 2017, doi: 10.1109/TCSII.2016.2614527.
[17] M. Seok, G. Kim, D. Blaauw and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2534-2545, Oct. 2012, doi: 10.1109/JSSC.2012.2206683.

[18] F. Olivera, L. S. da Silva and A. Petraglia, "A 120 mV Supply, Triode-Regulated Femto-Watt CMOS Voltage Reference Design," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 2, pp. 587-591, Feb. 2021, doi: 10.1109/TCSII.2020.3046368.
[19] Y. Wang, Q. Sun, H. Luo, X. Wang, R. Zhang and H. Zhang, "A 48 pW, 0.34 V, 0.019%/V Line Sensitivity Self-Biased Subthreshold Voltage Reference With DIBL Effect Compensation," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 2, pp. 611-621, Feb. 2020, doi: 10.1109/TCSI.2019.2946680.
[20] Y. Ji, J. Lee, B. Kim, H. -J. Park and J. -Y. Sim, "A 192-pW Voltage Reference Generating Bandgap–With Process and Temperature Dependence Compensation," in IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3281-3291, Dec. 2019, doi: 10.1109/JSSC.2019.2942356.
[21] Z. -k. Zhou et al., "A CMOS Voltage Reference Based on Mutual Compensation of Vtn and Vtp," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 59, no. 6, pp. 341-345, June 2012, doi: 10.1109/TCSII.2012.2195065.
[22] J. Jiang, W. Shu, J. Chang and J. Liu, "A novel subthreshold voltage reference featuring 17ppm/°C TC within −40°C to 125°C and 75dB PSRR," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), 2015, pp. 501-504, doi: 10.1109/ISCAS.2015.7168680.
[23] D. A. Badillo, "1.5V CMOS current reference with extended temperature operating range," 2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353), Phoenix-Scottsdale, AZ, USA, 2002, pp. III-III, doi: 10.1109/ISCAS.2002.1010194.
[24] Y. Deval, J. Tomas, J. B. Begueret, S. Dugalleix and J. P. Dom, "1-volt ratiometric temperature stable current reference," 1997 IEEE International Symposium on Circuits and Systems (ISCAS), Hong Kong, China, 1997, pp. 1984-1987 vol.3, doi: 10.1109/ISCAS.1997.621542.
[25] M. Radecker, A. Knoll, R. kocaman, V. Buguszewicz and R. Rudolf, "A wide range temperature stable integrated current reference," ESSCIRC 2004 - 29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705), Estoril, Portugal, 2003, pp. 583-586, doi: 10.1109/ESSCIRC.2003.1257202.
[26] C. Wu, W. L. Goh, C. L. Kok, W. Yang and L. Siek, "A low TC, supply independent and process compensated current reference," 2015 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 2015, pp. 1-4, doi: 10.1109/CICC.2015.7338488.
[27] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," in IEEE Journal of Solid-State Circuits, vol. 12, no. 3, pp. 224-231, June 1977, doi: 10.1109/JSSC.1977.1050882.
[28] H. J. Oguey and D. Aebischer, "CMOS current reference without resistance," in IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 1132-1135, July 1997, doi: 10.1109/4.597305.
[29] E. M. Camacho-Galeano, C. Galup-Montoro and M. C. Schneider, "A 2-nW 1.1-V self-biased current reference in CMOS technology," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 52, no. 2, pp. 61-65, Feb. 2005, doi: 10.1109/TCSII.2004.842059.
[30] T. Hirose, Y. Osaki, N. Kuroki and M. Numa, "A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities," 2010 Proceedings of ESSCIRC, Seville, Spain, 2010, pp. 114-117, doi: 10.1109/ESSCIRC.2010.5619819.
[31] G. Giustolisi, G. Palumbo, M. Criscione and F. Cutri, "A low-voltage low-power voltage reference based on subthreshold MOSFETs," in IEEE Journal of Solid-State Circuits, vol. 38, no. 1, pp. 151-154, Jan. 2003, doi: 10.1109/JSSC.2002.806266.
[32] Q. Dong, I. Lee, K. Yang, D. Blaauw and D. Sylvester, "A 1.02nW PMOS-only, trim-free current reference with 282ppm/°C from −40°C to 120°C and 1.6% within-wafer inaccuracy," ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference, Leuven, Belgium, 2017, pp. 19-22, doi: 10.1109/ESSCIRC.2017.8094515.
[33] S. Sengupta, K. Saurabh and P. E. Allen, "A process, voltage, and temperature compensated CMOS constant current reference," 2004 IEEE International Symposium on Circuits and Systems (ISCAS), Vancouver, BC, Canada, 2004, pp. I-I, doi: 10.1109/ISCAS.2004.1328197.
[34] D. Cordova, A. C. de Oliveira, P. Toledo, H. Klimach, S. Bampi and E. Fabris, "A sub-1 V, nanopower, ZTC based zero-VT temperature-compensated current reference," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, 2017, pp. 1-4, doi: 10.1109/ISCAS.2017.8050289.

[35] J. Lee and S. Cho, "A 1.4-µW 24.9-ppm/°C Current Reference With Process-Insensitive Temperature Compensation in 0.18-µm CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2527-2533, Oct. 2012, doi: 10.1109/JSSC.2012.2204475.
[36] B. Kelleci and A. I. Karsilayan, "Low-Voltage Temperature-Independent Current Reference with no External Components," 2007 IEEE International Symposium on Circuits and Systems, New Orleans, LA, USA, 2007, pp. 3836-3839, doi: 10.1109/ISCAS.2007.377875.
[37] G. Serrano and P. Hasler, "A Precision Low-TC Wide-Range CMOS Current Reference," in IEEE Journal of Solid-State Circuits, vol. 43, no. 2, pp. 558-565, Feb. 2008, doi: 10.1109/JSSC.2007.914336.
[38] Y. Wenger and B. Meinerzhagen, "Low-Voltage Current and Voltage Reference Design Based on the MOSFET ZTC Effect," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 9, pp. 3445-3456, Sept. 2019, doi: 10.1109/TCSI.2019.2925266.
[39] L. Wang and C. Zhan, "A 0.7-V 28-nW CMOS Subthreshold Voltage and Current Reference in One Simple Circuit," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 9, pp. 3457-3466, Sept. 2019, doi: 10.1109/TCSI.2019.2927240.
[40] A. Jain, A. Ali, S. Kiran and Z. Abbas, "A High PSRR, Stable CMOS Current Reference using Process Insensitive TC of Resistance for Wide Temperature Applications," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019, pp. 1-5, doi: 10.1109/ISCAS.2019.8702638.
[41] B. B. Yadav, K. Mounika, A. Bathi and Z. Abbas, "67ppm/°C, 66nA PVT Invariant Curvature Compensated Current Reference for Ultra-Low Power Applications," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9180857.
[42] B. -D. Yang, Y. -K. Shin, J. -S. Lee, Y. -K. Lee and K. -C. Ryu, "An accurate current reference using temperature and process compensation current mirror," 2009 IEEE Asian Solid-State Circuits Conference, Taipei, Taiwan, 2009, pp. 241-244, doi: 10.1109/ASSCC.2009.5357223.
[43] E. K. F. Lee, "Low voltage CMOS bandgap references with temperature compensated reference current output," Proceedings of 2010 IEEE International Symposium on Circuits and Systems, Paris, France, 2010, pp. 1643-1646, doi: 10.1109/ISCAS.2010.5537472.
[44] M. Choi, I. Lee, T. -K. Jang, D. Blaauw and D. Sylvester, "A 23pW, 780ppm/°C resistor-less current reference using subthreshold MOSFETs," ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC), Venice Lido, Italy, 2014, pp. 119-122, doi: 10.1109/ESSCIRC.2014.6942036.
[45] K. Kimura, "Low voltage techniques for bias circuits," in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 44, no. 5, pp. 459-465, May 1997, doi: 10.1109/81.572344.
[46] M. S. Eslampanah Sendi, S. Kananian, M. Sharifkhani and A. M. Sodagar, "Temperature Compensation in CMOS Peaking Current References," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 9, pp. 1139-1143, Sept. 2018, doi: 10.1109/TCSII.2018.2805832.
[47] Y. Osaki, T. Hirose, N. Kuroki and M. Numa, "1.2-V Supply, 100-nW, 1.09-V Bandgap and 0.7-V Supply, 52.5-nW, 0.55-V Subbandgap Reference Circuits for Nanowatt CMOS LSIs," in IEEE Journal of Solid-State Circuits, vol. 48, no. 6, pp. 1530-1538, June 2013, doi: 10.1109/JSSC.2013.2252523.