Innovative Design Approaches with Self-Adaptive Methods for Analog and RF Circuits

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fulfillment of the requirements for the degree of

Master of Science

in

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by

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CERTIFICATE

It is certified that the work contained in this thesis, titled "**Innovative Design Approaches with Self-Adaptive Methods for Analog and RF Circuits**" by **Bhartipudi Sahishnavi**, has been carried out under my supervision and is not submitted elsewhere for a degree.

Date

Adviser: Dr. Zia Abbas

To my Family & Friends

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Abstract

In analog and radio frequency (RF) circuit design, innovation is a cornerstone driving progress amid escalating demands for energy efficiency, reliability, and performance optimization. This thesis, titled "Innovative Design Approaches with Self-Adaptive Methods for Analog and RF Circuits," presents a comprehensive exploration of cutting-edge methodologies to revolutionize circuit design paradigms. Divided into two distinct yet interconnected sections, the thesis embarks on a journey through the intricate landscape of analog and RF circuitry.

The first section delves into the intricate art of low-power analog and RF design, driven by the relentless pursuit of energy efficiency. Here, novel architectures, circuit topologies, and optimization techniques have been explored to minimize power consumption while preserving signal integrity and performance metrics. The journey begins with a meticulous investigation into two low-supply 0.5V current/voltage reference designs tailored for ultra-low power IoT and biomedical applications. The first one, designed in CMOS 90nm technology, proposes a current and voltage reference that achieves a typical accuracy of 34.6ppm/$^{\circ}C$ (29.68ppm/$^{\circ}C$) over a wide temperature range of -55°C to 75°C with typical value 63.32pA(0.35V). We observe excellent line sensitivities of 0.0318%/V and 0.0576%/V for voltage and current references in a supply range of 0.5V - 2.3V. The second reference focuses on reducing the power to half compared to the previous one. The design generates reference values of 90.7pA and 288mV, giving an excellent temperature coefficient of 15.2ppm/°C and 36.8ppm/°C for compensated current and voltage values, respectively, at a nominal supply of 0.5V for a wide temperature range of -55°C to 100°C. The circuit

works for a wide voltage range of 0.5V - 2.6V with a supply sensitivity of 0.028%/V and 0.154%/V for current and voltage reference, respectively.

The thesis then introduces a new nW range gate-leakage-based Sub-Bandgap Voltage Reference (SUB-BGR) for low-power, high-temperature IoT applications. Designed in TSMC 65nm technology, the proposed architecture achieves an accuracy of 94ppm/°C. It achieves an excellent line sensitivity of 0.0066%/V for a supply range of 0.7V to 4V and PSRR of 89dB at DC 1V supply.

As the spectrum broadens, the focus shifts to the high-frequency domain, where the work explores the intricacies of on-chip Vector Network Analyzers (VNAs). It introduces a fully integrated low-power, low-area on-chip single-port CMOS VNA, designed explicitly for bio-molecule detection, operating in a tunable frequency range of 0.5GHz to 2.5GHz. This design incorporates innovative features such as an IDC sensor and a high-linearity Low Noise Amplifier (LNA), demonstrating superior performance metrics within a compact footprint.

The process, voltage, and temperature (PVT) variations immensely affect the circuit performance of the Analog and RF circuits. The second section of the thesis delves into self-adaptive methodologies tailored to mitigate variations across PVT, addressing the challenge of ensuring consistent circuit performance. Leveraging adaptive control and feedback mechanisms, self-adaptive loops are developed and implemented in simulation, dynamically adjusting circuit parameters in real-time. For efficient self-adaptation, the information of P, V, and T is necessary to provide accurate real-time feedback, enabling dynamic parameter adjustments in analog and RF circuits.

This thesis significantly contributes to the advancement of analog and RF circuit design methodologies through a synthesis of theoretical analyses, simulation studies, and practical implementations. By embracing innovation and harnessing the power of self-adaptive methods, this research paves the way for a new era of agile, efficient, and resilient analog and RF circuits.

Research Papers for Thesis Work

Conference Papers

1. **Bhartipudi Sahishnavi**, Sampath Kumar, Ashfakh Ali, Arnab Dey, Inhee Lee and Zia Abbas.***"A 0.5V, pico-watt, 0.06%/V / 0.03%/V low supply sensitive current/voltage reference without using amplifiers and resistors"***, *2023 IEEE International Symposium on Circuits and Systems* ***(ISCAS)***, [**Published**]

2. **Bhartipudi Sahishnavi**, Samriddhi Agarwal, Shameer Basha, Naveen Dasari, Andleeb Zahra, Prabhakar Bhimalapuram, Syed Azeemuddin, and Zia Abbas.***"An inductor-less, cost-effective On-chip CMOS VNA for bio-molecule detection"***, *2024 IEEE International Symposium on Circuits and Systems* ***(ISCAS)***, [**Accepted**]

3. Arnab Dey, Bharadwaj Subramaniam, Ashfakh Ali, **Bhartipudi Sahishnavi**, Abhishek Pullela, and Zia Abbas.***"A 2.3nW Gate-Leakage Based Sub-Bandgap Voltage Reference with Line Sensitivity of 0.0066%/V from -40°C to 150°C for Low-Power IoT Systems"***, *2023 IEEE International Symposium on Circuits and Systems* ***(ISCAS)***, [**Published**]

4. Shiva Sharma, Koushik De, **Bhartipudi Sahishnavi**, Khanh M Le, and Zia Abbas.***"Design and Optimization of Robust Process Monitors"***, *2024 IEEE 67th International Midwest Symposium on Circuits and Systems* ***(MWSCAS)***, [**Accepted**]

Journals

1. **Bhartipudi Sahishnavi**, Arnab Dey, Anubhab Banerjee, and Zia Abbas.***"A 275pW, 0.5V Supply insensitive Gate-leakage based Voltage/Current Reference circuit for a wide temperature range of -55 to 100°C without using Amplifiers and Resistors"***, *2024* ***Microelectronics Journal (Elsevier)***,[**Accepted**]

2. **Bhartipudi Sahishnavi**, Deepthi Amuru, Shameer Basha, Deekshith Akula, Khan Lee, and Zia Abbas.***"Self-adaptation of Analog/RF circuits "***, *2024* ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems***,[**Under Review**]

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Chapter 1

Introduction

The history of semiconductors is a fascinating tale that has changed our everyday lives and ushered in a period of unheard technological progress. A semiconductor is fundamentally a substance whose electrical conductivity is between that of an insulator and a conductor. Years of creativity have allowed for the manipulation and harnessing of this seemingly simple notion to create the complex microchips and integrated circuits that power the everyday electronics we depend on. (Fig 1.1)

The birth history of semiconductors can be traced back to the invention of the rectifier (AC-DC converter) in 1874. Many years later, in 1947 Shockley invented the junction transistor and in 1948 Bardeen and Brattain at Bell Laboratories in the US created the point-contact transistor. This announced the beginning of the era of transistors. Vacuum tubes were used in the 1946 computer created by the University of Pennsylvania in the United States. The computer was so big that its vacuum tubes took up the whole building, and it generated a lot of heat and used a lot of electricity. Subsequently, after the invention of the transistor, the ground-breaking transistor calculator (the computer) was created, and even then, computers have advanced exponentially. Shockley, Bardeen, and Brattain shared the 1956 Nobel Prize in Physics in recognition of their contributions to the study of semiconductors and the invention of the transistor.

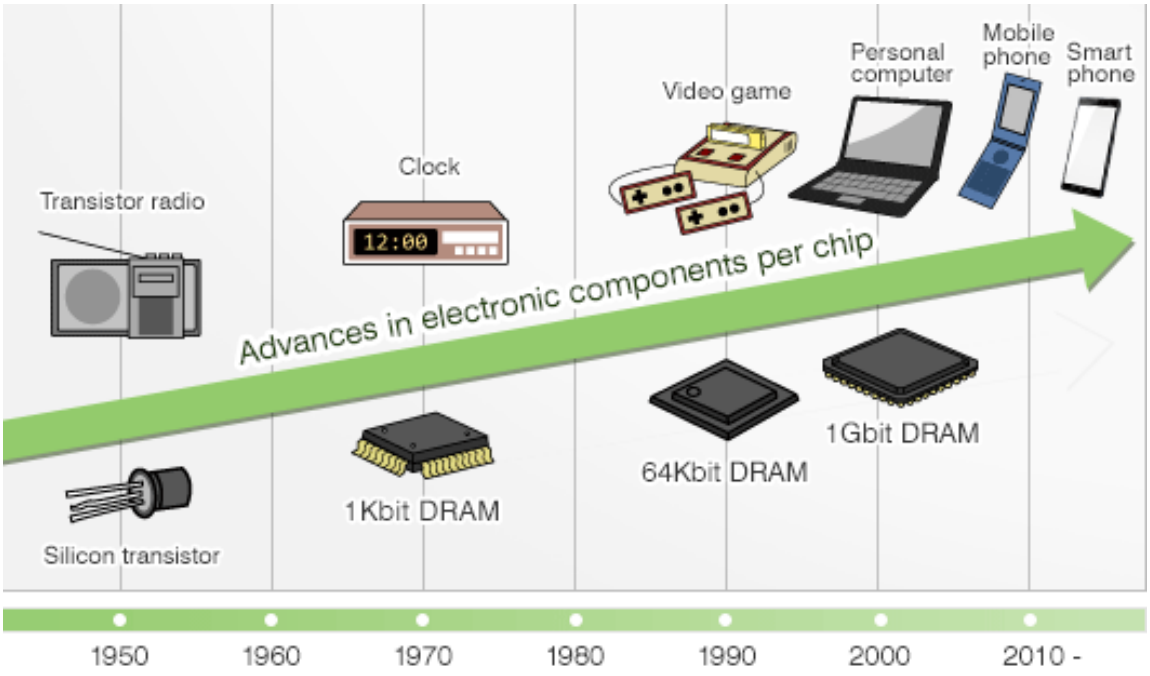


Figure 1.1: Journey of semiconductor[1]

Since the transistor's development, the semiconductor industry has experienced fast expansion. It had already surpassed the 100 million mark in 1957. Kilby of Texas Instruments (US) and Noyce of Fairchild Semiconductor devised the bipolar integrated circuit (IC) in 1959. This innovation signalled the beginning of the IC era and had a significant impact on the history of semiconductors. Due to its tiny size and lightweight, the integrated circuit (IC) was widely utilized in numerous electric products. Texas Instruments used integrated circuits (IC) to create the electronic desktop calculator, or calculator, in 1967. Up to the end of the 1970s, there were intense "calculator wars" amongst electronic equipment makers in Japan as they released calculators one after another. The development of the large-scale integrated circuit (LSI) marked a further advancement in IC integration. The 1980s saw the development of the VLSI (between 100,000 and 10 million electronic components per chip), while the 1990s saw the development of the ULSI (over

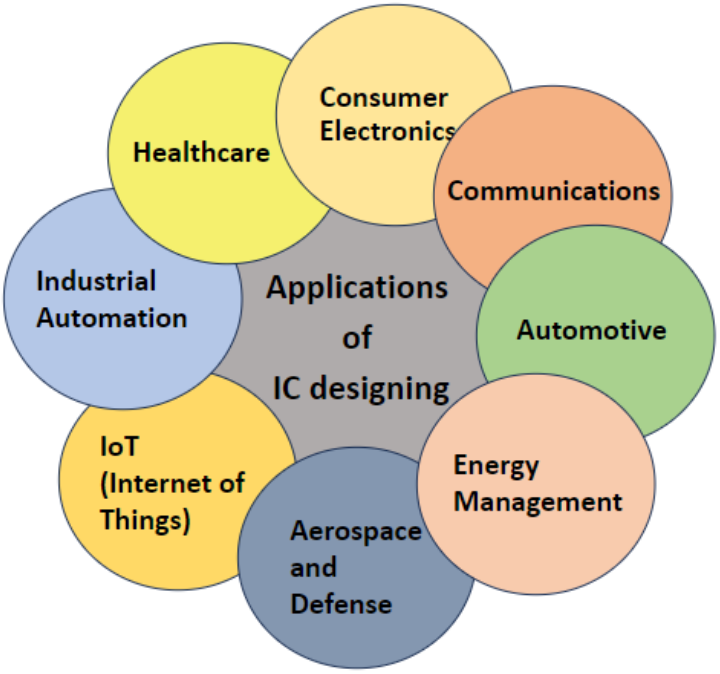


Figure 1.2: Applications of IC designing

10 million electronic components per chip). System LSIs, or multi-function LSIs having several functions integrated into a single chip, were mass-produced in the 2000s. With IC moving towards high performance and multi-functionality, its range of applications is growing. Nowadays, semiconductors are a need for daily living and are employed in every aspect of our civilization.

1.1 Importance of IC Designing

Integrated Circuit (IC) design stands at the forefront of technological innovation, serving as the cornerstone of modern electronic systems across a myriad of applications. As the fundamental building blocks of electronic devices, ICs play a pivotal role in shaping the functionality, performance, and efficiency of everything from consumer electronics to industrial automation and beyond.

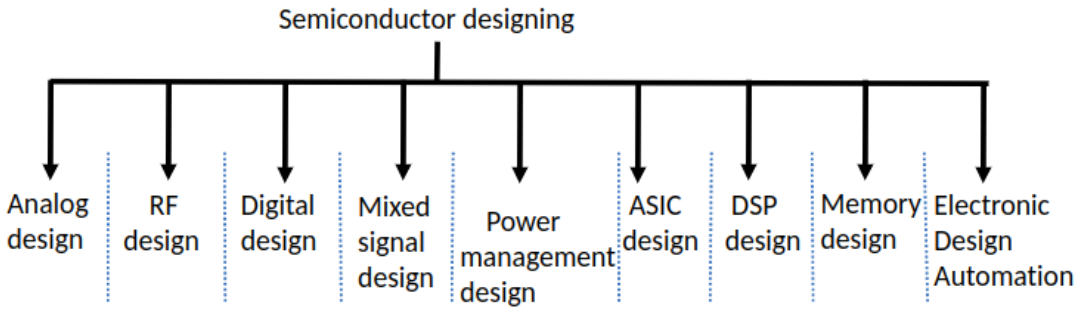


Figure 1.3: Spectrum of Semiconductor designing

The importance of integrated circuit (IC) designing cannot be overstated in today's interconnected world. At the heart of virtually every electronic device, ICs serve as the foundation upon which innovation thrives. From smartphones and computers to medical devices and automotive systems, ICs enable the seamless integration of complex functionalities into compact, efficient, and reliable chips. IC designing not only drives technological progress but also enhances the efficiency, functionality, and connectivity of electronic devices, shaping the way we communicate, work, and interact with the world around us. Moreover, IC design fuels economic growth by stimulating innovation, creating job opportunities, and fostering entrepreneurship in the semiconductor industry. With its pervasive influence across diverse sectors, IC designing stands as a cornerstone of modern civilization, empowering society with the tools and technologies to tackle complex challenges and propel humanity forward into a future of endless possibilities. The major applications of IC design are shown in Fig 1.2.

IC design encompasses a wide range of specialized areas, each focusing on different aspects of electronic circuits and systems. Some of the key areas include(Fig 1.3):

1. ***Analog Design:***

   Description: Involves designing circuits, including amplifiers, filters, and analog-to-digital converters, that process continuous signals.

Applications: Analog circuits are essential for many tasks, such as sensors, communication interfaces, and audio processing.

2. ***Digital Design:***

   Description: focuses on the design of digital circuits, including logic gates, digital processors, and memory circuits, that process discrete binary signals. Applications: Micro-controllers, digital signal processors, and computing systems all depend on digital design.

3. ***RF (Radio Frequency) Design:***

   Description: Specialized area dealing with the design of circuits operating at radio frequencies, commonly used in wireless communication systems.

   Applications: RF design is critical for wireless communication devices, such as mobile phones, Wi-Fi, Bluetooth, and radar systems.

4. ***Mixed-Signal Design:***

   Description: Involves the integration of both analog and digital components on the same chip to handle both continuous and discrete signals.

   Applications: Common in applications like data converters, analog-to-digital/digital-to-analog converters, and sensor interfaces.

5. ***Power Management Design:***

   Description: Focuses on the efficient management and distribution of power within electronic systems.

   Applications: Crucial for mobile devices, battery-powered devices, and energy-efficient electronic systems.

6. ***ASIC (Application-Specific Integrated Circuit) Design:***

   Description: Involves designing custom integrated circuits tailored for specific applications or tasks.

Applications: Used in various industries for specialized tasks, such as image processing, automotive control systems, and networking.

7. ***Memory Design:***

   Description: Focuses on the design of memory circuits, including RAM (Random Access Memory) and non-volatile memory.

   Applications: Essential for storing and retrieving data in electronic systems, ranging from computer memory to flash storage.

8. ***Digital Signal Processing (DSP):***

   Description: Involves the manipulation of digital signals to extract meaningful information or enhance the quality of the signal.

   Applications: Widely used in audio processing, image processing, telecommunications, and control systems.

9. ***EDA (Electronic Design Automation):***

   Description: Encompasses the use of software tools and methodologies to automate the design and verification of electronic systems.

   Applications: EDA tools are used throughout the semiconductor design process, aiding in simulation, synthesis, and layout.

These areas often overlap, and semiconductor designers may specialize in one or more of these domains depending on the specific requirements of their projects. Advances in semiconductor design continue to drive innovation and the development of increasingly complex and sophisticated electronic systems.

1.2 Analog and RF Designing

Analog and RF (Radio Frequency) design stand as pillars of modern electronics, each representing a specialized domain within integrated circuit (IC) design with unique char-

acteristics and applications.[6] Analog design revolves around the processing of continuous signals, such as voltage or current, to perform functions ranging from amplification and filtering to signal conditioning and conversion. In contrast, RF design encompasses circuits operating at high frequencies, enabling wireless communication systems, radar systems, and RF identification (RFID) devices. Together, analog and RF design form the backbone of countless electronic devices, facilitating seamless communication, precise signal processing, and efficient power management. As technology continues to advance, the importance of analog and RF designing only grows, driving innovation and shaping the future of wireless connectivity, sensing, and automation.

The key differences between analog and RF designing:

1. ***Frequency Range:***

   Analog Design: Analog circuits typically operate at frequencies ranging from DC (Direct Current) to a few megahertz (MHz). These circuits are primarily used for processing continuous signals, such as voltage or current, in various applications, including amplification, filtering, and signal conditioning.

   RF Design: RF circuits operate at much higher frequencies, typically ranging from a few megahertz to several gigahertz (GHz). These circuits are specifically designed for wireless communication systems, radar systems, and RF identification (RFID) devices, where high-frequency signal processing is required.

2. ***Signal Characteristics:***

   Analog Design: Analog circuits process continuous signals and are characterized by their linearity, dynamic range, and signal-to-noise ratio (SNR). These circuits focus on preserving the integrity of the analog signal throughout various processing stages.

   RF Design: RF circuits deal with modulated signals and are characterized by their bandwidth, frequency response, and modulation schemes. These circuits are designed

to transmit, receive, and process high-frequency electromagnetic waves efficiently, often using techniques such as impedance matching and frequency conversion.

3. ***Applications:***

   Analog Design: Analog circuits find applications in a wide range of systems, including audio amplifiers, sensor interfaces, power management circuits, and data acquisition systems. These circuits are essential for processing real-world signals and interfacing with the external environment.

   RF Design: RF circuits are primarily used in wireless communication systems, such as cellular networks, Wi-Fi, Bluetooth, and satellite communication. These circuits enable the transmission, reception, and processing of RF signals for voice, data, and multimedia communication over the airwaves.

4. ***Design Challenges:***

   Analog Design: Analog circuits face challenges related to noise, distortion, and nonlinearity, which can degrade signal quality and affect circuit performance. Designers must carefully consider factors such as component matching, thermal stability, and power consumption to achieve desired specifications.

   RF Design: RF circuits face additional challenges due to the high frequencies involved, including signal attenuation, impedance matching, and electromagnetic interference (EMI). Designers must address these challenges while maintaining signal integrity, maximizing efficiency, and complying with regulatory standards.

1.3 Motivation of Self Adaptive Strategy for Designs

The motivation behind developing self-adaptive circuits that are capable of tackling variations in IC design stems from the increasing complexity and variability inherent in modern semiconductor manufacturing processes. These variations can lead to deviations in

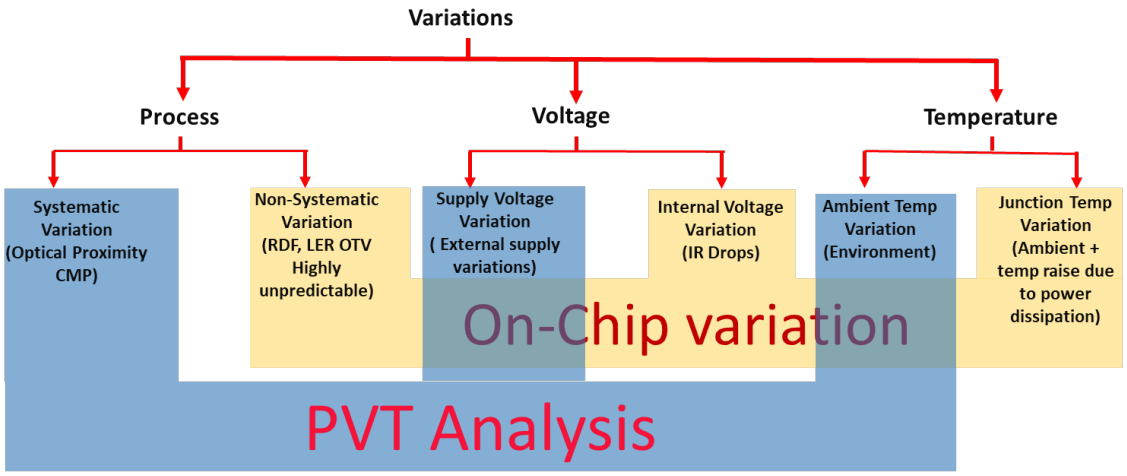


Figure 1.4: Variations after fabrication in IC designing[2]

circuit performance, power consumption, and reliability, ultimately affecting yield, time-to-market, and overall product quality. After fabrication, integrated circuits (ICs) can experience several variations(Fig 1.4), including:

1. ***Process Variations:*** These variations arise from manufacturing processes and result in differences in dimensions, doping concentrations, and material properties across individual devices and circuits. Process variations can lead to deviations in transistor characteristics, such as threshold voltage, mobility, and capacitance, impacting circuit performance, power consumption, and yield.

2. ***Voltage Variations:*** Voltage variations, also known as supply voltage variations, occur due to fluctuations in the power supply voltage delivered to the IC. These variations can stem from power delivery network impedance, load fluctuations, or transient events, leading to changes in transistor operating conditions, timing constraints, and power consumption.

3. ***Temperature Variations:*** Temperature variations refer to changes in ambient or junction temperatures experienced by the IC during operation. Temperature fluctuations can affect device characteristics, such as carrier mobility, threshold voltage, and leakage current, leading to shifts in circuit performance, timing behaviour, and reliability.

4. ***Device Mismatch:*** Device mismatch refers to inherent variations in device parameters, such as threshold voltage, transconductance, and channel length, due to manufacturing tolerances and statistical fluctuations. Device mismatch can introduce uncertainties in circuit behaviour, affecting performance metrics such as gain, linearity, and noise.

5. ***Interconnect Variations:*** Interconnect variations arise from variations in metal layer thickness, width, and spacing, as well as parasitic capacitance and resistance in the metal interconnects. These variations can impact signal propagation delay, crosstalk, and power dissipation in high-speed and high-density ICs.

6. ***Environmental Variations:*** Environmental variations encompass changes in operating conditions, such as humidity, electromagnetic interference (EMI), and radiation exposure, which can affect circuit reliability, noise immunity, and performance degradation over time.

7. ***Aging and Degradation:*** Aging and degradation effects, such as hot carrier injection (HCI), bias temperature instability (BTI), and electromigration (EM), can lead to long-term changes in device characteristics and reliability. These effects can degrade circuit performance, increase leakage currents, and reduce the operational lifespan of the IC.

   The article "Design Challenges in Single Digit Technology Nodes" [3] delves into the escalating significance of process variations and other variations as semiconductor

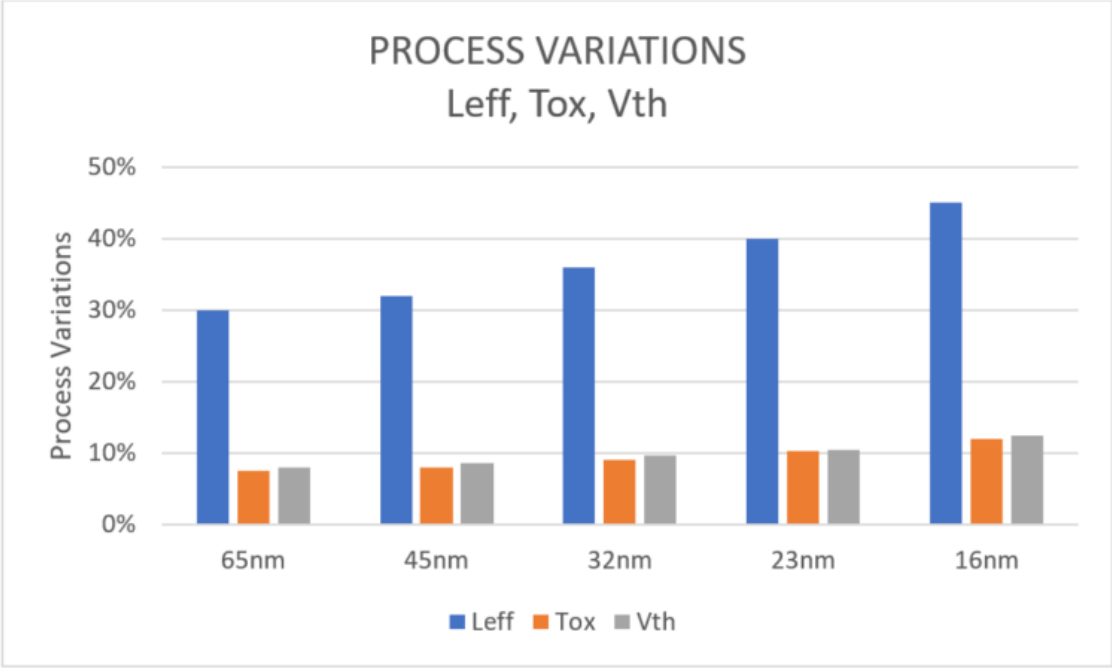


Figure 1.5: Increase in process variation in lower nodes[3]

technology nodes shrink towards single-digit nanometer scales.(Fig 1.5) It underscores the profound impact of advancements in semiconductor manufacturing, particularly in nodes as small as 7nm and beyond, which introduce a myriad of complexities and hurdles in IC design. The article emphasizes the heightened importance of addressing process variability, layout-dependent effects, power consumption constraints, and design rule limitations as technology nodes continue to decrease. It stresses the critical role of innovative design methodologies, such as Design-Technology Co-Optimization (DTCO) and Machine Learning (ML)-driven design, in not only mitigating the adverse effects of variations but also in achieving optimal performance, power efficiency, and yield in next-generation integrated circuits.

1.4 Thesis Organisation

The following manuscript presents the design-level works justifying its title. The thesis consists of two parts. Part 1, "Novel Design Approaches", starts with designing basic reference circuits for advanced applications in Chapter 2 and expands to high-frequency RF design (Chapter 3). Part 2, "Self Adaptive Methodology for PVT variations", embraces the fusion of Machine learning in self-adapting the circuits for tackling post-fabrication variation (Chapter 4) and the novel design of the PVT sensor for the above (Chapter 5). Chapter 6 provides the conclusion and gives the Future scope.

In Chapter 2, we propose three Low-power Analog reference designs. The first design is a 0.5V supply, gate leakage-based current/voltage reference for ultra-low power IoT and biomedical applications implemented in CMOS 90nm technology. The first current (voltage) reference achieves a typical accuracy of 34.6ppm/$^{\circ}C$ (29.68ppm/$^{\circ}C$) over a temperature range of -55°C to 75°C with typical value 63.32pA(0.35V). Excellent line sensitivity of 0.0318%/V and 0.0576%/V are observed for voltage and current reference in a supply range of 0.5V - 2.3V. The second design gives reference values of 90.7pA and 288V. It works for a wide voltage range of 0.5V - 2.6V with a supply sensitivity of 0.028%/V and 0.154%/V for current and voltage reference, respectively. The entire circuit takes a power of 275.36pW at nominal conditions. The design gives an excellent temperature coefficient of 15.2ppm/°C and 36.8ppm/°C for compensated current and voltage values, respectively, at a nominal supply of 0.5V for a wide temperature range of -55°C to 100°C.

In our final design, we introduce a Sub-Bandgap Voltage Reference (SUB-BGR) utilizing gate-leakage characteristics within an nW range. This reference voltage source, designed for high-temperature IoT applications with low power consumption, delivers a stable 336mV output without the need for high-value resistors. Operating efficiently across a wide temperature span from -40°C to 150°C, our circuit exhibits only a modest 9.2-fold increase in power consumption within the upper-temperature range, a notable improvement compared to conventional SUB-BGRs. Fabricated using TSMC 65nm technology, our design

boasts a temperature coefficient accuracy of 94ppm/°C. It also demonstrates exceptional line sensitivity of 0.0066%/V over a supply range of 0.7V to 4V, accompanied by a high power supply rejection ratio (PSRR) of 89dB at DC and a 1V supply. Our proposed approach offers robustness against process variations, with a $\pm 3\sigma$ inaccuracy of 4.305% without requiring any trimming. Occupying a mere 0.008mm^2 area, the circuit operates at an ultra-low power consumption level, drawing only 2.36nW at 27°C and 21.74nW at 150°C with a 0.7V supply.

Chapter 3 presents a fully integrated low-power area on-chip single port CMOS VNA (Vector Network Analyser) designed in 65nm CMOS technology to detect the biomolecule. The proposed design works in a tunable frequency range of 0.5GHz to 2.5GHz, ensuring much higher precision than the VNA working at a higher frequency range. An IDC sensor has introduced a fully integrated architecture for detecting S_{11} of the bio-molecules. A resistive bridge coupler is used for wideband operation with a directivity of 14.89dB up to 2.5GHz. Also, a high-linearity LNA (low noise amplifier) is designed with a linearity of -13dB and a gain of 14 dB. The LNA has a low NF of 3.21dB. The design occupies an active area of $0.01767mm^2$ and consumes power of 41mW from a 1 V supply.

Chapter 4 presents a complete self-adaptive technique using Machine learning, showing the entire loop using Python and skill scripting. The technique is demonstrated in three designs: High-frequency low-noise Amplifier, Transmitter block and VCO.

Finally, in Chapter 5, we conclude the works with an insight into future improvements and scope.

Part- I

Novel Designs Approaches

Chapter 2

Low Power Analog Reference Circuits

2.1 Introduction

Low-power reference circuits are indispensable elements in modern integrated circuit (IC) design, playing a pivotal role across a spectrum of applications. Their significance lies in their ability to optimize energy consumption, particularly in today's energy-conscious environment, where reducing power usage is paramount for extending battery life, minimizing operating costs, and reducing environmental impact. These circuits provide a foundational framework for designing energy-efficient systems, serving as benchmarks for power consumption optimization throughout the entire IC. With the prevalence of battery-powered devices such as smartphones, wearables, and IoT gadgets, low-power reference circuits enable the development of energy-efficient electronics, ensuring prolonged battery life and enhancing user experience by minimizing the need for frequent recharges. Moreover, in the realm of high-density integration, as semiconductor technologies progress and IC integration density increases, low-power reference circuits become essential for maintaining acceptable power budgets, preventing thermal issues, and ensuring reliable operation in densely-packed semiconductor devices. Additionally, they play a critical role in enabling the design of ultra-low-power electronics for IoT devices and wearables, where seamless connectivity and prolonged device lifespans are paramount. Beyond consumer electron-

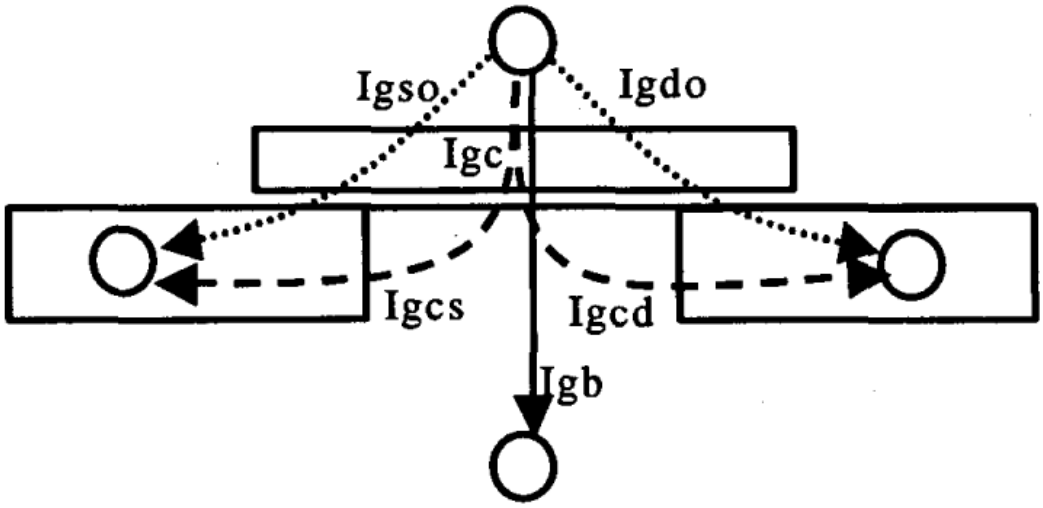


Figure 2.1: Components of gate leakage transistor [4]

ics, low-power reference circuits contribute to green computing initiatives by facilitating the design of energy-efficient processors, memory modules, and communication interfaces, thus reducing energy consumption and environmental impact in data centres and cloud computing infrastructure. Finally, these circuits meet regulatory compliance by providing efficient power management solutions that adhere to industry-standard power consumption specifications. Overall, the importance of low-power reference circuits continues to grow as energy efficiency becomes increasingly critical in the design of electronic systems. The paper [7] shows gate leakage current increases as we scale to lower technology nodes. This gate leakage is properly mathematically characterised in [4]. Using gate leakage transistors for low-power designing in low-technology nodes represents a strategic approach to mitigating power consumption challenges inherent in advanced semiconductor processes. There are many [8] circuits that take advantage of gate leakage to achieve low power.

The ***temperature variation of gate leakage current*** is a critical factor to consider when designing current references, particularly as semiconductor technologies advance and gate oxide thickness decreases. When the gate oxide thickness is reduced below 3nm,

carrier direct tunnelling between the gate and the silicon beneath becomes significant, leading to a leakage current flowing through the transistor's gate. This leakage current, which can range from picoamps to nanoamps, must be carefully analyzed, especially in lower technology nodes such as 130nm, 90nm, 65nm, or 55nm.

Fig 2.1 illustrates the various components of gate leakage current, including gate-to-substrate current (Igb), gate-to-channel current (Igc), which further partitions into Igcs and Igcd, and gate-to-source/drain currents (Igs and Igd).

The expressions for these components of gate leakage current vary depending on the transistor's operating region. In bulk technologies, the gate-to-substrate current is significantly lower than gate-to-channel and gate-to-source/drain currents and is often neglected. Similarly, the contribution of gate-to-source/drain currents (Igs and Igd) to total gate leakage is typically less than 3% and can also be neglected in most cases. The gate leakage tunnelling current expressions for accumulation and inversion region are observed in [9, 10] respectively. The gate leakage current in accumulation mode is approximated as below in [9]:

$$I_{gc} = K * K_2 * V_{gs} * (V_{gs} - V_{th}) * (1 + \alpha V_{oxdepinv}) \tag{2.1}$$

The gate leakage current in inversion mode is approximated as below in [10]:

$$I_{gc} = K * V_{gs} * (V_{gs} - K_1) \tag{2.2}$$

where K, K_1, K_2 are temperature independent terms. $V_{oxdepinv}$ is the voltage across the gate oxide in the depletion/inversion region whose accurate prediction of characteristics is difficult. So, using gate leakage in the ***accumulation region has some advantages*** as its temperature nature only depends upon the characteristics of Vgs. This chapter explains three novel low-power Reference analog designs using gate leakage transistors.

2.2 A 0.5V, pico-watt, 0.06%/V / 0.03%/V Low Supply Sensitive Current/Voltage Reference Without Using Amplifiers and Resistors

2.2.1 Introduction

The increasing demand for IoT in various fields like biomedical, agriculture, wearable, and automobile requires much more advanced electronic designs to meet the specifications. Most of these applications use references to power them. For better power management in this world of mos scaling, the necessity for Sub 1-V Ultra-low-power circuit designs is escalating rapidly. Both Current and Voltage reference blocks at the pico ampere level play a crucial role in ultra-low power IoT sensing applications. It is advantageous, concerning the area and power to have both references in a single block.

Voltage references are commonly realized using BJTs and are termed bandgap references (BGR) [11] [12] [13] [14]. Although such reference voltage in BGRs is highly resilient to process, supply, and temperature (PVT) variations, their power consumption is in the order of µW and nW. Most of these designs use a supply voltage greater than 0.5V. For ensuring low supply voltages, voltage references are designed by exploiting a basic 2T transistor model that relies on Vth subtraction of different thickness MOSFETs [15]. In the design [16], a novel paralleled 2-transistor structure was used for reference voltage generation, and an auxiliary amplifier was used to decrease the Line Sensitivity and PSRR. But usage of resistors increased their power consumption to nW, and usage of amplifiers demands capacitors for stability purposes that increase area. Although the design works at a minimum supply of 0.5V the line sensitivity of 0.3%/V is quite high for a voltage reference. The reference [17][18][19][20], uses additional bulk voltage for Vth compensation that helps in avoiding the usage of amplifiers and resistors. All these references work at a supply of 0.5V. Designs [17][18] require to access the internal body nodes of deep n-well MOSFETs which might not be feasible in all cases. Design [19][20] uses a current subtraction circuit

for body bias which helped them to reduce line sensitivity but the power consumption increased to nW.

Current references are conventionally variants of the beta multiplier or generated based on the V/R principle using Op-amp and cancelling the temperature coefficients of voltage and resistors [21][22][23]. Such resistor-based designs are unsuitable for pW applications and consume a large area. Design [9] exploits beta multiplier architecture and Vth compensation to achieve the specifications. Native oxide is used for Vth compensation and to reduce the line sensitivity, but that has increased the supply voltage greater than 1V. Another common approach is using a 2-T transistor and an Op-Amp as a buffer to obtain a reference current[24]. Design [24] works at a supply of 0.5V but usage of sub-threshold leakage limited the design to work at negative temperature and even the line sensitivity of 0.95%/V is huge for current reference. Op Amps can be designed at 0.5V supply [25][26] but they raise stability issues demanding capacitors. Designs [27][28] don't include Native oxides, amplifiers, and resistors but their temperature range is limited because of sub-threshold leakage and their Line sensitivities are high. References [29, 30, 31, 32, 10] depicts designs of current and voltage reference in a single circuit. The designs [29]-[30] use amplifiers and resistors in their designs. Designs [31]-[32] avoid the usage of amplifiers but their power consumption is nW and the supply voltage greater than 0.5V. Design[10] is a pico-W design but uses native oxide and works for higher supply voltage.

This paper presents a pico-watt current/ voltage reference for a lower supply voltage of 0.5V and a wide voltage range of 0.5-2.3V. The design avoids the usage of amplifiers, resistors, and Native devices. To the author's knowledge, the line sensitivity(even in the worst case) obtained is better than the corresponding designs working at 0.5V supply voltage and works for a practical temperature range of -55^oC to 75^oC.

The rest of the section is organized as follows. Section 2.2.2 deals with the design and analysis of the proposed circuit. Section 2.2.3 explains the trimming procedure used. Section 2.2.4 presents the results of the references, and section 2.2.5 concludes the paper.

2.2.2 Design and Analysis of the Circuit

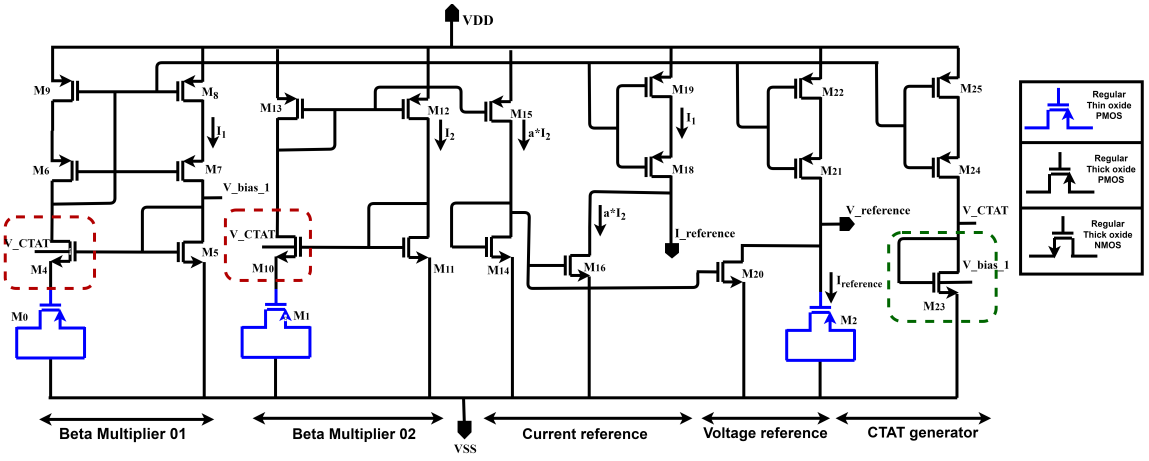


Figure 2.2: Proposed Voltage/Current reference

The transistor-level schematic of the proposed circuit is shown in Fig 2.2. It has been shown that gate leakage transistors can replace resistors for low-power pW circuits(reference), but we can see that the tunnelling currents show variations in temperature, demanding a CTAT voltage at its gate for compensation. In [9], they used the Vth compensation technique to generate a CTAT for which native oxide was used. Native oxides cannot be used for low supply voltage designing as the Vth difference of native oxide and corresponding thick oxide will be more than 0.5V. Therefore, we are exploiting the body voltage for a compensated voltage at the gate terminal of the gate leakage transistor, and the gate leakage is chosen such that its variation with temperature is extremely minimal. Fig 2.3b shows the gate leakage characteristics. The temperature range is limited to 75^oC because body leakage becomes unavoidable at higher temperatures, as shown in 2.3c. To attain proper line sensitivity for the reference current, two temperature-compensated currents are subtracted to cancel out their supply dependency. Hence, two beta multiplier circuits are designed, each giving temperature-compensated current. A CTAT generator is designed to generate a CTAT voltage at the body of NMOS in a Beta multiplier to obtain

the compensated current. The following subsections give a detailed explanation of each block.

2.2.2.1 Beta Multiplier

Beta multiplier circuits use gate leakage transistors whose characteristics are similar to temperature-compensated resistors. Compensated current is obtained by generating a compensated voltage Vcomp at the gate terminal of the leakage transistor by giving a CTAT at the body of its NMOS. The equations of the compensated Voltage are given as

$$V_{comp} = V_{gs1} - V_{gs2} \tag{2.3}$$

$$I_1 = \frac{(V_{gs1} - V_{gs2})}{R} \tag{2.4}$$

where R is the resistance offered by gate leakage which is constant with temperature(Fig 2.3b).

$$I_1 = \frac{(V_{th_1} - V_{th_2} + mV_T ln(\frac{(w/l)_2}{(w/l)_1}))}{R} \tag{2.5}$$

$$V_{th_1} = V_{th_0} \tag{2.6}$$

$$V_{th_2} = V_{th_0} + \gamma \cdot \left(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right) \tag{2.7}$$

by properly adjusting the ratio of w/l and by giving proper CTAT at the body of the NMOS we can make the numerator of (2.5) temperature compensated. The second Beta multiplier is also designed in the same manner except the lengths of NMOS are reduced and a simple current mirror is used to increase its supply dependency. The reason for the above is discussed in the current reference session.

2.2.2.2 CTAT Generator

The CTAT generator uses the concept that Vgs of diode connected NMOS is a CTAT when a constant current flows across it. The equation of CTAT is

$$V_{gs} = V_{th0} + mV_T ln(\frac{Io}{UnCox(w/l)(m-1){V_T}^2}) \tag{2.8}$$

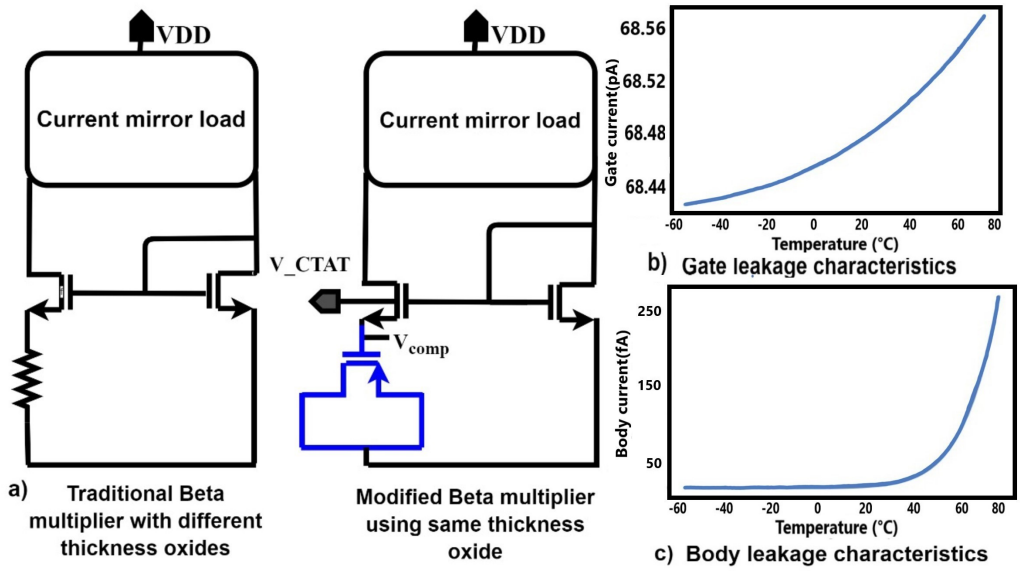


Figure 2.3: a) The beta multiplier circuit b) Gate leakage Characteristic c) Body leakage characteristic

The slope of such CTAT generated will be more than 1m. To reduce its CTAT nature, another CTAT is given to its body. To avoid additional circuitry, the extra CTAT is taken from the Beta multiplier. The beta multiplier circuits are designed in such a way that both use the same CTAT generator for their compensation process. After the addition of CTAT to the body the final Vgs equation will be

$$V_{gs} = V_{th0} - \gamma \cdot \left(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right) + mV_T ln(\frac{Io}{UnCox(w/l)(m-1){V_T}^2})$$

2.2.2.3 Current Reference

The reference current is generated by subtracting two temperature-compensated currents (I1, I2) obtained by two beta multipliers. Subtraction is done to omit the supply

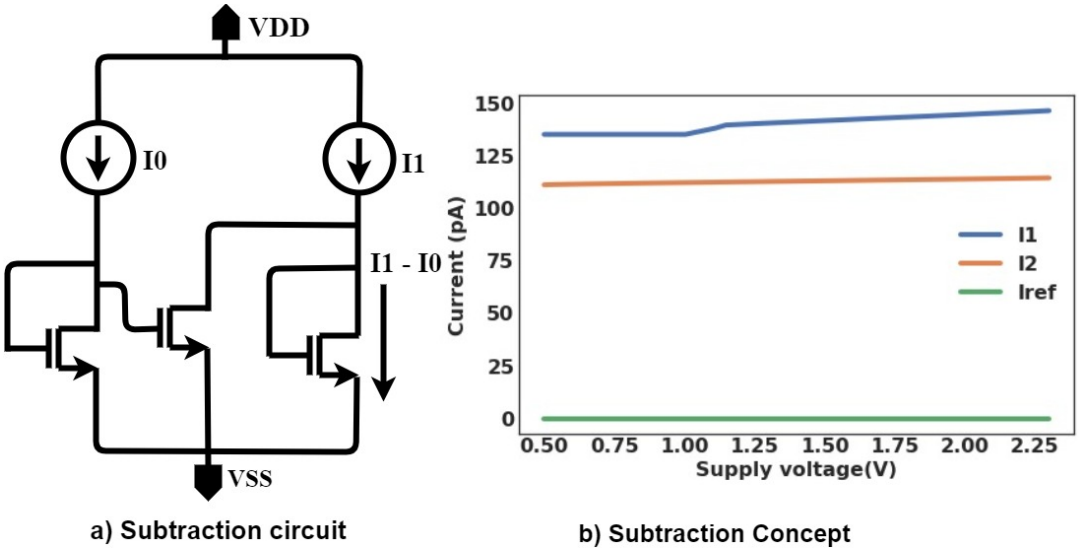


Figure 2.4: Subtraction circuit for line sensitivity improvement

dependency. The equation is shown

$$I_{ref} = I_1 - a * I_2 \tag{2.9}$$

Since the two currents are temperature-compensated, the resultant reference current will also be temperature-compensated. The line sensitivity of the reference current is ensured by properly selecting the coefficient of subtraction 'a' of the currents. The variation of I2 is designed to be more than I1 by reducing the lengths of NMOS and by changing the current mirror architecture. More variation of I2 with supply is necessary to have 'a' less than 1. 'a' greater than 1 will reduce our reference current to much smaller values. The coefficient is chosen such that the effective variation of reference current is much less to supply. Fig 2.4 shows the variation of currents of beta multipliers for supply. We can approximate the current equations as:

$$I_1 = s_1 * V + c_1 \tag{2.10}$$

$$I_2 = s_2 * V + c_2 \tag{2.11}$$

$$I_{ref} = I_1 - a * I_2 = (s_1 - a * s_2) * V + (c_1 - a * c_2) \tag{2.12}$$

'a' is chosen such that s1 - a*s2 becomes zero.

2.2.2.4 Voltage Reference

The reference voltage is obtained by sending the reference current through a gate leakage transistor (selected in such a way that it acts almost as an ideal resistor with an extremely small temperature variation). Using the leakages used are of the same type to avoid process variation.

2.2.3 Trimming

Gate leakage-based current references are usually more sensitive to process variations. Thus, a trimming circuit is essential to control the variation. The usage of 3 gate leakage transistors increases the complexity and size of trimming circuits. It is observed that the multiplier of the transistors should vary in a ratio to reduce the variation. To ensure compact trimming and to reduce the trim bits we rely on simultaneous trimming of all the gate leakage transistors using one set of trim bits. The multipliers of gate leakage transistors of beta multipliers 1 and 2 are in a ratio of 2:3. By using a 5-bit trimming all the gate leakages are simultaneously trimmed. The trimming circuitry is shown in Fig 2.5.

2.2.4 Results and Discussion

The proposed voltage/current reference is implemented in a 90nm technology. The accuracies of the compensated current and voltage curves are shown in Fig 2.6a and the values are observed to be 34.53ppm/°C and 29.6ppm/°C, respectively for a temperature range of -55 to 75 °C.

From the above results, we can find the current and voltage nominal values as 63.3pA and 0.35V, respectively. Fig 2.6b. shows the supply sensitivity of the reference curves which are found to be 0.06%/V (0.031%/V) for current(voltage) curves. The worst corner line sensitivity is 0.362%/V (0.173%/V) for current(voltage)(Fig 2.6d.) is much less than

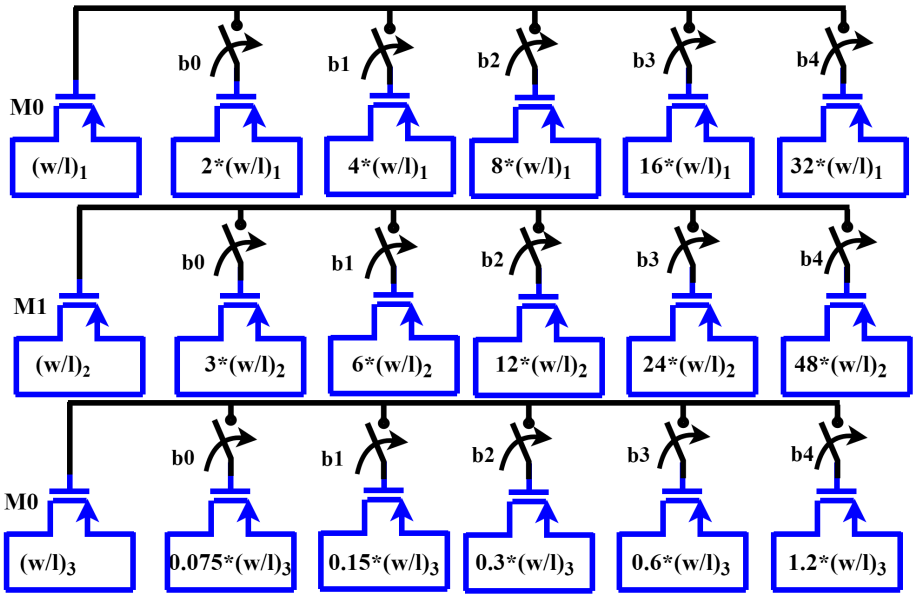


Figure 2.5: Gate leakage transistor trimming circuitry

the line sensitivities of corresponding current reference papers at 0.5V to the author's best knowledge. Fig 2.7 shows the variation for 1000 samples. From Fig 2.7a. and b. the current reference value has a mean(μ) of 66.2pA and variation(σ) of 20pA without trimming that can be effectively reduced to 2pA with trimming. In Fig 2.7c., the 3σ variation of voltage reference is 0.046V, and the mean is 0.354V having 13% of variation with worst case temperature coefficient of 150ppm/°C at nominal conditions. The design consumes 415pW of power and has a voltage reference PSRR of -59.218dB@DC.The start-up time for the current (voltage) reference is 2.79ms(2.58ms). The layout of the proposed design is shown in Fig 2.8 which occupies an area of $0.0096mm^2$.

Table 2.1 summarizes the circuit's performance with the corresponding reference designs. Most of the voltage/current reference circuits like [29, 33, 34], consume nW power with a supply much greater than 0.5V and also use amplifiers. Although the reference [10] consumes pW power, its supply voltage is 1V and uses native oxide devices. When compared to the voltage reference designs [18, 19] that work on supply voltages less than

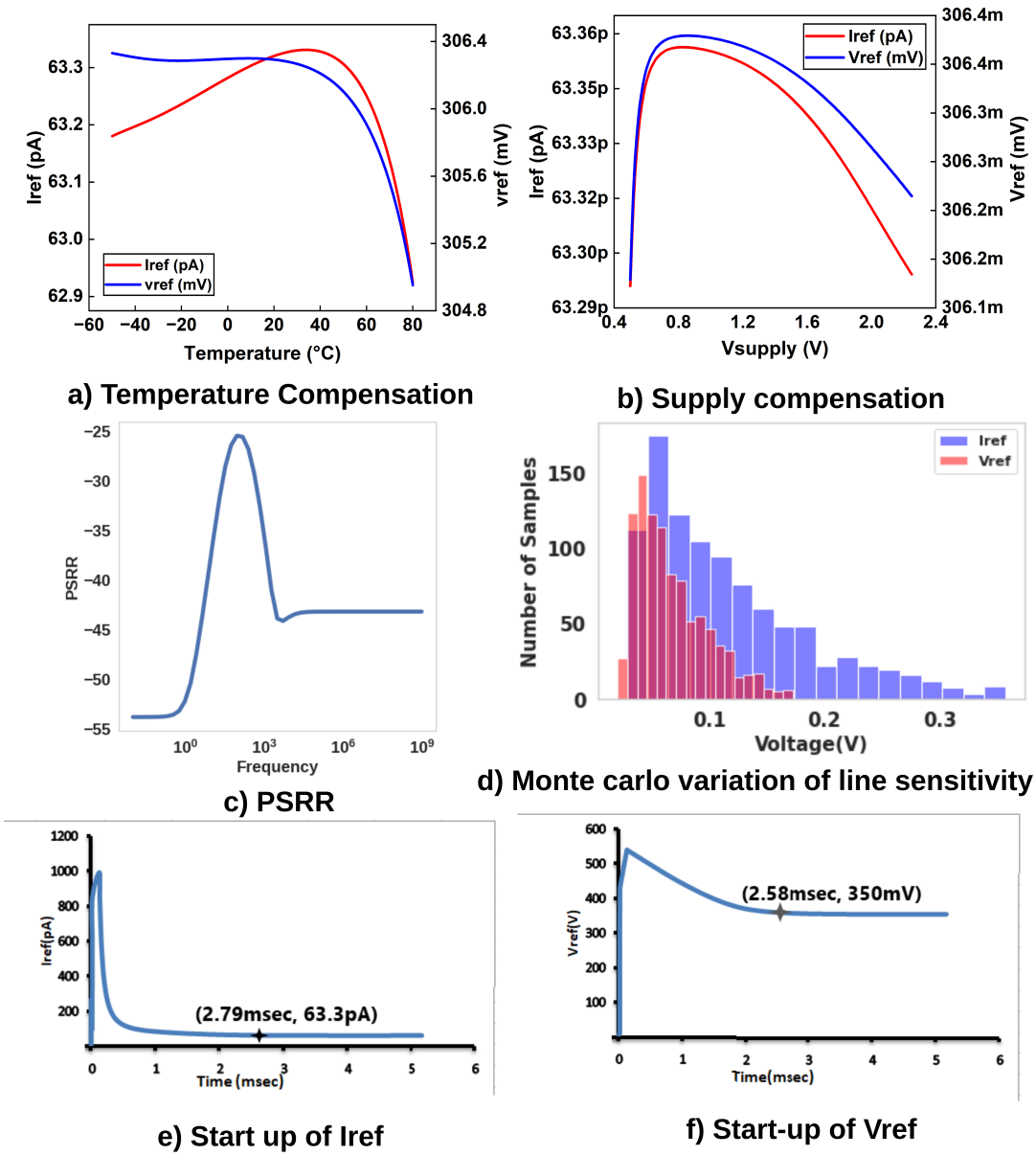


Figure 2.6: Results of reference circuit

0.5V, design [18] has a much greater temperature coefficient of 832ppm/°C and doesn't work at negative temperatures. Although design [19] gives a promising temperature coef-

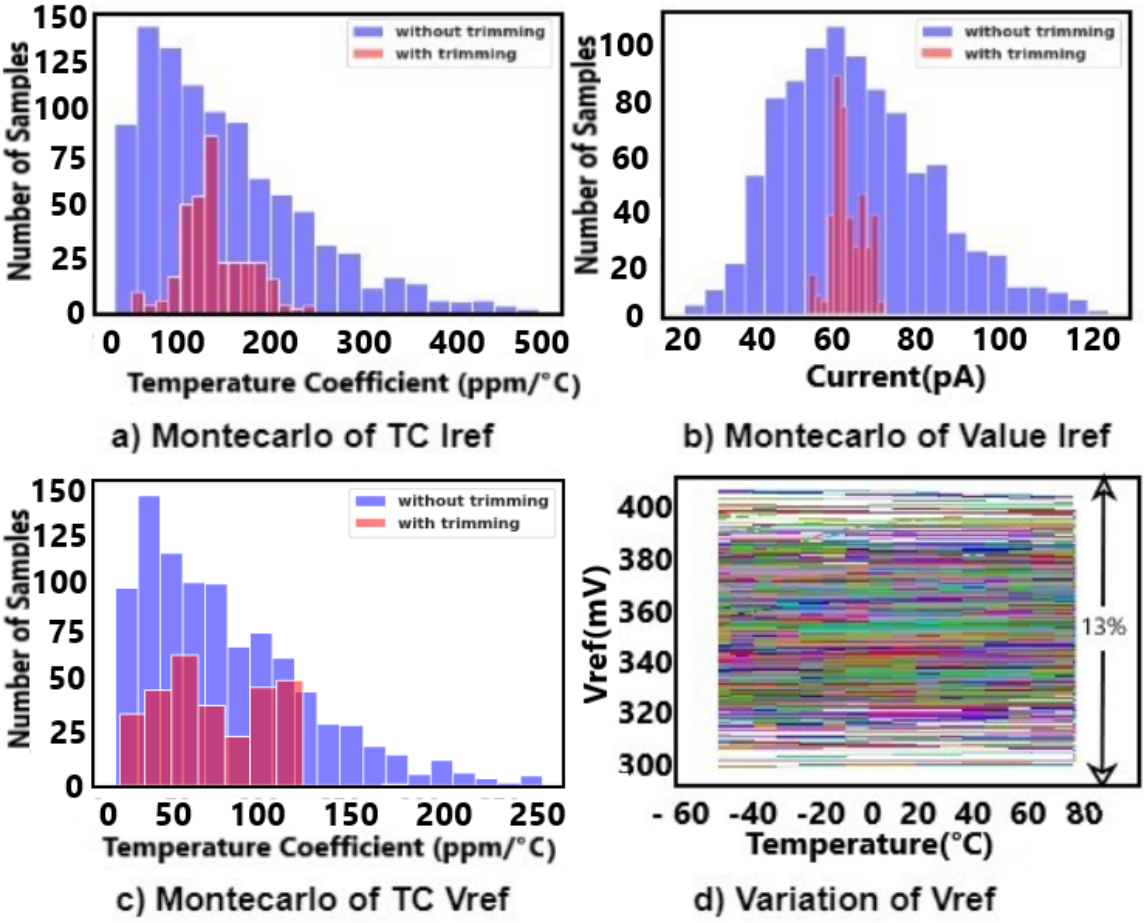


Figure 2.7: Montecarlo variations of reference values

ficient and temperature range, it consumes nW power. The current references working at 0.5V supply [24, 28, 27] don't work at a proper negative temperature range as they rely on sub-threshold leakage. These designs have line sensitivities (2.6,0.78,2.5(%/V)) which are much greater than the LS of the proposed design (0.057%/V).

2.2.5 Conclusion

This paper introduces a pioneering pico-watt current/voltage reference design tailored to provide superior, supply-insensitive reference values even at a low supply voltage of

Specifications	**This work**	[10]	[29]	[33]	[34]	[27]	[28]	[24]	[18]	[19]
Technology	**90nm**	90nm	180nm	180nm	180nm	40nm	65nm	65nm	180nm	180nm
Type	**Vref/Iref**	Vref/Iref	Vref/Iref	Vref/Iref	Vref/Iref	Iref	Iref	Iref	Vref	Vref
Vref(V) / Iref(pA)	**0.354/63.33**	0.53/43	1.238/6640	0.368/9970	0.5512/9400	-/2.4	-/1.2	-/5	0.046/-	0.118/-
Supply Voltage(V)	**0.5**	1	1.2	0.7	0.7	0.5	0.4	0.5	0.2	0.45
Temperature Range (°C)	**-55 to 75**	-55 to 100	-0 to 110	-40 to 125	-25 to 75	0 to 85	-20 to 60	0 to 100	0 to 70	-40 to 85
TC(ppm/(°C))	**29.68/34.53**	22/58	26/283	43/150	54/29	-/19	-/469	-/31	832/-	59.4/-
Power Consumption	**415pW**	156pW	9.3nW	28nW	5.32uW	8.2pW	3.4pW	14.5pW	3.2pW	15.6nW
Start up circuit	**Used**	Not Used	Used	Used	Used	NA	NA	NA	NA	NA
Calibration	**1-point**	1-point	1-point	1-point	1-point	1-point	2-point	1-point	1-point	1-point
Supply Range	**0.5V-2.3V**	1V-3V	1.3V-1.8V	0.7V-2V	-	0.5V-2.5V	0.4V-1.2V	0.5V-1.8V	0.2V-1.8V	0.45V-1.8V
Line Sensitivity(%/V/%/V)	**0.0318/0.057**	0.029/0.059	0.08/1.16	0.027/0.6	-/2.6	-/0.78	-/2.5	-/0.95	0.14/-	0.033/-
PSRR	**-59.218dB@DC**	-77dB@DC	-46dB@100	-59dB@10	-	-	-	-	-	-
Area(mm^2)	**0.0096**	0.00157	0.055	0.055	0.02	0.00025	0.008	0.000176	0.019	0.0132
Usage of Native oxide/ Amplifiers/Resistors	**No**	Native oxide	Amplifier	Resistors,Amplifiers	Resistors	No	No	Amplifiers	No	No

Table 2.1: **Comparison Table**

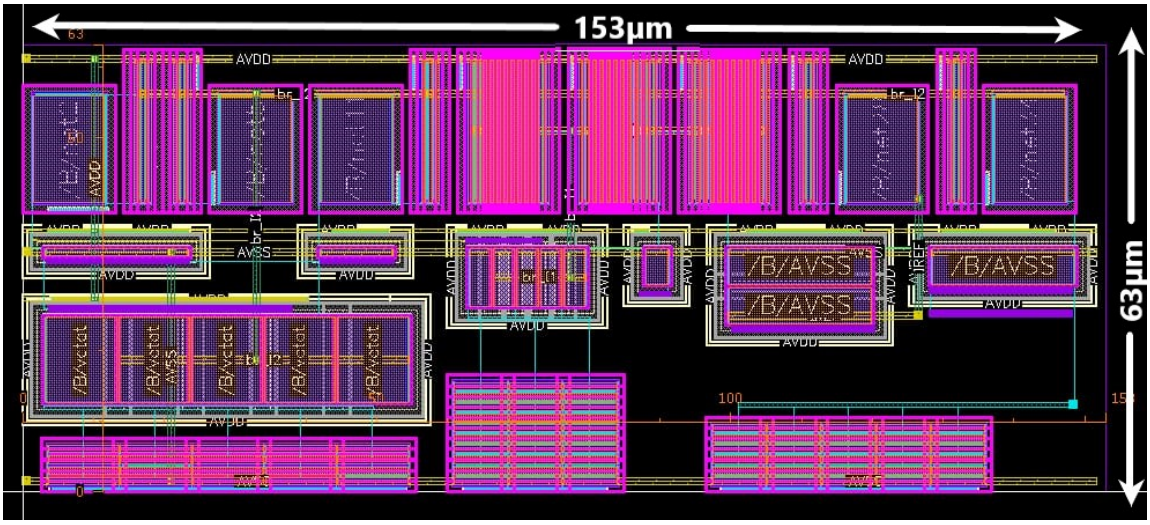


Figure 2.8: Layout

0.5V. Departing from conventional approaches, this design sidesteps the use of amplifiers and resistors, resulting in a straightforward and stable circuit with minimal area footprint. Central to this innovation is the utilization of multiple gate leakage transistors strategically incorporated to harness their inherent characteristics.

A key advancement lies in the implementation of a novel trimming technique that concurrently adjusts all gate leakage transistors. This innovative method effectively mitigates variations, ensuring consistent and reliable performance across diverse operating conditions. By trimming all gate leakage transistors simultaneously, the design achieves enhanced stability and precision, surpassing traditional trimming methods' limitations.

Overall, this novel design represents a significant advancement in current/voltage reference technology, offering unparalleled performance, efficiency, and reliability in low-voltage applications while minimizing circuit complexity and area requirements.

2.3 A 275pW, 0.5V Supply Insensitive Gate-leakage based Voltage/Current Reference Circuit for a Wide Temperature Range of -55 to 100°C Without Using Amplifiers and Resistors

2.3.1 Introduction

The trend towards scaling in electronic systems has driven a growing demand for more advanced voltage and current reference architectures in recent years. This trend, characterized by reduced size and increased integration of electronic devices, necessitates references that offer greater accuracy, stability, and precision at lower voltages and currents.

To meet the demands of this trend, both voltage and current reference architectures have had to evolve to provide more accurate, stable, and precise references at lower voltages and currents. Traditional architectures such as low dropout (LDO) voltage references, bandgap voltage references, Beta multiplier current references, trans-conductance-based references, and current mirrors are refined and improved to enhance performance and efficiency compared to earlier designs. The necessity of higher precision and accuracy in electronic systems has further driven the development of more advanced voltage and current reference architectures, ensuring their reliability and effectiveness across various applications.

Voltage and current references provide a stable, precise reference voltage or current as a reference point for measuring and controlling other voltage or current levels. Various applications, such as power supplies, data converters, and measurement equipment, use voltage references. Other essential applications like current sensing, precision measurement, and control systems demand current reference. The references play an essential role in ensuring the accuracy and consistent operation of electronic systems. They are critical for many telecommunications, automotive, industrial control, and medical equipment applications.

The design of voltage references uses a variety of techniques and architectures. The specific design will depend upon the desired performance characteristics and the application for the reference. One common approach for designing on-chip voltage references is to use a band-gap reference architecture[11, 12, 13, 14]. Although the architecture is widely used in modern integrated circuits and offers good performance and stability over a wide range of temperatures, they suffer from the massive demand for power(in µW and nW) and also need supply greater than 1V, making them insufficient for low power applications. Designs [35, 36, 37, 38] has modified the traditional BGR architecture to reduce the supply voltage. In design [35], MOSFETs acting in weak inversion region replace BJTs, which lowered the voltage drop from 0.6 to 0.2 V, hence opening up for a proper function at a much lower supply voltage of 0.6V. Bulk current biasing is used for all the PMOS transistors to reduce the threshold voltage and increase the voltage headroom. Design [36] uses a switched capacitor technique to reduce the supply voltage where capacitors are used to hold the PTAT and CTAT voltages and are appropriately weighted and added to generate the desirable reference voltage. Designs [37, 38] works for low supply voltage using Schottky diodes instead of BJTs working for supply voltages of 0.6V and 0.45V, respectively. The turn-on voltage of the Schottky diode is between 0.2 and 0.3V, significantly lower than the 0.6 to 0.7V typically needed to turn on a PN junction diode, making them a suitable substitute for low supply designs. However, Schottky diodes require specialized fabrication processes, which may not be compatible with the processes used for fabricating other circuit components. All the above designs use resistors and Op-Amps, contributing heavily to high power consumption. Another typical architecture for low supply voltage and low power exploits a basic 2-transistor working model [15] that relies on threshold voltage (Vth) subtraction of different thickness ZVT and NVT MOSFETs. Design [16] uses design [15] for reference voltage generation and an auxiliary amplifier to decrease the Line Sensitivity and increase PSRR. Although the design works at a minimum supply of 0.5V, the line sensitivity of 0.3%/V is relatively high for a voltage reference. The references [17, 18, 19, 20]

use additional bulk voltage for Vth compensation, which helps avoid the usage of amplifiers and resistors, significantly reducing the power and area. All these references work for a supply of less than 0.5V. Designs [17, 18] require access to the internal body nodes of deep n-well MOSFETs, which might not be feasible in all cases. Designs [19, 20] use a current subtraction circuit for body bias, which helped them to reduce line sensitivity, but the power consumption has increased to nW.

Current references are typical variants of beta multipliers in which the reference uses the V/R principle where temperature variations of voltage and resistors are canceled[21, 22, 23]. Furthermore, these circuits become more sensitive to supply fluctuations and power supply noise for a lower supply. Another approach is to generate reference voltage and use a voltage-to-current converter circuit. The design [24] uses a 2-transistor voltage reference and an Op-Amp as a buffer to obtain a reference current that works for a low supply of 0.5. However, it suffers from a high supply sensitivity of 0.94%/V, and usage of sub-threshold leakage limits the temperature range to 0 -100 °C. These designs use operational amplifiers (Op-Amps) and resistors. Such resistor-based designs are not suitable for pW applications and even consume a large area. Op Amps designed at 0.5V supply [25, 26] raise stability issues demanding cautious placement of capacitors. The design [9] is a modified beta multiplier architecture where the resistor is replaced with a gate leakage transistor for low power (pW) but works for a supply voltage greater than 1V. The above designs also use native devices to reduce supply sensitivity, but their usage has some limitations for low supply voltages. Designs [27, 28] works for low power (pW) and low supply (Sub 0.5V) by using gate leakage and sub-threshold leakage but have limitations concerning the supply sensitivity and temperature range. Their supply sensitivities are 0.78%/V and 2.5%/V, respectively, and they work for a temperature range of 0 -85 °C and -20 -60 °C, respectively.

References [29, 33, 30, 31, 34, 32, 39, 10, 40] depict the designs of current and voltage references in a single circuit. There are multiple approaches to designing voltage and current references for use in low-power systems, including the use of nano-power sub-bandgap

voltage and current reference topology, all-in-one bandgap voltage and current reference circuits, and low-voltage current and voltage reference designs based on the MOSFET ZTC effect. CMOS technology and leakage compensation techniques further reduce power consumption. The designs [29, 33, 30] use amplifiers and resistors in their designs. Design [29] uses a subthreshold leakage-based PTAT generator and a PN diode as a CTAT voltage. The above designs work for a supply greater than 1V. Although design [33] works for a supply of 0.7V where voltage reference uses a simple 2T transistor model and current reference is obtained by passing this through a temperature-insensitive resistor, it has a high supply-sensitive current(0.6%/V) and temperature-sensitive current(149.8ppm/°C). Design [30] gives better temperature-compensated reference values of 6.6 and 34ppm/°C for voltage and current, respectively, but works for a supply voltage of 2.5V. Designs [31, 34, 32] avoid the usage of amplifiers but have high power consumption and supply voltage. [31] uses a simple three-branch self-biased structure using BJT to generate current reference and voltage reference is derived by driving the current to a temperature-insensitive resistor. Design [34] uses the principle of bandgap reference for generating reference voltage and a current subtractor circuit that nullifies the PTAT nature to obtain current reference. The design works for a supply of 0.7V, but due to the use of resistors, its power has increased to uW. The design [32] uses a sub-bandgap model without using op-amps to achieve a reference for a wide range of -40 to 120 °C. The design [39] works for a supply of 0.85V where a difference generates the voltage reference V_{th} of two different gate thickness MOSFETs and generates a current reference using a resistor. All the designs utilize power in the range of nW, limiting their application to much lower power. Design [10, 40] works at a low power of pico-W by using gate leakage transistor. The design [10] uses native oxides that have limitations with respect to cost and have increased the supply to 1V. The design [40] works for a lower supply of 0.5V with a power consumption of around 500pW.

The state-of-the-art architectures mentioned above exhibit limitations. Some designs may operate effectively at lower supply voltages but at the expense of higher power con-

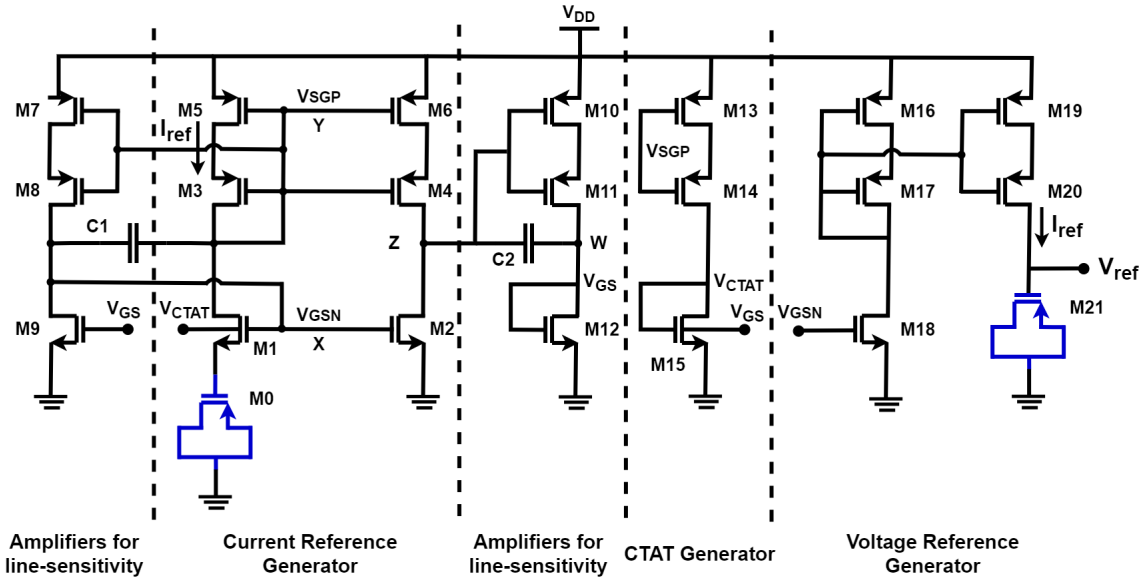


Figure 2.9: Proposed Voltage/Current reference

sumption or higher line sensitivity. Additionally, integrating multiple MOSFET types to improve functionality may escalate production costs. Furthermore, using components such as resistors and amplifiers may introduce trade-offs concerning circuit area and cost efficiency. This paper presents a novel pico-watt current/voltage reference that works at a lower supply voltage of 0.5V, operating for a wide voltage range of 0.5-2.3V and for a practical temperature range of -55 to 100°avoiding usage of amplifiers, resistors, and Native devices.

2.3.2 Proposed Circuit

As shown in Fig 2.9, the proposed circuit relies on the most generic beta multiplier circuit. The beta multiplier circuit Fig 2.10a generates a reference current relying on the principle of subtraction of V_{gs} of two MOSFETs

$$\begin{aligned} V_{comp} &= V_{gsNM1} - V_{gsNM2} \\ I_1 &= \frac{(V_{gsNM1} - V_{gsNM2})}{R} \\ I_1 &= \frac{(V_{thNM1} - V_{thNM2} + mV_T ln(\frac{(w/l)NM2}{(w/l)NM1}))}{R} \end{aligned} \tag{2.13}$$

Gate leakage transistor replaces resistor(R), giving Giga-Ohms a high resistance without

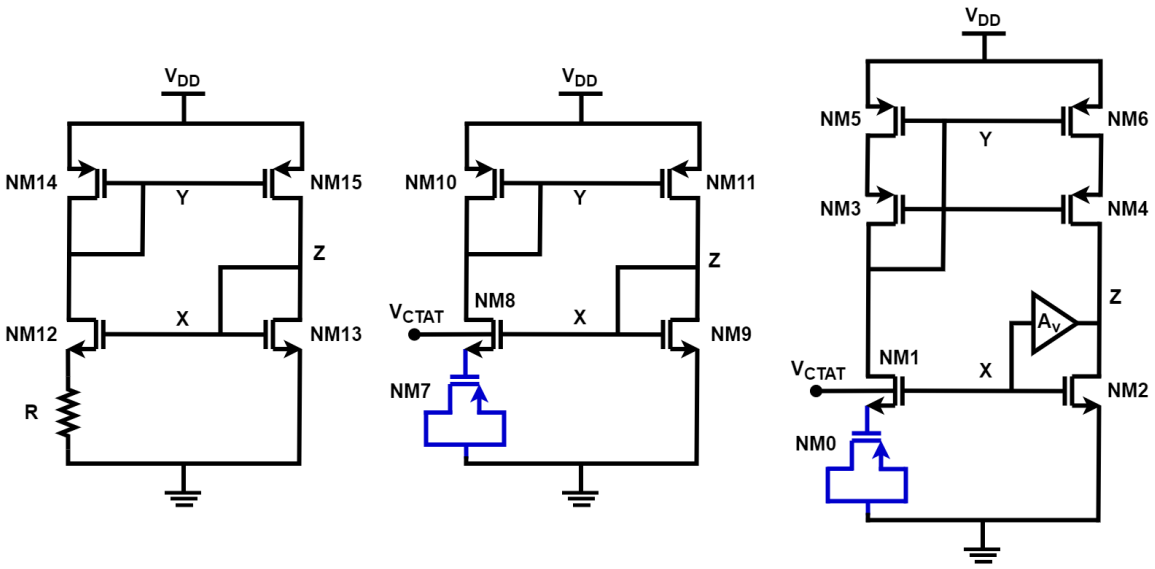


Figure 2.10: a) Traditional beta multiplier b) Modified beta multiplier for temperature compensation c) Modifications for improved supply sensitivity

utilizing a high area.[41]

The [42] explains the modelling of gate leakage transistors for practical temperature range. The gate leakage transistor used in this design is employed in the accumulation region and chosen such that temperature variations are minimal. Fig 2.11 shows the temperature characteristics of the gate leakage transistor.

2.3.2.1 Temperature Compensation

Temperature-compensated current is obtained from properly setting CTAT curve $V_{thNM2}-V_{thNM1}$ and PTAT curve $mV_Tln(\frac{(w/l)NM2}{(w/l)NM1})$ precisely with the nature of Resistance(R) in (2.13). Analyzing the characteristics of the gate leakage transistor reveals its stable value concerning temperature, allowing us to approximate its nature to a ZTC. So, to obtain temperature-compensated current, we need to cancel the CTAT and PTAT nature of the numerator of the equation. The general practice is to use two different MOSFETs whose

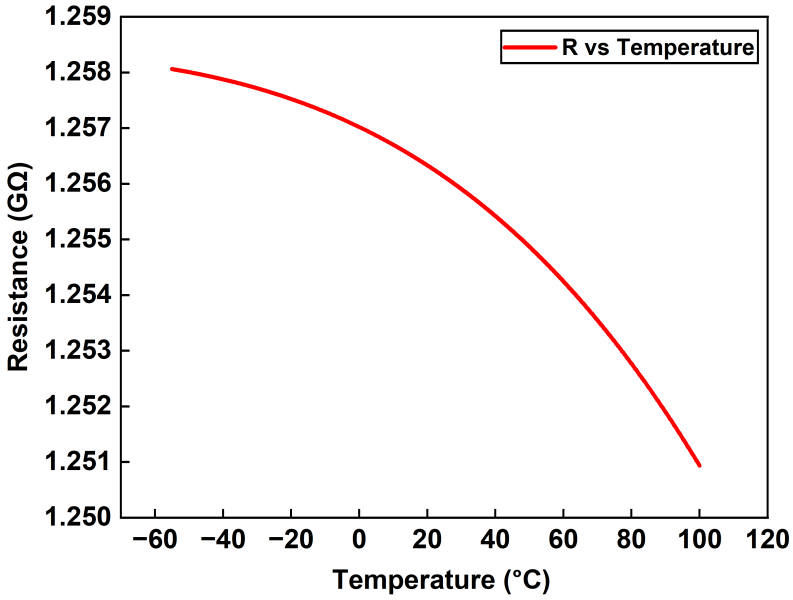


Figure 2.11: Gate leakage transistor characerstics

V_{th} difference gives sufficient CTAT to compensate for the PTAT, which depends on the ratio of (w/l). Using native oxide as one of the MOSFETs is a common practice, but it is undesirable in this case because of the supply limitations as the value of $V_{thNM2} - V_{thNM1}$ in case of native will be more than 500mV. Using two different MOSFETs whose V_{th} difference is less leads to high variations concerning the process.

We propose a new technique for temperature compensation, exploiting the concept of V_{th} dependence on body voltage. The compensation is achieved by applying a CTAT to the body of one of the MOSFETs, generating a difference in the V_{th} even when using two similar MOSFETs. Fig 2.10b. depicts the modified beta multiplier circuit for temperature compensation.

The V_{th} of two such MOSFETs are

$$\begin{aligned} V_{th_{N}M3} &= V_{th_0} \\ V_{th_{N}M4} &= V_{th_0} + \gamma \cdot \left(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|} \right) \end{aligned} \tag{2.14}$$

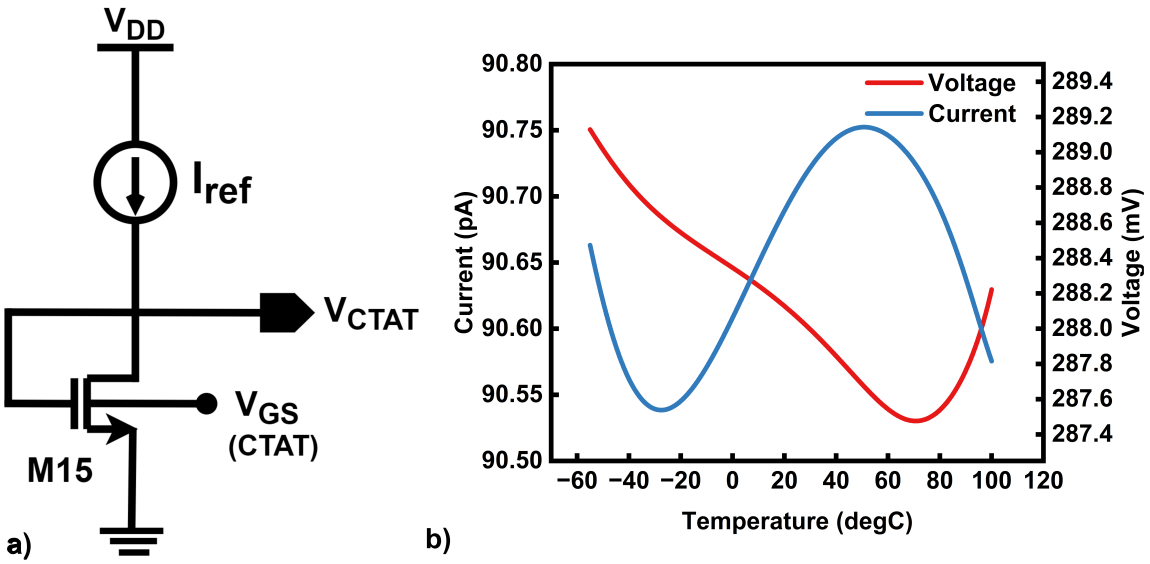


Figure 2.12: a)CTAT generator b)Temperature compensated curves

By properly adjusting the aspect ratios and by giving proper CTAT voltage at the body of the MOSFETs, the numerator can be temperature compensated in (2.13).

The voltage reference uses the concept of gate voltage generation, which is when current flows through the gate leakage transistor. Using the same gate leakage transistor of the same characteristics as explained earlier, the reference current generated flows through the gate leakage transistor. The above technique successfully provides temperature-compensated current and voltage curves, as shown in Fig 2.12b.

$$V_{ref} = I_{ref} * R \tag{2.15}$$

We designed the CTAT generator to address the issue., as shown in Fig 2.12a. The V_{gs} of diode-connected MOSFET is a CTAT voltage when a constant current is allowed in it. The CTAT voltage obtained will be

$$V_{gs} = V_{th0} + mV_T ln(\frac{I_o}{\mu_n C_{ox}(w/l)(m-1){V_T}^2}) \tag{2.16}$$

It's observed that on using a temperature-independent current source the slope of CTAT is much higher than the practical range(greater than 1mV/°C) and the slope of CTAT has a minimum variation with (w/l) of the MOSFET. For better control on the slope, another CTAT is given to its body giving the final curve.

$$V_{gs} = V_{th0} - \gamma \cdot \left(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right) + mV_T ln(\frac{I_o}{\mu_n C_{ox}(w/l)(m-1){V_T}^2}) \tag{2.17}$$

To avoid external circuitry for CTAT giving at the body of the MOSFET, it's taken from the beta multiplier circuit itself as shown. The constant current source is obtained by mirroring the reference current generated.

2.3.2.2 Improving Line-sensitivity

The line sensitivity of the conventional beta multiplier heavily depends upon the strength of the current mirror load. The operation of current mirrors is affected by the supply voltage. As the supply voltage decreases, the transistors may exhibit more significant variability in their characteristics, leading to a less precise output current. In addition, at lower supply voltages, the voltage headroom across the current mirror is also reduced, limiting the range of output currents that the current mirror can accurately produce. Moreover, at lower supply voltages, the current mirror may also be more sensitive to noise and fluctuations in the supply voltage, which can lead to variations in the output current and reduce the stability of the circuit.

For better performance of the current mirror, the current mirror load can be cascoded. However, the NMOS current mirror in our design cannot be cascoded because of the headroom issues. To improve the mirroring action, we can increase the feedback strength of diode-connected MOSFET by increasing the gain by A_V as shown in Fig 2.10c. [43, 44]. To increase the feedback gain and avoid change in the phase, we add two CS amplifiers, as

shown in Fig 2.9. Current reference generator block. The excess gain added is

$$\begin{aligned} A_V = -(gm_{10} * (gm_{11} * rds_{11} * rds_{10}) || (\frac{1}{gm_{12}})) \\ * - (gm_9 * (rds_9 || gm_8 * rds_8 * rds_7))) \end{aligned} \tag{2.18}$$

The conventional beta multiplier as shown in Fig 2.10a. is in positive feedback with a loop gain of less than 1, making it stable as in Fig 2.14a.

$$\begin{aligned} loopgain_{without} = \frac{1}{gm_{NM5} * R} \\ loopgain_{with} = \frac{A_V}{gm_{NM5} * R} \end{aligned} \tag{2.19}$$

The effect of adding an amplifier can be seen in the loop gain graph, as shown in Fig 2.14b. For positive feedback, to ensure stability, we need to make the magnitude of loop Gain less than 1 when the phase of loop Gain crosses zero degrees. So, to stabilize the circuit, we need to add a miller capacitor between the first two dominant poles such that pole splitting happens and the magnitude drops to less than 1 when the phase of loop Gain crosses zero degrees.

Considering the main positive feedback loop formed by nodes X, Y, Z, and W, as seen in Fig 2.9. the current reference generator block along with the amplifiers for line sensitivity. The equivalent resistance and capacitance at node X can be calculated as follows:

$$\begin{aligned} R_{nodeX} &= rds_9 || (gm_8 * rds_8 * rds_7) \\ C_{nodeX} &= Cgs_2 + Cgd_2(1 - A_2) + Cgs_1(1 - A_{01}) \\ &\quad + Cgd_1(1 - A_1) + Cgd_9(1 - \frac{1}{A_9}) \\ &\quad + Cgd_8(1 - \frac{1}{A_8}) \end{aligned} \tag{2.20}$$

The equivalent resistance and capacitance at node Y can be calculated as follows:

$$\begin{aligned} R_{nodeY} &= \frac{1}{gm_5}||(gm_1 * rds_1 * R) \\ C_{nodeY} &= Cgs_5 + Cgs_6 + Cgd_5(1 - A_5) + Cgd_6(1 - A_6) \\ &\quad + Cgs_3 + Cgs_4 + Cgd_4(1 - A_4) + Cgs_7 + \\ &\quad Cgs_8(1 - A_{08}) + Cgd_7(1 - A_7) + Cgd_8(1 - A_8) \\ &\quad + Cgd_1(1 - \frac{1}{A_1}) \end{aligned} \tag{2.21}$$

The equivalent resistance and capacitance at node Z can be calculated as follows:

$$\begin{aligned} R_{nodeZ} &= (gm_4 * rds_4 * rds_6)||rds_2 \\ C_{nodeZ} &= Cgs_{10} + Cgs_{11}(1 - A_{011}) + Cgd_{10}(1 - A_{10}) \\ &\quad + Cgd_{11}(1 - A_{11}) + Cgd_4(1 - \frac{1}{A_4}) + Cgd_2(1 - \frac{1}{A_2}) \end{aligned} \tag{2.22}$$

The equivalent resistance and capacitance at node W can be calculated as follows:

$$\begin{aligned} R_{nodeW} &= \frac{1}{gm_{12}}||(gm_{11} * rds_{11} * rds_{10}) \\ C_{nodeW} &= Cgs_{12} + Cgs_9 + Cgd_{11}(1 - \frac{1}{A_{11}}) \\ &\quad + Cgd_9(1 - \frac{1}{A_9}) \end{aligned} \tag{2.23}$$

Where Cgs and Cgd are the gate-to-source and gate-to-drain capacitances of MOSFET, A_i is the gain across that MOSFET (i) from gate-to-drain, A_{0i} is the gain across that MOSFET (i) from gate to source. We can observe that the resistance at node X will be high and capacitance at node X will be high as $A_2 = -gm_2 * (rds_2||gm_4 * rds_4 * rds_6) + \frac{1}{gm_5 * R} * (gm_6 * (rds_2||gm_4 * rds_4 * rds_6))$, making node X a dominant pole. Although node Y has a high capacitance with the addition of parasitic capacitance of MOSFETs M_5, M_6, M_4, M_7, M_8, its resistance is low ($\frac{1}{gm_5}$). The parasitic capacitance of these MOSFETs will be high because of the high area for proper mirroring, making node Y the next dominant pole. The main miller cap C1 is added between nodes X and Y for proper pole

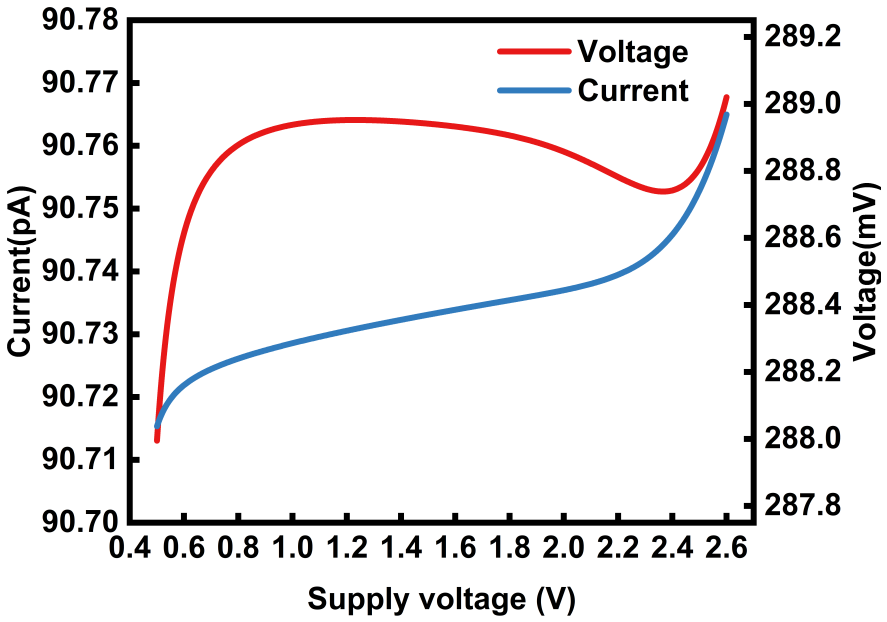


Figure 2.13: Line Sensitivity

splitting. Another capacitance is added between nodes Z and W to compensate for the excess zeros created by capacitance C1 and increase the phase margin.

As Fig 2.14a depicts the loop gain and phase of a simple beta multiplier in positive feedback, its stability is ensured by having less than 0 dB for all the frequency ranges. From Fig 2.14b, we can see that after adding the amplifiers, the loop gain became positive and unstable. In Fig. 2.14c, we can see the effect of adding capacitors, which increases phase. So, when the phase crosses 0°, i.e., when the feedback changes to positive, the loop gain becomes negative, which makes the loop stable, and the circuit becomes stable with a phase margin of 66°. The proposed architecture improves the line sensitivity of the reference working from 0.5V to 2.5V, and the curves are shown in Fig 2.13.

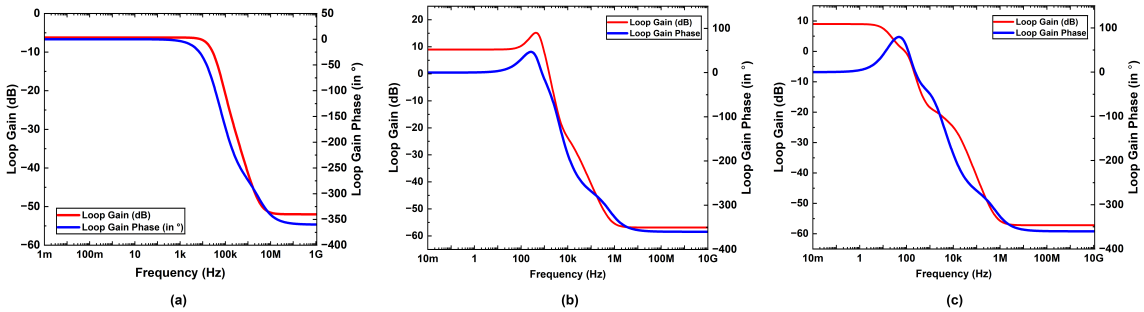


Figure 2.14: a) The loop gain of Beta-multiplier(Fig 2.10b) b) Loop gain after adding amplifier(Fig 2.10c) c) Loop gain after adding capacitors

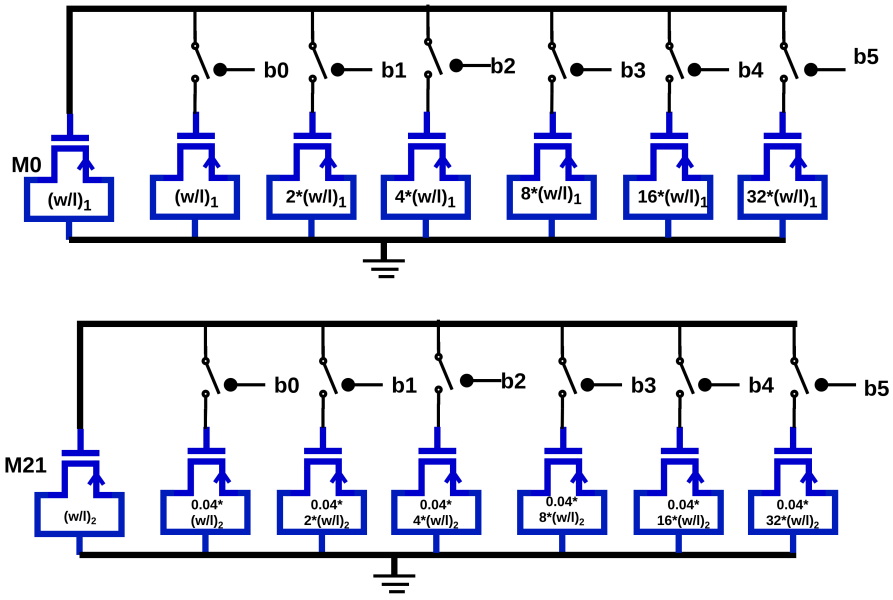


Figure 2.15: Trimming circuitry

2.3.3 Trimming

Gate leakage-based current references are particularly sensitive to process variations, necessitating the use of a trimming circuit to control this variation effectively. Trimming the gate leakages of two transistors typically requires a higher number of trim bits. However, an innovative approach involves adjusting the widths of the trim circuit components according to a specific ratio, such as 1:0.04. By selecting these widths appropriately, it becomes possible to trim the two gate leakages simultaneously using just 6-bit trim bits, as illustrated in Fig 2.15. This approach streamlines the trimming process and optimizes resource utilization. Notably, the switches employed in this circuit are gate-boosted and low-leakage switches, chosen for their ability to minimize leakage and enhance overall circuit performance.[45, 46, 47, 48]

2.3.4 Results and Discussion

The proposed Voltage/Current reference is designed and implemented in a 90nm CMOS process. Fig 2.12b shows temperature-compensated current and voltage plots. It depicts the temperature coefficient (TC) of 15.2 ppm/°C and 36.8 ppm/°C, respectively, for the temperature range of -55 to 100°C. Fig 2.13 shows the proposed circuit works for the supply range of 0.5-2.6V, having supply sensitivity of 0.0284%/V and 0.154%/V for current and voltage reference, respectively. The design consumes 275.26pW at nominal conditions, and due to the usage of gate leakage-based resistance, the power consumption remains almost constant (1.00294 times) over the temperature range of -55 to 100°C. Fig 2.16 shows the variation for 1000 samples. From Fig 2.16d. and 2.16e. the current reference value has a mean(µ) of 90.7pA and variation(σ) of 20pA without trimming that can be effectively reduced to 2pA with trimming. In Fig 2.16f. and 2.16g., the 3σ variation of voltage reference is 0.026V, and the mean is 0.288V having 9% of variation with worst case temperature coefficient of 150ppm/°C at nominal conditions. This design uses the same 6-bit trim bits for both current reference and voltage reference trimming which degrades

the 3σ variation of voltage reference. The 3σ variation of voltage reference can be improved by using separate trim bits for voltage reference. The PSRR at DC for the voltage reference at 0.5V, 1V, and 1.5V are -60dB, -87dB, and -88dB, respectively. The PSRR at a higher frequency is around -38dB, which can be increased by increasing the size of the gate leakage-based capacitor at the expense of increasing the area. As this architecture contains multiple loops, a start-up circuit is added to avoid any degenerative conditions. Fig 2.16b and 2.16c show the 99% settling times for the current and voltage reference to be 18ms and 20ms, respectively. The layout of the proposed design is shown in Fig 2.17, which occupies an area of 0.087 mm^2.

Table 2.2: Performance summary and comparison with state-of-the-art Current/Voltage references

	This work	[40]	[10]	[34]	[29]	[39]	[33]	[31]
Technology(nm)	**90**	90	90	180	180	180	180	180
Type	**Iref/Vref**	Iref/Vref	Iref/Vref	Iref/Vref	Iref/Vref	Iref/Vref	Iref/Vref	Iref/Vref
V_{DD} (Supply Range)	**0.5V-2.6V**	0.5V	1V-3V	0.7V	1.3V-1.8V	0.8V-2V	0.7-2	1.1V-2V
Power(nW)	**0.275**	0.415	0.156	7.6	9.3	12	28	51
I_{ref}(A)/V_{ref}(V)	**90.7pA/0.288**	63.33pA/0.354	43pA/0.534	940nA/0.512	6.64nA/1.238	7.5nA/0.346	9.97nA/0.368	6.7nA/0.180
Trimming used	**Yes**	Yes	Yes	Yes	Yes	No	Yes	Yes
Temperature Range(°C)	**-55 - 100**	-55 - 75	-55 - 100	-25 - 75	0 - 110	-40 - 125	-40 - 125	-40 - 120
TC (ppm/°C)	**15.2/36.8**	34.53/29.68	22/58	54/29	283/26	59/21.98	149.8/43.1	40.33/32.76
Line Sensitivity (%/V)	**0.0284/0.154**	0.057/0.0318	0.029/0.059	0.058/1.76	1.16/0.08	0.31/-	0.6/0.027	0.03/0.031
PSRR (db@DC)	**-60**	-59.21	-77	-80@100	-46@100	-60@10	-59@10	-59@10
Area (mm^2)	**0.087**	0.0096	0.00157	0.063	0.055	0.063	0.04	-
Resistors/Amplifiers/Native	**Not Used**	Not Used	Used	Used	Used	Used	Used	Used

Tables 2.2 and 2.3 summarize the circuit's performance with the corresponding reference designs. Most of the current/voltage reference circuits, like [29, 33, 30, 34, 39] consume nW range power with a supply much greater than 0.5V and use amplifiers. Although the references [10] and [**?**] consume pW power, [10] has a minimum supply voltage of 1V and uses native oxide devices, while [**?**] has a lower temperature range and higher power

Table 2.3: Performance summary and comparison with state-of-the-art low power references

	This work	[23]	[9]	[27]	[28]	[20]	[17]	[18]
Technology(nm)	**90**	180	55	40	65	130	180	180
Type	**Iref/Vref**	Iref	Iref	Iref	Iref	Vref	Vref	Vref
V_{DD} (Supply Range)	**0.5V-2.6V**	1.4V	1.2V-4V	0.5V	0.4V-1.2V	0.5V	0.25V	0.2V-1.8V
Power(nW)	**0.275**	300	0.144	0.008	0.003	0.002	0.005	0.003
I_{ref}(A)/V_{ref}(V)	**90.7pA/0.288**	50nA	60pA	2.4pA	1.2pA	0.175	0.091	0.042
Trimming used	**Yes**	Yes	Yes	Yes	No	No	No	No
Temperature Range(°C)	**-55 - 100**	-55 - 125	-55 - 125	0 - 85	-20 - 60	-20 - 80	0 - 120	0 - 70
TC (ppm/°C)	**15.24/36.8**	11.6	19	18.6	469.3	19.4	24.86	832
Line Sensitivity (%/V)	**0.0284/0.154**	0.05	0.07	0.78	2.5	0.033	0.42	0.14
PSRR (db@DC)	**-60**	-75@10	-	-80@1	-238.4@1	-70@100	-	-
Area (mm^2)	**0.087**	0.009	0.0003	0.00025	0.008	0.001	0.002	0.019
Resistors/Amplifiers/Native	**Not Used**	Used	Not Used	Used	Used	Used	Not Used	Not Used

consumption compared to our design. The proposed design works from a low supply voltage of 0.5V for a wide temperature range from –55 to 100°C while consuming only 275.36pW.

2.3.5 Conclusion

Voltage and current references play a critical role in various electronic systems, providing stable and accurate reference signals for other components to operate properly. A novel pico-watt current/ voltage reference circuit that works for a low supply of 0.5V is proposed in the paper. With proper mathematical support and justification, the design modifies the basic beta-multiplier architecture to achieve the required specifications at a low supply voltage. The design doesn't include resistors or amplifiers, giving an easy and stable circuit with a low area. It works for a wide temperature range of -55 to 100 °C and a wide voltage of 0.5 to 2.6V, giving an excellent temperature coefficient and line sensitivity for the reference values. The design gives better line sensitivity for current reference working at 0.5V supply

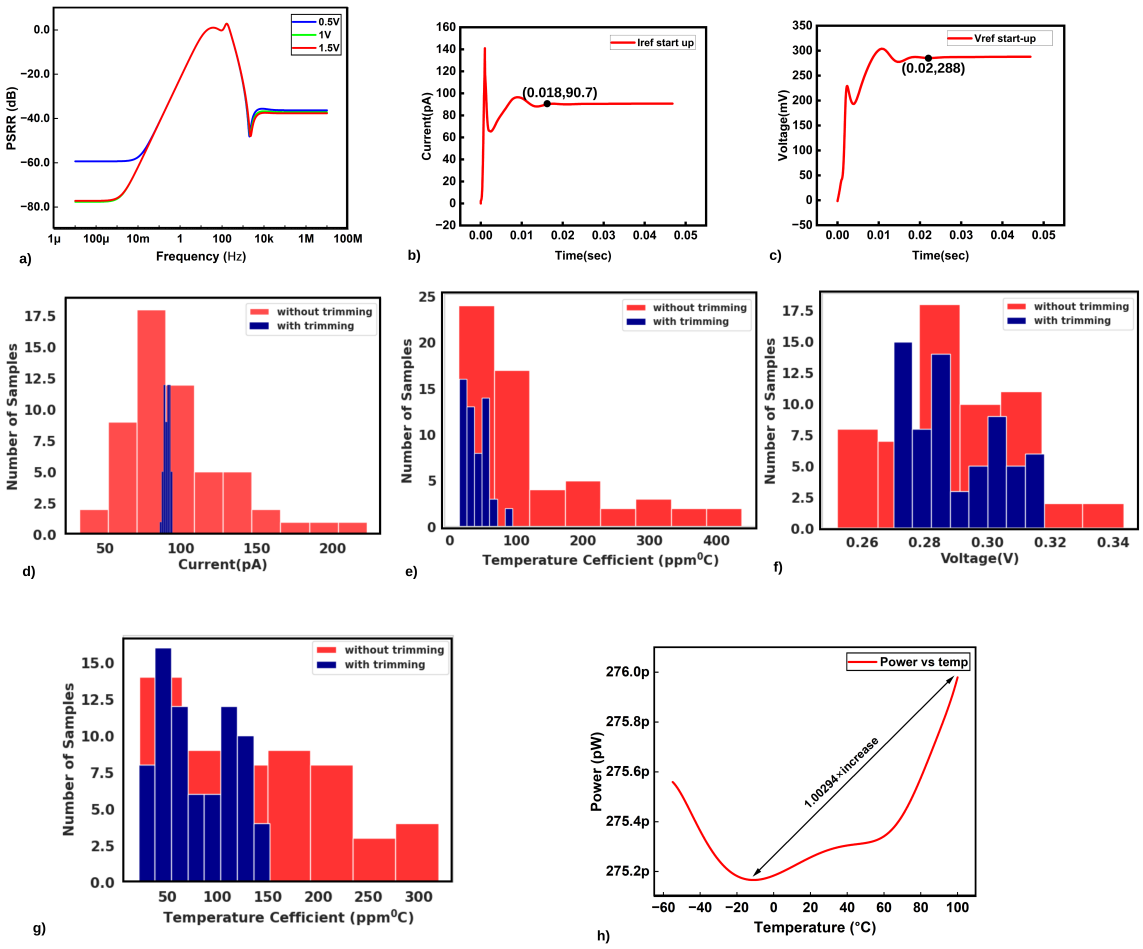


Figure 2.16: a) PSRR of the circuit b) Start-up time for current reference c) Start-up time for voltage reference d) Monte-Carlo variation of current reference value e) Monte-Carlo variation of current reference TC f) Monte-Carlo variation of voltage reference value g) Monte-Carlo variation of voltage reference TC h) Variation of power with temperature

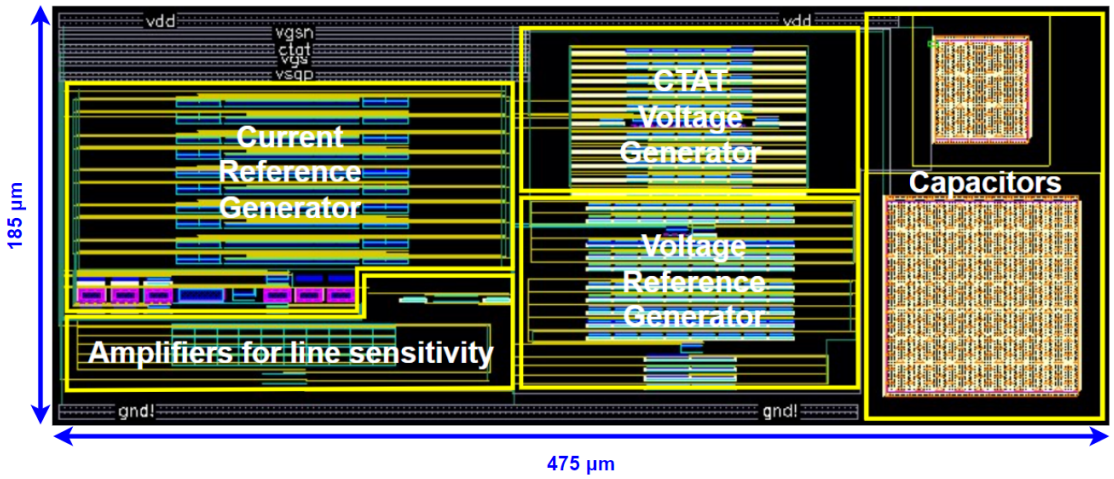


Figure 2.17: Layout

when compared to the state-of-art. Multiple gate leakage transistors are used, and a different method of trimming that trims all the gate leakage transistors simultaneously, effectively reducing the variation, is used.

2.4 A 2.36nW Gate-Leakage Based Sub-Bandgap Voltage Reference with $4.305\% \pm 3\sigma$-inaccuracy from -40°C to 150°C for Low-Power IoT Systems

2.4.1 Introduction

The surge and swift evolution of the Internet of Things (IoT) have spawned numerous applications, spanning from intelligent wearables and wireless sensors to medical devices, smart home accessories, and remote sensing systems. Given the emphasis on compact form factors, these devices are typically powered by miniaturized batteries or energy harvesting units like photovoltaic cells and RF energy harvesters. However, power consumption emerges as a critical bottleneck, necessitating aggressive reduction strategies to enable the widespread adoption of this technology. While duty cycling is commonly employed to lower average power consumption, traditional voltage references, which operate continuously, require innovative architectures to address power constraints effectively. In addition to power efficiency, these references must function reliably across a wide temperature range with high accuracy and line sensitivity, all while minimizing the need for extensive trimming circuits. Leveraging the inherent stability and reduced process, supply, and temperature dependencies of bandgap references, the design of BJT-based references presents a promising avenue for meeting these demanding requirements.

Conventional voltage references, exemplified by works such as [11, 12, 13, 14], operate within the μW range, posing significant limitations on system lifetime and hindering their applicability in low-power scenarios. While voltage references using Silicon-On-Insulator (SOI) technology have been proposed for high-temperature environments [49], they still exhibit power consumption in the μW range. Addressing this challenge, [50, 32, 51, 52, 53] introduce voltage references with nW power consumption; however, these solutions typically employ high-value resistances, leading to increased silicon area, and are limited to specific temperature ranges. Similarly, approaches like the one presented in [54] utilize

sample-and-hold techniques to achieve average power consumption in the nW range but suffer from large silicon footprints and restricted operating temperatures. Furthermore, efforts to develop pW voltage references [55, 56, 57, 58] for high-temperature applications encounter challenges such as exponential power consumption growth with temperature and limited functionality in negative temperatures, primarily due to dependency on sub-threshold leakage phenomena and reliance on native oxide devices (NVT MOSFETs) not universally available.

In contrast, this paper introduces a novel 2.3nW sub-bandgap voltage reference tailored for high-temperature remote sensing applications. Unlike prior approaches, the proposed sub-BGR architecture eliminates the need for high-value resistors, native devices, or complex compensation techniques, thereby minimizing power consumption, silicon area, and supply voltage requirements. By leveraging the gate leakage current properties of thin oxide devices in weak inversion mode, the proposed solution achieves robust and efficient generation of the reference voltage essential for reliable operation in harsh environments.

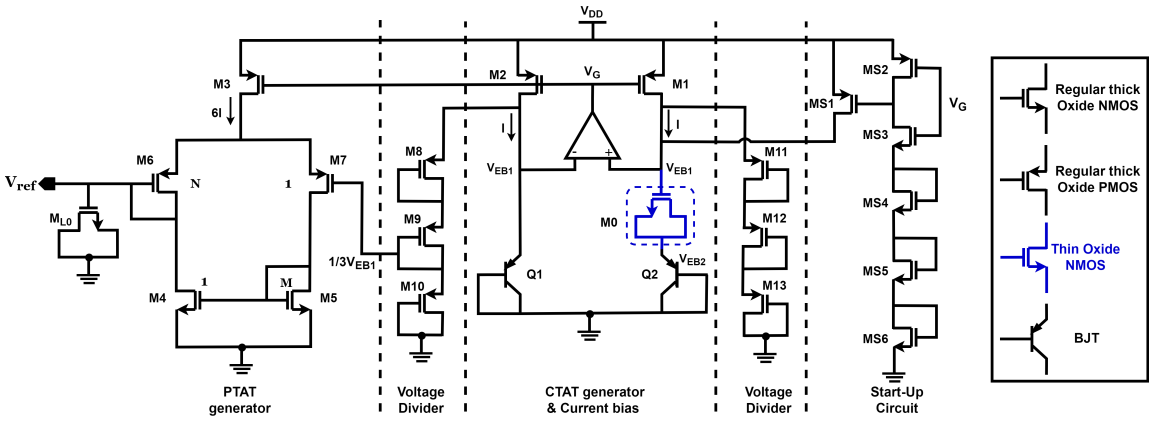


Figure 2.18: Block Diagram of the proposed sub-BGR

2.4.2 Proposed Sub-Bandgap Voltage Reference

The proposed sub-BGR architecture, depicted in Fig 2.18, features a design where all transistors, except for M0, utilize standard thick oxide NMOS and PMOS devices. M0, on the other hand, employs a thin oxide structure, enabling tunnelling current to flow through its gate due to its remarkably low oxide thickness. This unique characteristic allows M0 to bias the circuit in a low current regime without necessitating large resistor values. Operating in weak inversion mode, the gate leakage transistor M0 exhibits specific I-V characteristics and expressions, elaborated upon in the subsequent section.

The circuit primarily comprises a PTAT and CTAT generator, each compensating accordingly to produce the reference voltage. The core of the CTAT generator, constituting Bipolar Junction Transistors (BJTs) Q1 and Q2 and a two-stage NMOS Operational Transconductance Amplifier (OTA), is biased by an accumulation mode gate leakage-based PTAT current reference of 137pA, as depicted in Fig 2.19b. This current reference design ensures the functionality of the OTA across all corners in the wide temperature range.

The PTAT generator incorporates a differential pair and current mirror to generate PTAT voltage. To align the PTAT slope, a voltage divider is employed to adjust the slope of the CTAT voltage, thereby generating the reference voltage accordingly. The symmetric

placement of the voltage divider on both sides of the sub-BGR core ensures uniform loading effects in both branches of the current mirror.

A capacitor (C_{eq}=2.8pF), implemented using a thick oxide device (M_{L0}), is connected at the output to enhance power supply rejection ratio (PSRR) at higher frequencies. Additionally, a start-up circuit [59] is integrated to prevent any degenerate conditions.

2.4.2.1 Derivation for Weak Inversion Mode Gate-leakage Current

As mentioned above, a gate-leakage transistor is used to bias the circuit in a low current regime. As the gate-leakage transistor is operated in a weak inversion region, we have three major current components, the gate-to-source/drain current(I_{gs} and I_{gd}) and gate-to-channel current(I_{gc}). The gate to source current will be of the form [60]:

$$I_{gs} = K * V_{gs} \left(V_{gs} - V_{fbsd}\right) \tag{2.24}$$

Here K comprises the effective dimension of gate-leakage MOSFET and modelling constants, which are constant for a given technology node and is independent of temperature. Here V_{fbsd} is the flat-band voltage between gate and S/D which has an approximate value of 6.67mV as given in [60]. From the symmetry of the gate-leakage MOSFET, the gate-to-source current will be equal to the gate-to-drain and hence $I_{gsd}(= I_{gs} + I_{gd})$ will be twice of gate-to-source current(I_{gs}).

The total gate leakage also consists of the gate-to-channel current (I_{gc}), which is given by [9]:

$$\begin{aligned} I_{gc} = {} & W_{eff} L_{eff} \cdot A \cdot T_{ox\ \text{Ratio}} \cdot V_{gse} \cdot V_{aux} \cdot \exp[-B \cdot TOXE \\ & (AIGC - BIGC.V_{oxdepinv}) \cdot (1 + CIGC \cdot V_{oxdepinv})] \end{aligned} \tag{2.25}$$

$$V_{aux} = NIGC \cdot v_t \cdot \ln\left(1 + \exp\left(\frac{V_{gse} - V_{TH}}{NIGC \cdot v_t}\right)\right) \tag{2.26}$$

$$V_{\text{oxdepinv}} = K_{1ox}\sqrt{\phi_s} + (V_{gs} - V_{th}) \tag{2.27}$$

Here V_{oxdepinv} , V_{aux}, ϕ_s are defined in[61] and parameters A, $T_{ox\ \text{Ratio}}$, B, TOXE, AIGC, BIGC, CIGC, NIGC in Eq.(2.25) and Eq.(2.26) are constants for a given technology and are independent of temperature. Since the gate-leakage transistor is operated in weak inversion(V_{gs}-V_{TH} is negative), the exponential term is very small, therefore approximating logarithmic function to the first order as $\log(1+x) \approx x$ we get V_{aux} function as

$$V_{aux} = NIGC \cdot v_t \cdot \exp\left(\frac{\text{V}_{\text{gs}} - V_{TH}}{NIGC \cdot v_t}\right) \tag{2.28}$$

Applying further approximation as done in [9], the exponential term in Eq.(2.25) can be approximated by a linear fit curve given by $f\left(V_{\text{oxdepinv}}\right) = K_2\left(1 + \alpha V_{\text{oxdepinv}}\right)$, where α is a constant whose value is small. The gate-to-channel current can be written as

$$I_{gc} = K_1 * K_2 * V_{gs} \exp\left(\frac{\text{V}_{\text{gs}} - V_{TH}}{K'}\right)(1 + \alpha V_{oxdepinv}) \tag{2.29}$$

Where $K' = NIGC.v_t, K_1 = W_{eff} * L_{eff} * A * T_{\text{oxRatio}} * \text{K}'$. Here W_{eff}, L_{eff} are the effective dimensions of the MOSFET. The total gate leakage current can be written as

$$\begin{aligned} I_g = {} & K_1 * K_2 * V_{gs} \exp\left(\frac{V_{gs} - V_{TH}}{K'}\right)\left(1 + \alpha V_{\text{oxdepinv}}\right) \\ & + K * V_{gs}\left(V_{gs} - V_{fbsd}\right) \end{aligned} \tag{2.30}$$

From Eq.(2.30), the temperature coefficient of gate current depends only on Vgs. PTAT voltage across the gate leakage mosfet results in non-linear PTAT current, seen in Fig 2.19b. This non-linear PTAT current improves circuit operation at higher temperatures as threshold voltage reduces. A PTAT current is needed for the PTAT and CTAT generator to function correctly. Gate leakage transistor operation for wide temperature range measured in [62].

2.4.2.2 Temperature Compensation

From Fig 2.18 V_{gs} across M0 is equal to V_{EB1} - V_{EB2}. As we know for a BJT V_{EB}=$V_T \ln\left(\frac{I}{I_{S2}}\right)$ Here, Q2 consists of n parallel units of Q1, so $I_{S2} = nI_{S1}$. V_{gs} across M0

is as follows,

$$\begin{aligned} V_{EB1} - V_{EB2} &= V_T \ln\left(\frac{I}{I_{S1}}\right) - V_T \ln\left(\frac{I}{I_{S2}}\right) \\ &= V_T \ln(n) \end{aligned} \tag{2.31}$$

This PTAT voltage across the gate leakage transistor generates the PTAT current shown in Fig 2.19 and helps bias the PTAT generator at higher temperatures. It also generates the CTAT voltage V_{EB1}, after the voltage divider, which works as an input to the PTAT generator. In conventional sub-BGR circuits, PTAT voltage is generated using BJT and resistors. Moreover, we need high resistance for ultra-low power IoT applications, which takes a large silicon area. This paper incorporates a differential pair and a current mirror-based structure to generate PTAT voltage [63]. As MOSFET operates in the subthreshold region, V_{GG} can be expressed as follows.

$$\begin{aligned} V_{\mathrm{GG}} &= V_{\mathrm{ref}} - \frac{1}{3}V_{\mathrm{EB1}} = V_{\mathrm{SG},M7} - V_{\mathrm{SG},M6} \\ &= V_{\mathrm{TH}} + \eta V_T \ln\left(\frac{I_{M7}}{K_{M7} I_0}\right) - V_{\mathrm{TH}} - \eta V_T \ln\left(\frac{I_{M6}}{K_{M6} I_0}\right) \\ &= \eta V_T \ln\left(\frac{K_{M5} K_{M6}}{K_{M4} K_{M7}}\right) \end{aligned} \tag{2.32}$$

Where, $I_0 (= \mu C_{\mathrm{OX}} (\eta - 1) V_T^2)$ is a process dependent parameter. K_{M6}, K_{M7}, K_{M4} and K_{M5} are the aspect ratios of the PMOS differential pair and the NMOS current mirrors, respectively.

$$\begin{aligned} V_{\mathrm{ref}} &= V_{\mathrm{GG}} + \frac{1}{3}V_{\mathrm{EB1}} \\ &= \eta V_T \ln\left(\frac{K_{M5} K_{M6}}{K_{M4} K_{M7}}\right) + \frac{1}{3}V_{\mathrm{EB1}} \end{aligned} \tag{2.33}$$

Considering the TC of V_{EB1} to be k_1, the TC of V_{ref} can be given as:

$$\frac{\partial V_{ref}}{\partial T} = \eta \frac{k}{q} \ln\left(\frac{K_{M5} K_{M6}}{K_{M4} K_{M7}}\right) + \frac{1}{3} k_1 \tag{2.34}$$

Therefore, a temperature-compensated voltage can be obtained by appropriately sizing the transistors M4-M7.

2.4.3 Results and Discussion

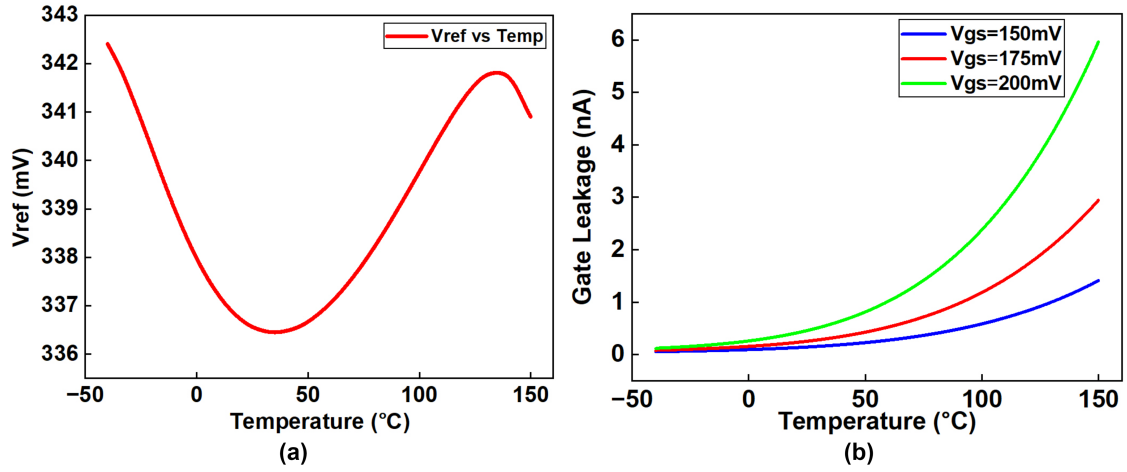


Figure 2.19: (a) Vref vs Temp (b) Gate leakage current vs Temp

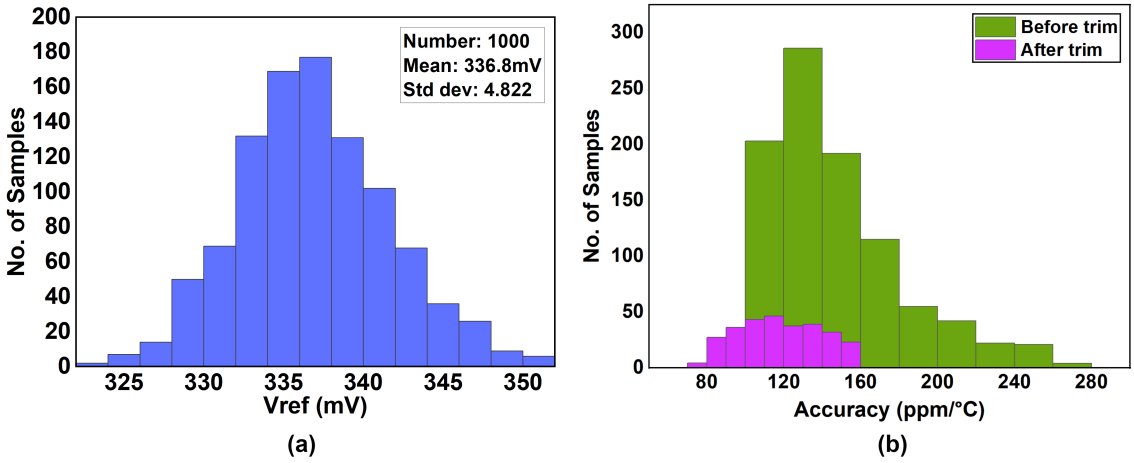


Figure 2.20: (a) MC of V_{ref} (b) MC of Accuracy pre and post trim

The 65nm CMOS process is used in the design and implementation of the suggested Sub-Bandgap reference. The reference voltage's temperature variation is displayed in Fig 2.19, which indicates that the reference's temperature coefficient (TC) is 94 ppm/°C. Monte-

Carlo simulation is used to illustrate the statistical results for both process and mismatch (1000 samples) for the Sub-Bandgap Reference. Concerning both process and mismatch, the V_{ref} variation is displayed in Fig 2.20. The observed mean and standard deviation are 336.8 mV and 4.822 mV, respectively, and this leads to a $\pm 3\sigma$ variation of 4.295%. The V_{ref} variation with respect to temperature (ranging from -40 to 150°) at various process corners is displayed in Fig 2.21a. One way to modify the variation of the TC and absolute value is to apply 1-point trim to the thin oxide gate leakage transistor M0. In this case, gate-boosted and low-leakage switches like [64, 65, 66] are used. Fig 2.21b provides post-trim findings of V_{ref} w.r.t temperature, demonstrating the efficacy of trimming throughout a broad temperature range and various process corners. The pre-trim result displays a mean and standard deviation of 153 ppm/°C and 49.01 ppm/°C, respectively, whereas the 1-point trim results in an improved mean and standard deviation of 117.7819 ppm/°C and 21.35 ppm/°C, respectively. Fig. 2.21b displays the accuracy results before and after trimming. This demonstrates that there is little loss of accuracy when using the suggested circuit even without trimming. As seen in Fig 2.22a, the PSRR at DC for the sub-Bandgap at 0.7V, 1V, and 3V are -57.17dB, -89.39dB, and -115.2dB, respectively.

By increasing the size of the gate-leakage-based capacitor at the expense of increased area, the power supply rejection ratio at higher frequencies can be enhanced. The line sensitivity at the SS, TT, and FF corners is seen to be 0.006623%/V, 0.0066%/V, and 0.00844%/V, respectively, in the supply range of 0.7V–4V, as shown in Fig 2.22. The power consumption only varies by 30x times in the temperature range of -40°C to 150°C at different supply voltages (Fig 2.23a) and by a factor of 1.025x over the supply range of 0.7V-4V (Fig 2.23b), due to the non-exponential character of the current. Fig 2.24 shows that the starter circuit's observed settling time for 99% of the steady state value is 21.89 ms. As shown in Fig 2.25, the proposed Sub-Bandgap reference configuration uses an active area

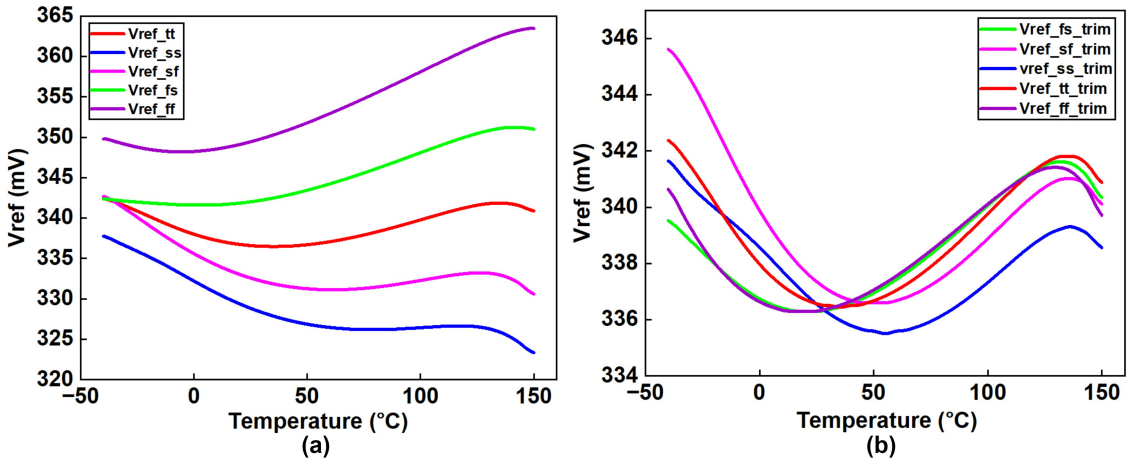


Figure 2.21: (a) V_{ref} at different corners w/o trimming (b) V_{ref} at different corners with trimming

Table 2.4: Comparison with State-of-the-Art Architectures

Specifications	**This Work**	[59]	[63]	[52]	[67]	[55]	[58]	[53]	[68]	[69]
Technology	**65nm**	180nm	180nm	180nm	65nm	180nm	180nm	180nm	180nm	65nm
Type	**Sub-BGR**	Sub-BGR	Sub-BGR	Sub-BGR	Sub-BGR	Vref	Vref	Sub-BGR	CMOS Vref	CMOS Vref
Vref (mV)	**336**	411.86	548	477	495	0.74(V)	1.048(V)	260	210	134
Temperature Range (^oC)	**-40 to 150**	-40 to 125	-40 to 120	-20 to 120	-40 to 120	0 to 170	-55 to 150	-50 to 85	-40 to 140	-40 to 125
TC (ppm/^oC)	**94**	33.7	114	51.2	42	27	45	95	82	18.1
Power Consumption	**2.3nW**	85nW	52.5nW	37nW	36nW	31.4pW	650pW	0.98nW	9.6nW	0.33nW
Power w.r.t temperature	**30x**	~1.187x	NA	1.017x	—	23584x	16160x	NA	~100x	2.16x
Start-up circuit	**Used**	Used	Used	Used	Used	Not used	Used	Not Used	Not Used	Not Used
Settling-time (ms)	**21.89**	NA	6	NA	5	1040	4.7	NA	NA	NA
Variation Coefficient σ/μ(%)	**1.435**	0.39	1.05	0.89	1.027	None	0.187	1.4192	0.31	3
Supply Range	**0.7V-4V**	0.9V-1.8V	0.7V-1.8V	0.8V-1.6V	0.5V-1V	0.9V-3.3V	1.5V-2.5V	0.65V-1.8V	0.4V-1.8V	0.9V-1.6V
Line sensitivity (%/V)	**0.0066**	0.06	6.47	0.0451	0.64	0.27	0.016	0.023	0.027	1.29
PSRR	**-89dB @ DC**	-61dB @10	-56dB @100	-58dB@50	-50dB@DC	NA	-71.8dB@100	—	-59dB@10	—
Area (mm^2)	**0.0851**	0.11	0.0246	0.034	0.0532	0.0076	0.0072	0.075	0.021	0.0046

of 0.0851 mm^2. Lastly, Table 2.4 presents a performance comparison between the suggested sub-bandgap reference and various cutting-edge voltage references.

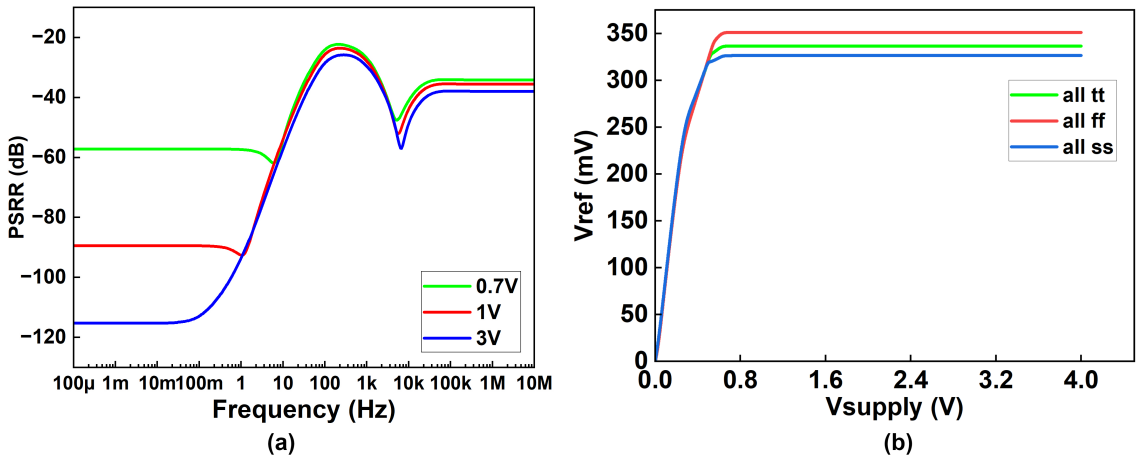


Figure 2.22: (a) PSRR of V_{ref} (b) Line Sensitivity of V_{ref}

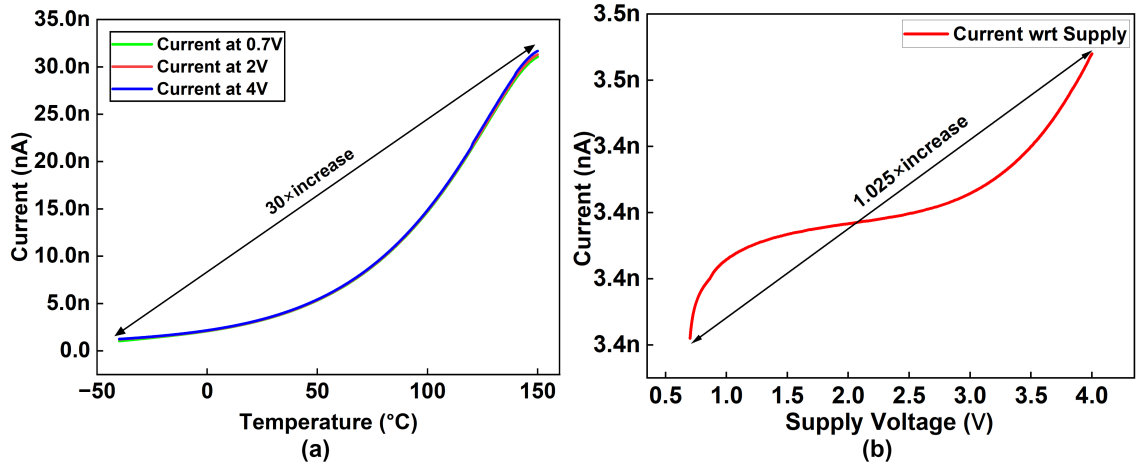


Figure 2.23: (a) Current vs temp at different supply (b) Current vs supply

2.4.4 Conclusion

This work offers a brand-new high-temperature range Sub-bandgap reference that generates the reference voltage utilising a single-stage PTAT voltage source created with an asymmetric differential pair and scaled CTAT voltage received from the BJT's base-emitter

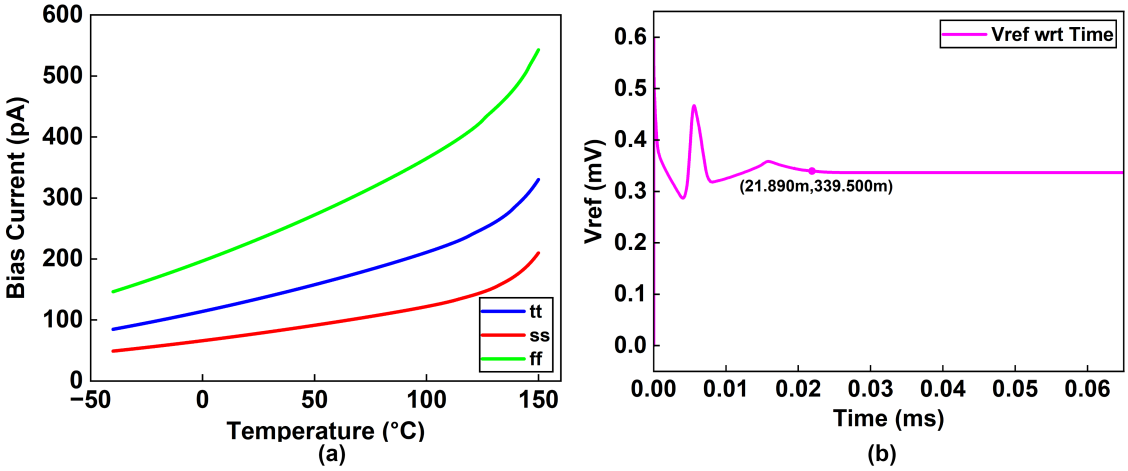


Figure 2.24: (a) Current Bias (b) Start-up time of V_{ref}

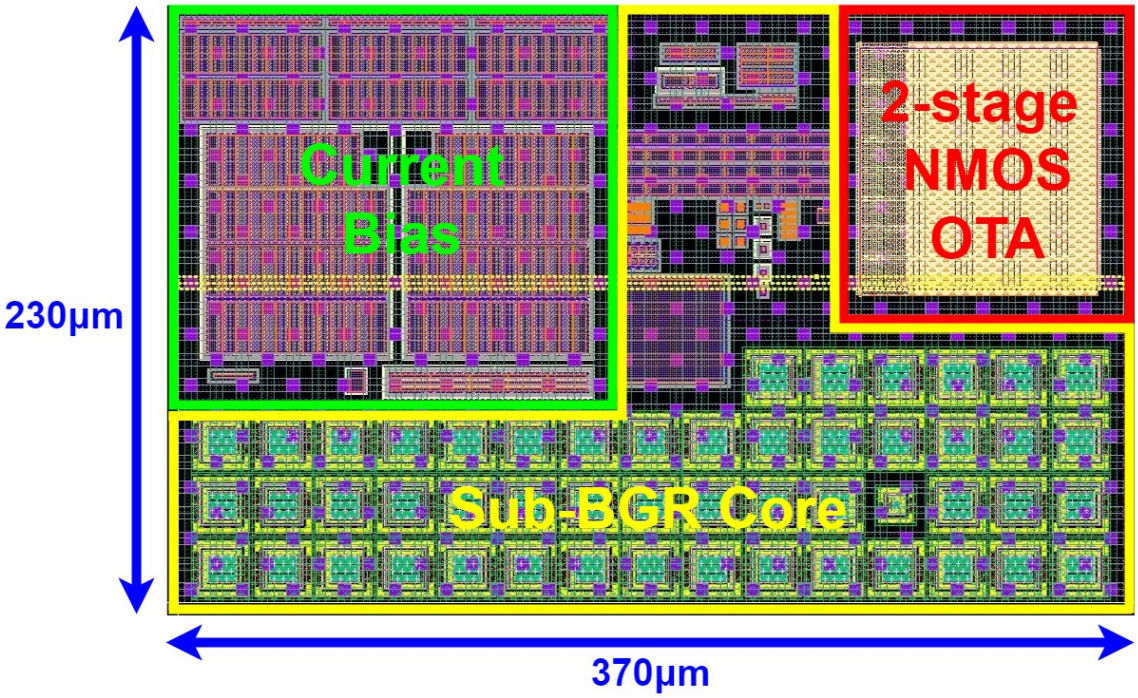


Figure 2.25: Layout of Proposed sub-BGR

voltage. Without the need for a native oxide transistor, the circuit has a state-of-the-art line sensitivity of 0.0066%/V while consuming only 2.3nW of power and running at a minimum supply voltage of 0.7V. It is appropriate for low-power and wide-temperature range applications due to its decreased power consumption range over temperature and supply as well as other competitive specifications.

Chapter 3

High-Frequency Cost-Effective On-chip CMOS VNA for Bio-molecule Detection

3.1 Introduction

Over a few decades, it has been observed that the development in medicinal diagnosis and detection of bio-samples, such as proteins, keratin, cellulose, etc., requires point-of-care (POC) diagnostics and Lab-on-a-Chip devices. [70, 71, 72, 73, 74, 75, 76] RF/Microwave-based sensors can be practical alternatives over biochemical sensors that offer several advantages like robustness, portability, accessibility, small sample volume requirement, and rapid testing, even on a large-scale necessity during a public health crisis. [77, 78, 79].

RF-based Biosensor-on-Chip (BoC) could bridge the gap between diagnostics in central laboratories and diagnostics at the patient bedside, bringing substantial advancements in Point-of-Care (PoC) diagnostic applications [80]. Integrating a biosensor on a single chip makes it possible to detect, analyze, and continuously monitor bio-samples in real-time. Integration can also reduce the overall size and complexity of the system, making it more portable and cost-effective. The system architecture of a BoC is shown in Fig 3.1.

A possible simple BoC solution for applications like bio-molecule detection is crucial to ensure accessibility and ease of use, making it more practical and efficient for researchers

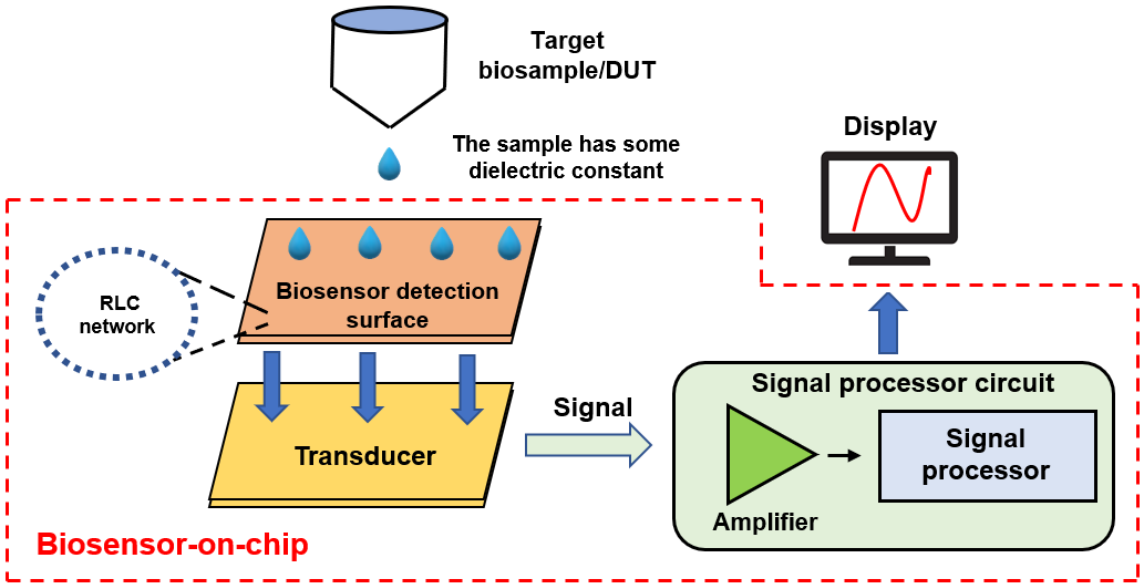


Figure 3.1: System architecture of biosensor-on-chip

and practitioners in various fields such as healthcare, biotechnology, and environmental monitoring. This can be achieved by exploiting the concept that when a bio-molecule binds to the surface of a biosensor, it changes the properties of the biosensor. This change can be measured and used to detect the presence of the bio-molecule. Various RF and microwave sensors have been developed for bio-sample detection, broadly categorized into resonant and non-resonant methods. Planar sensors, a subset of resonant RF sensing methods, particularly stand out due to their straightforward and compact design. [81] Planar resonant sensors such as inter-digitated capacitors (IDCs) are chosen for sensing and quantitative analysis of bio-liquids because of their high-quality factors and easy fabrication. When a bio-sample is placed over the IDC, the molecules bind to the electrode's surface, changing its effective capacitance.[81, 82, 83, 84, 85] The various bio-molecules with their permittivity are shown in Fig 3.2

The change in the capacitance of the IDC sensor is best measured using an ***on-chip Vector Network Analyser (VNA)*** [86]. One of the promising attempts of the VNA

Bio molecule	Dielectric Constant
Water	80
Acetonitride	42.3
Methanol	36.3
Ethanol	29.4
Acetone	25.2
Formic acid	58
Hexane	18.43
Chloroform	27.5
Formamide	109
Cyanide	158
Blood	50

Figure 3.2: Biomolecles with their relative permitivity

is the determination of the relative permittivity of bio-samples, human cancer cells, etc. [87, 88, 89, 90].

The paper aims to design an on-chip VNA for bio-molecule detection using IDC sensor. A compact, cost-effective, and accurate design of VNA holds great utility in bio-molecule detection due to the widespread application of bio-molecule analysis. Simplicity and ease in the detection scheme are paramount, making such VNAs an ideal choice for this purpose.

A non-tunable millimetre wave fully integrated on-chip VNA for detecting tumour cells working at 40 GHz has been proposed in [91, 92, 93, 94]. However, a tunable on-chip VNA can detect a broader range of bio-molecules, from small proteins to large DNA molecules, by adjusting its frequency range. This makes it more versatile, giving it higher sensitivity and accuracy. They also use a co-planar-based detection window that has much lesser sensitivity than the IDC sensor. The increased sensitivity can be advantageous when de-

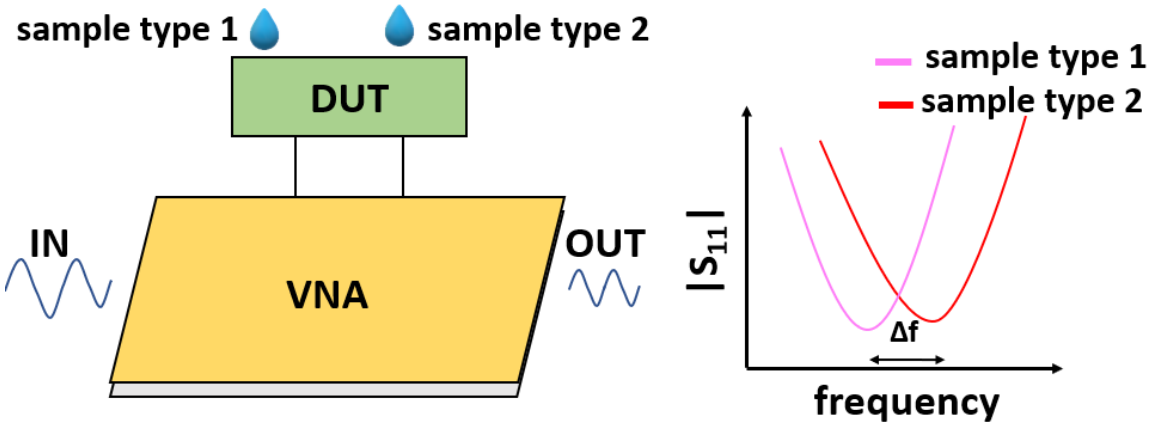


Figure 3.3: Detection principle and analysis of on-chip VNA

tecting subtle variations in capacitance. In [95], a micro-strip transmission line-based VNA working at a millimetre wave range of 50-100 GHz has been reported. While the design is tunable, it works at a high supply of 3.3V and uses a balun for single to differential signal conversion increasing the area and power. The design works at a millimetre wave range whose sensitivity is much less than micrometre-wave for bio-molecule detection. As lower frequencies can penetrate biological samples effectively, they allow interactions with molecules close to the sensor surface, making them more sensitive to capacitance-based sensors. Authors in [96, 97, 98] have designed a tunable on-chip VNA at a microwave range. [96, 97] used a co-planar waveguide for DUT, whereas [98] used an MSL-SIW detection window. These detectors have some disadvantages compared to IDC detectors, such as higher complexity, higher loss, lower sensitivity, limited frequency range, and limited scalability. [96, 97] uses SiGe chips that can offer performance advantages at high frequency but they come with higher cost, power consumption and complexity compared to CMOS chips.

All the state-of-the-art designs have disadvantages for bio-molecule detection. This work proposes a fully integrated tunable microwave range on-chip VNA working at 0.5 GHz to 2 GHz in a 65nm technology node. The detection principle and analysis of an

on-chip VNA are demonstrated in Fig 3.3. The design uses no BJT, or transmission line-based components giving us high measurement accuracy, dynamic range, power handling capability, and lower chip area. The design works from a low supply of 1V and consumes a total power of 41mW. It occupies an active area of $0.01767mm^2$. Chapter 3.2 briefly describes the proposed architecture and details about each block, Chapter 3.3 gives the results and discussion, and Chapter 3.4 concludes the topic.

3.2 Proposed Architecture

The proposed design is shown in Fig 3.4. comprises of the directional bridge for reference and reflected wave separation, a controlled oscillator (VCO) for generating varying frequency input signal, and an LNA for amplification of the signal. Fig 3.5 shows the RLC equivalent of IDC sensor used for simulation.

The design exploits the concept that the interaction of various samples with electromagnetic waves at different frequencies heavily depends on their unique dielectric properties. When a variable frequency input signal(f_{in}) generated from VCO is applied to the DUT(Design under test) containing the biosample, the phase and amplitude of the output signal will vary depending on its dielectric property. Therefore, by measuring the changes in the phase and amplitude of the output signal at different frequencies, the properties of DUT are extracted. From the properties of DUT, the type of sample is detected.

The electrical model of the DUT(IDC sensor) is represented in Fig 3.5 The capacitance of the IDC is varied depending on the biosample's dielectric property. The dependency of IDC's capacitance on the dielectric property of biosample is given by

$$C = \frac{\epsilon_0 * \epsilon_r * A}{d} \tag{3.1}$$

where ϵ_r is dielectric property of the bio sample. The change in capacitance of DUT will change its resonant frequency. At the resonant frequency, the impedance of DUT

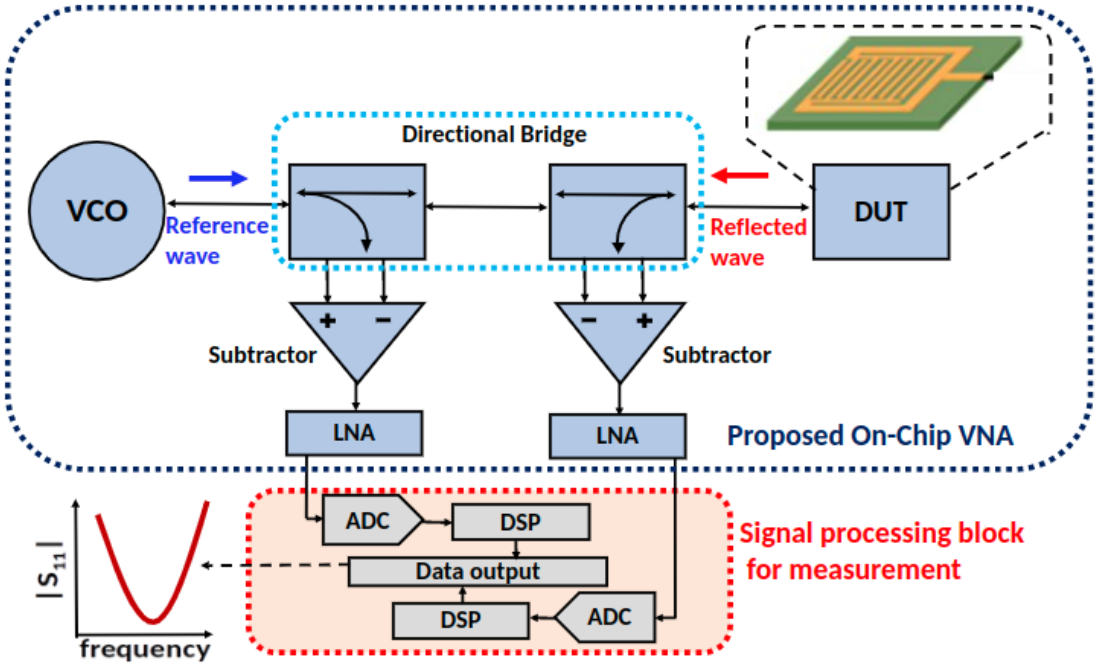


Figure 3.4: Proposed block diagram

reduces to pure resistive which is made equal to the channel impedance. So, when the frequency of the input wave matches with the resonant frequency of the DUT, it leads to impedance matching resulting in the least reflections. Therefore at the resonant frequency, the magnitude of the input voltage reflection coefficient of DUT ($|S11|$) will be at its lowest. The $|S11|$ of the DUT can be expressed in simple terms as:

$$|S11| = 20log\frac{|Reflected|\angle Reflected}{|Reference|\angle Reference} \tag{3.2}$$

From observing the variation of the magnitude of $|S11|$ the changed capacitance of the DUT is detected, which is back-traced to the dielectric property of the biosample using equation (3.2). In summary, the proposed design can identify the biosample using an IDC sensor by analyzing the variation of the magnitude of $|S11|$ of DUT to the input wave frequency.

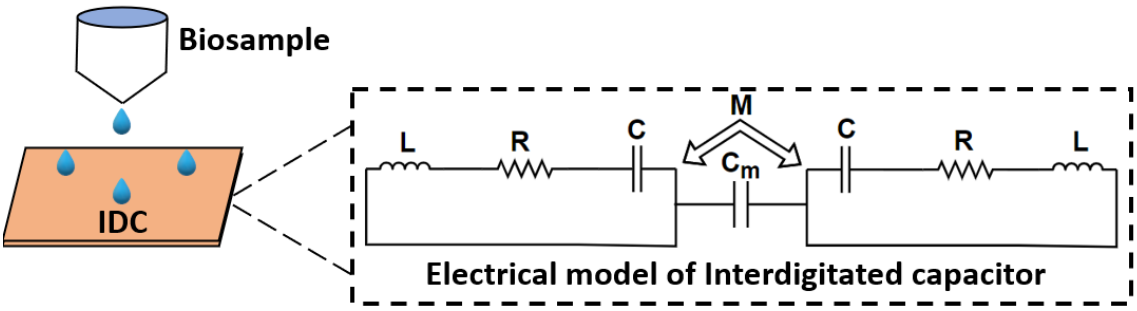


Figure 3.5: RLC equivalent of IDC sensor

Two separate LNAs with high linearity are used for reference and reflected waves to amplify and avoid further propagation of noise generated because of VCO. Analog-to-digital conversion, digital filtering, and signal process are performed at the back end for S-parameter measurements.

3.2.1 Directional Bridge

A directional bridge, or a directional coupler, is an electronic component that splits or combines signals in a transmission line [99]. The primary function of a directional bridge is to allow a portion of the power in a transmission line to be diverted to a secondary circuit or device while maintaining signal integrity and minimizing reflections. Its frequency-independent characteristic is the main advantage of using a directional bridge over a simple coupler design. The block diagram of the directional bridge is shown in Fig 3.6, where the reference and reflected wave are separated.

As in Fig 3.6 port 1 is the input port, port 2 is the transmitted port, and port 3 is the coupled port. The bridge splits the waveform at port 1 between ports 2 and 3. The black box connected between node A and port 1 is a subtractor circuit with high input impedance to avoid any current flow in the subtractor. A directional bridge works on the principle of the resistive divider. The directional feature of the bridge enables it to

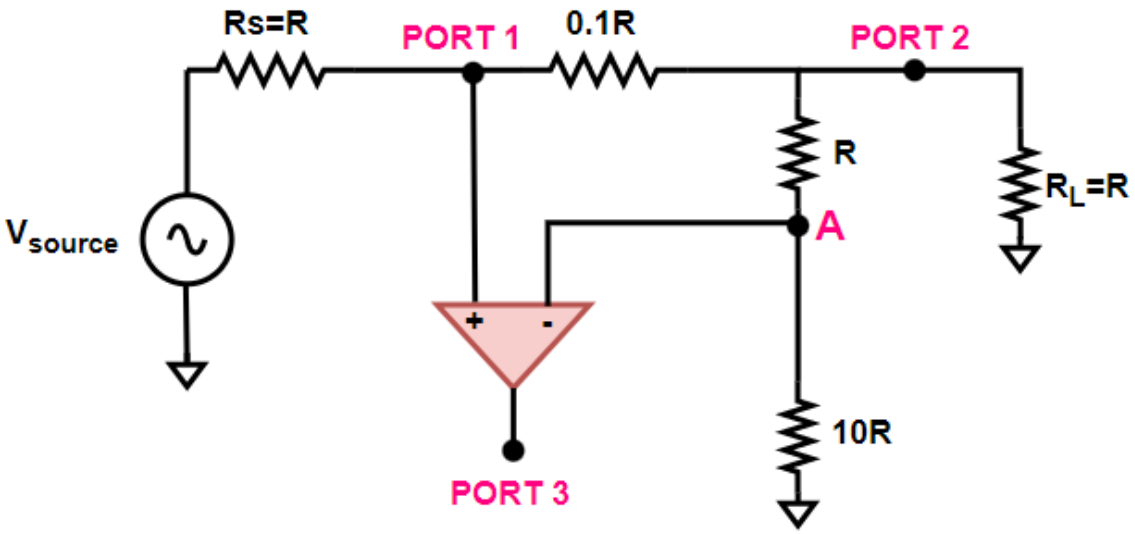


Figure 3.6: Schematic of a uni-directional bridge

differentiate between the forward and reflected waves in a transmission line, which allows it to accurately measure the impedance even in the presence of reflections.

The working of the bridge is depicted in Fig 3.7. Considering input at port 1, and assuming that the peak-to-peak voltage of the waveform is V at node B, the voltages at the other nodes are as follows:

$$\begin{aligned} V_B &= V(V) \\ V_C &= ((R||11R) + 0.1 * R) * V = 0.902 * V \\ V_A &= (\frac{10R}{10R + R}) * 0.902 * V = 0.82 * V \\ V_{PORT3} &= (1 - 0.82) * V \end{aligned} \tag{3.3}$$

The coupling coefficient(C) of the directional bridge is

$$\begin{aligned} C &= -20log(\frac{V_A}{V_C}) \\ &= -20log(0.18) \\ &= 14.89dB \end{aligned} \tag{3.4}$$

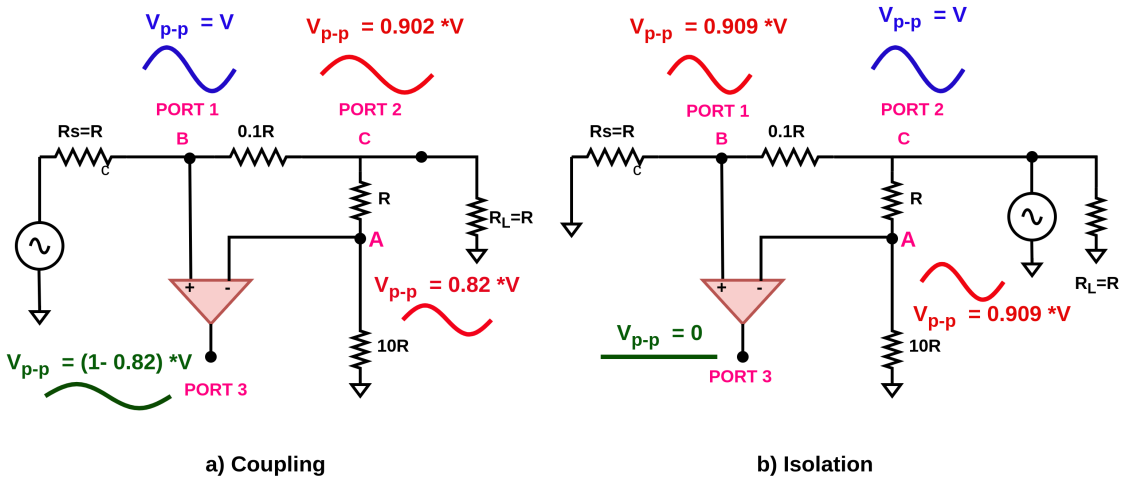


Figure 3.7: Working of a directional bridge

When the input is from port 2 let the voltage at node C be V. Then voltages at the other nodes are as follows:

$$\begin{aligned} V_C &= V(V) \\ V_B &= (\frac{R}{R+0.1R}) * V = 0.909 * V \\ V_A &= (\frac{10R}{10R+R}) * V = 0.909 * V \\ V_{PORT3} &= 0 \end{aligned} \tag{3.5}$$

So the directional bridge completely isolates port 3 from port 2.

In the above discussion, we have considered the black box as a subtractor with a very high input impedance configured to respond to a voltage difference between two nodes of the bridge network. Various types of designs are used for achieving the operation of the black box like a passive transformer, passive diode, power sensing device, a direct current coupled (DC coupled) differential amplifier with a high common mode rejection ratio, Gilbert Cell mixer with differential radio frequency input, other mixers or samplers with differential RF inputs, or an integrated transformer or balun. Using a differential mixer

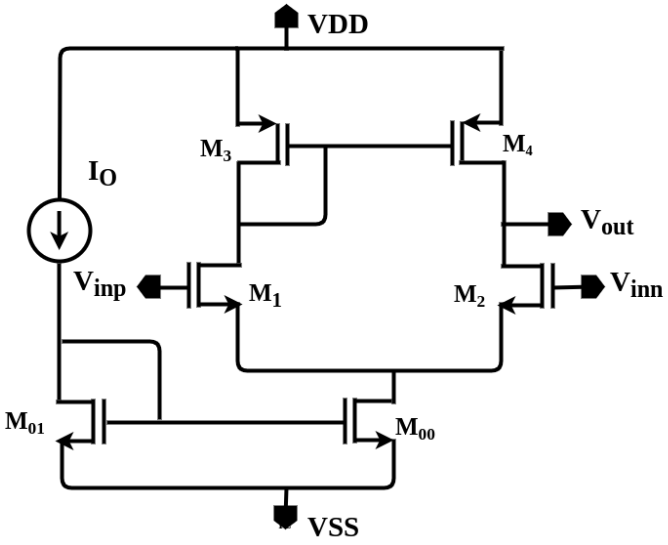


Figure 3.8: Schematic of Differential amplifier

may lead to one potential disadvantage in terms of complexity, which can increase the cost and power of the overall system. It can also introduce additional noise and distortion compared to a single-ended mixer, reducing the overall signal quality and limiting the system's performance.

The challenge of interfacing differential RF circuits to single-ended ones has been with the RF (and other) design community for many years.

The working of the bridge demands a differential to a single-end converter whose output is the coupled port. Various inductive designs are used for achieving the operation like a passive transformer, passive diode, integrated transformer or balun.

These device gives a disadvantage of high EMI, high area and low input impedance leading to the degradation of the working of the bridge. The above issue can be solved by using a differential amplifier with high ICMR Fig 3.8. The differential amplifier achieves a DC gain of 80dB with a UGB of 2.5GHz and a phase margin of 60°. It works for a wide ICMR of 0.2-0.65V.

3.2.2 Low Noise Amplifier

An LNA (Low-Noise Amplifier) is an essential component for designing an on-chip VNA (Vector Network Analyzer) because it amplifies the received signal with minimal added noise. As the frequency range is in Giga Hertz, noise can have a noticeable impact on the signal signifying the use of a low-noise amplifier instead of a general amplifier. The design of an LNA involves achieving the desired gain, noise figure, and stability by using various techniques. LNA achieves low noise amplification by using a combination of circuit design techniques and component selection to minimize the amount of noise that is added to the signal. These techniques include using a low-noise transistor, optimizing the matching network, using negative feedback, and implementing a bias circuit. Multiple LNA architectures are used depending on the application and its specifications. [100]

Most LNAs include inductors for their operation. While inductors have many advantages in electronic circuits, such as storing energy and filtering signals, there are several disadvantages to having inductors in on-chip circuits. Some of the disadvantages include size and complexity, parasitic effects, limited frequency range, and sensitivity to process variations. The LNA used in the design is shown in Fig 3.9. The LNA is a modified design of [100] where a CS amplifier replaces the end buffer for a better gain and output matching that is independent of MOSFET parameters.

The LNA is designed using a resistive feedback technique, which replaces the inductors with resistors to achieve a smaller die area, better linearity, and higher gain. The proposed design includes a low-pass filter to improve the linearity of the LNA and a cascade configuration to increase the gain. The use of resistive feedback topology and cascade configuration in the LNA design can help reduce noise. In a resistive feedback topology, the input signal is divided into two paths: a forward path and a feedback path. The feedback path includes a resistor connected between the output and input nodes of the amplifier, creating a negative feedback loop. The two paths create noise in opposite phases and gain in the same phase with the help of a CG amplifier. On adding the two the noise is reduced

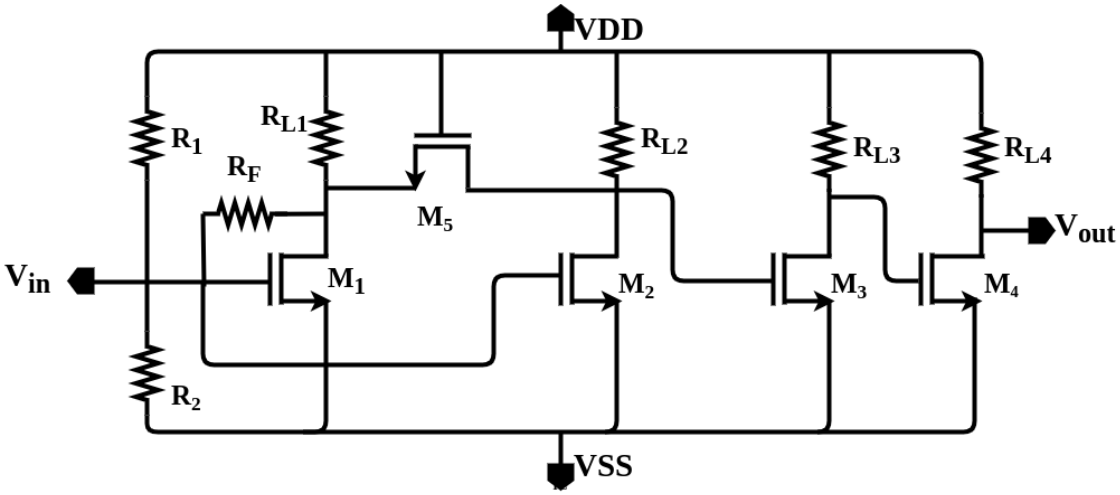


Figure 3.9: Schematic of LNA

significantly. In addition, the use of a cascade configuration in the LNA design can help improve noise performance. The effective noise figure for cascaded blocks is given by

$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 * G_2} ... \tag{3.6}$$

where F_1 is the noise power of stage 1 and G_1 is it's gain. It can be seen that the first stage has a higher impact on noise which is reduced by using resistive feedback. The high gains of subsequent stages reduce their effect on noise. The input and output impedance of the block is

$$\begin{aligned} Zin &= \frac{RF + 1/gm_5}{1 + (gm_1/gm_5)} \\ Z_{out} &= R_{l4} || rds_4 \end{aligned} \tag{3.7}$$

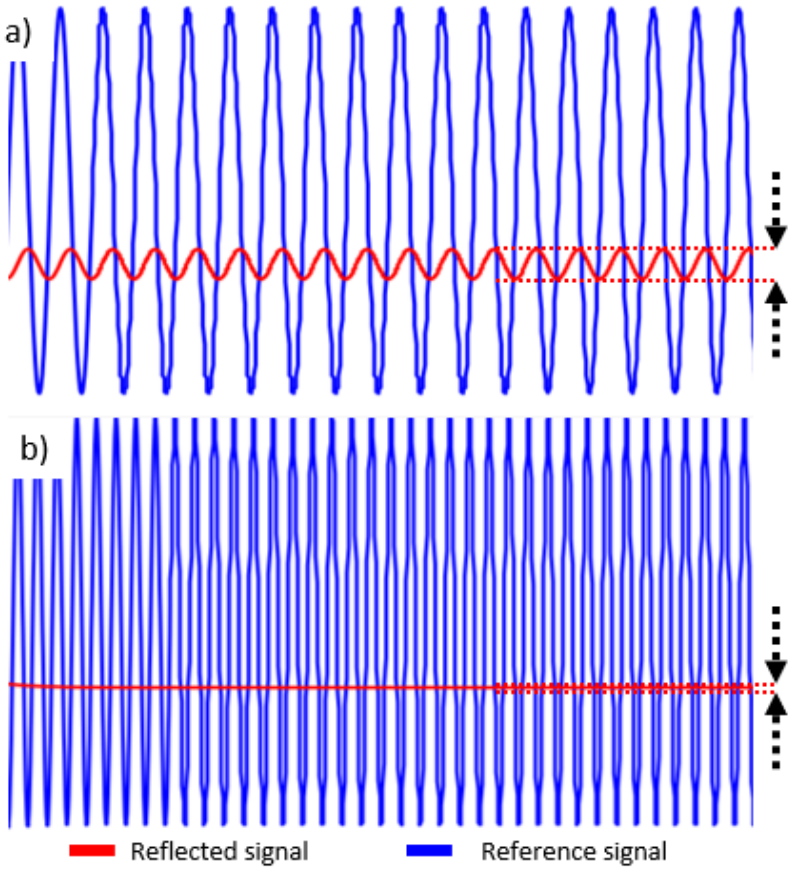


Figure 3.10: The reference and reflected waveform for water molecule at a) 10GHz b) 25GHz showing that at 25GHz the reflections are the least

3.3 Results and Discussion

Fig 3.10 represents the reflected and reference waveform of water whose dielectric constant is 80 as bio-molecule at two different frequencies. For proof of concept, water is taken as a reference bio-molecule. The IDC sensor has been modelled as below and is

represented with an LC circuit.

$$\begin{aligned} \frac{A}{d} &= 0.035cm \\ L &= 1nH \end{aligned} \tag{3.8}$$

giving a capacitance of 25pF for water molecules. When the input reference waveform has a frequency of 1GHz there will not be any reflections from the IDC as it reaches resonance which can be seen in Fig 3.10. It is evident that the S_{11} for water molecule will be at least at 1GHz when compared with any other frequency, giving us a peak as shown in Fig 3.11.

The above design works for a range of 0.5G-2.5GHz and detects bio-molecules whose dielectric constants can be in the range of 12.8-320. Bio-molecules with dielectric constants in the above range are also diverse in terms of their composition and function. This range encompasses a wide variety of bio-molecules including proteins, nucleic acids (DNA and RNA), carbohydrates and lipids among others. Some of which includes Acetonitride(42.3), Methanol (36.3), Ethanol(29.4), Acetone(25.2), Formic Acid(58), Hexane(18.43), Chloroform(27.5), Cyanide(158), Blood(50) etc that are mostly used in daily labs.

Fig 3.11 depicts the S11 obtained for three different bio-molecules. Each bio-molecule has a peak at a different frequency depending upon its dielectric constant. Taking this frequency the dielectric constant can be calculated using the formula:

$$\begin{aligned} C &= \left(\frac{1}{2 * \pi * f * \sqrt{L}}\right)^2 \\ \epsilon_r &= \frac{C * d}{\epsilon_0 * A} \end{aligned} \tag{3.9}$$

Where C is the capacitance of the bio-molecule, L is the inductance offered by the IDC sensor, f is the resonant frequency, and d and A are the sensor parameters. So from equations 3.8 and 3.9, the bio-molecules in Fig 3.11 give peaks at 1.59GHz, 1GHz and 0.71GHz whose IDC capacitance can be calculated as 10pF, 25pF and 50pF respectively. The dielectric constants of each can be further calculated as 32, 80 and 160, and using the values bio-samples can be detected as to be DNA, water and cyanide respectively.

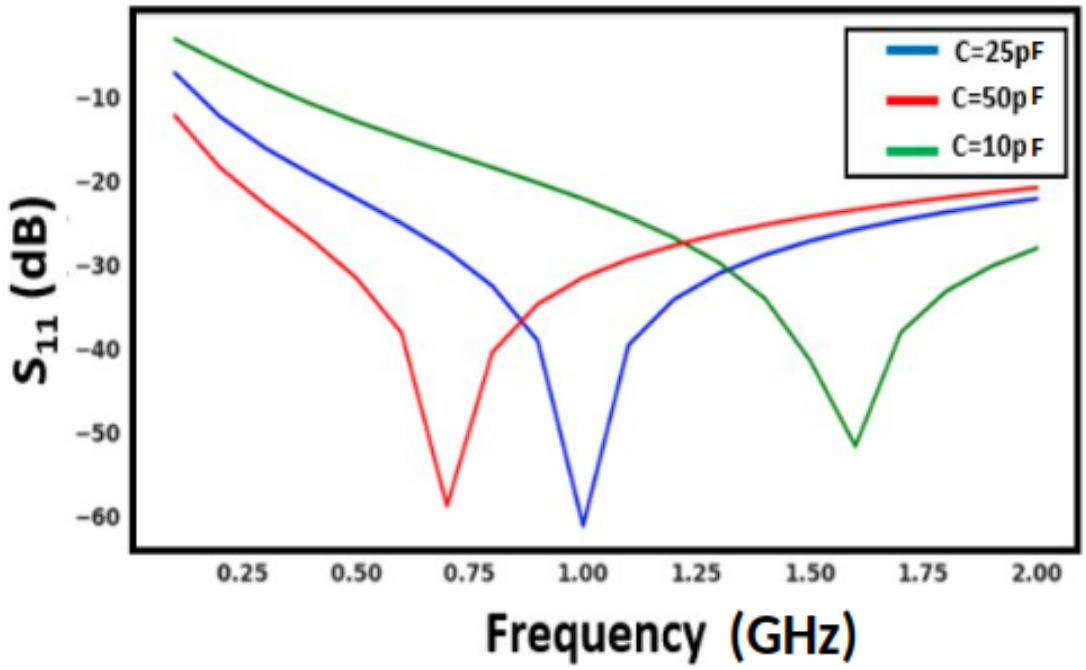


Figure 3.11: S_{11} vs frequency graph showing the variations of the peak with different capacitance of IDC sensor that changes with the bio-molecule used

The layout of the design is shown in Fig 3.12. It occupies an area of $0.01767mm^2$ (188um x 98um). Table 3.1 shows the comparison of the proposed design with a general-purpose VNA design and application-specific VNA design. [101] is used for the application of tumour cell analysis that uses a co-planar-based detection window and [102] is a general purpose on chip VNA designed. The design in [101] is not tunable and works for 40GHz occupying an area of $4mm^2$ which is much higher than the area of our proposed design chip. The design in [102] uses SiGe chip that has higher costs and has increased the power consumption to 640mW and also has a higher area of $1.8mm^2$ than our proposed design.

Table 3.1: Comparison with State-of-the-Art Architectures

Specifications	**This Work**	[101]	[102]
Target	**Bio-molecule detection**	Tumor cell analysis	General purpose
Technology	**CMOS 65nm**	CMOS 65nm	SiGe chip
Frequency range	**0.5-2.5GHz**	40GHz	0.01-26GHz
Supply(V)	**1**	-	3.3
Power(mW)	**41**	24.8	640
Area(mm^2)	**0.01767**	4	1.8

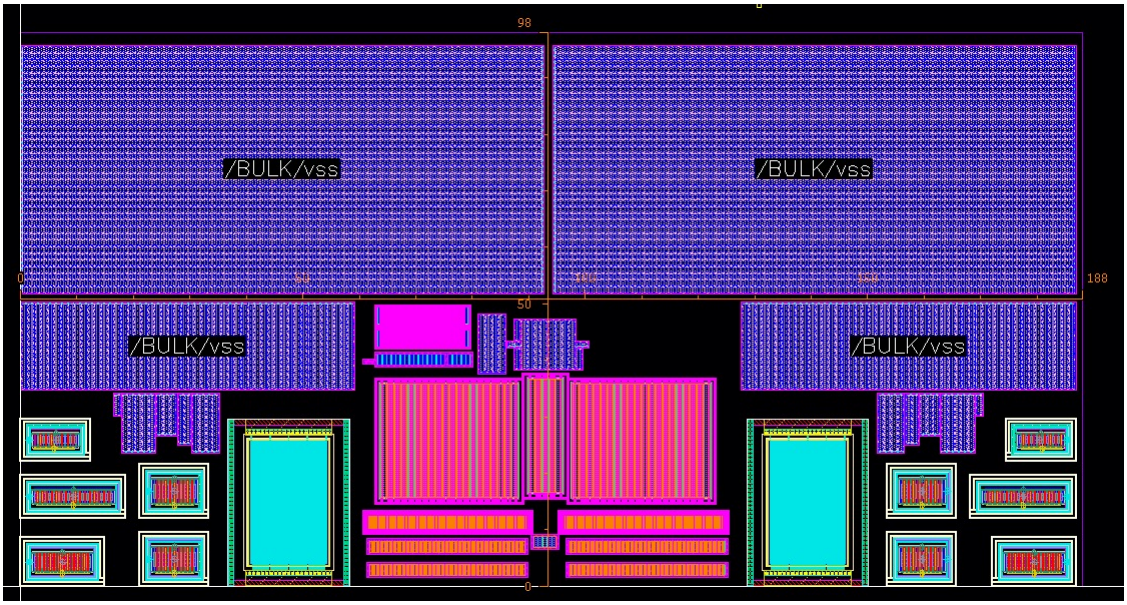


Figure 3.12: Layout of the design

3.4 Conclusion

This work presents a fully integrated inductor-less on-chip CMOS VNA (Vector Network Analyser) designed in 65nm CMOS technology to detect the bio-molecule. The proposed design works in a tunable frequency range of 0.5GHz to 2.5GHz, thereby ensuring much higher precision compared to the VNA working at a higher frequency range. The design can sense bio-liquids whose dielectric constants are in the range of 12 to 320. The proposed design provides a simple, low-area, compact and accurate solution for bio-molecule detection that holds great utility due to its widespread application.

Part - II

Self Adaptive Methodology for PVT Variations

Chapter 4

ML Driven Self-Adaptive Loop to Reduce Post Fabrication PVT Variations

4.1 Introduction

Analog and RF circuits are hampered by Process, Voltage, and Temperature (PVT) variations stemming from manufacturing inconsistencies, voltage fluctuations, and temperature changes. These variations cause deviations in circuit parameters, leading to performance degradation and reliability issues such as signal distortion and reduced dynamic range. Furthermore, PVT variations accelerate ageing mechanisms like bias temperature instability (BTI) and hot carrier injection (HCI), impacting long-term reliability.

To combat these challenges, techniques such as process-aware design, adaptive biasing, and calibration circuits are employed. These methods compensate for variations in operating conditions and ensure consistent performance across different process corners. In the realm of automated analog circuit design, various techniques have emerged, encompassing circuit topology selection, circuit parameter optimization, and layout generation. Among these approaches, circuit parameter optimization stands out as particularly appealing. This method is favoured due to its well-defined nature as a constrained nonlinear optimization problem, making it amenable to solutions by established optimization algorithms.[103] By focusing on refining circuit parameters to meet specified constraints and objectives, this op-

timization technique enables the generation of high-quality analog circuits with enhanced performance and reliability. Machine learning (ML) is particularly effective when employed for optimization tasks like developing optimised designs, which can be further extended, especially in the calibration of variations.[104, 105]

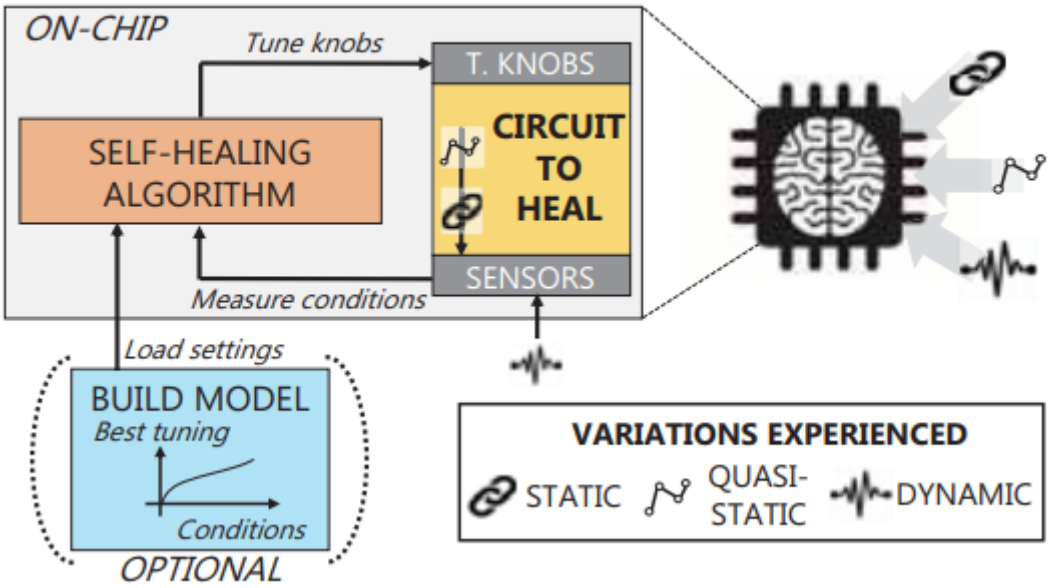


Figure 4.1: Methodology of Self adaptation [5]

[5] has classified the variations into three categories as

1. ***Static Variations:*** These variations have a one-time impact on the circuit and remain constant thereafter. They are typically caused by manufacturing discrepancies or defects.

2. ***Quasi-Static Variations:*** Quasi-static variations slowly affect the circuit over time. Examples include aging effects or stress-induced changes.

3. ***Dynamic Variations:*** Dynamic variations exert rapidly changing influences on the circuit. This category encompasses variations due to temperature fluctuations, voltage changes, and shifting operating conditions.

and based upon the variations tackled by various techniques, the techniques are classified as:

1. ***Self-calibration:*** These techniques are designed to compensate for static variations exclusively, such as manufacturing discrepancies or defects.

2. ***Self-healing:*** Capable of addressing both static and quasi-static variations, self-healing methods tackle challenges such as ageing or stress-induced variations.

3. ***Self-adaptation:*** These techniques offer the broadest scope, addressing static, quasi-static, and dynamic variations. They are adept at handling dynamic operating conditions and channel impairments, providing robust compensation across a wide range of scenarios. Fig 4.1

The thesis will follow the above classification for referring to the state of the arts.

Although [5] gives a detailed idea about various advantages of self-adaption, the fact that power consumption for on-chip self-adaptation is more than 100mW is very concerning. As higher power dissipation generally incurs increased manufacturing costs due to various factors. [106] propose an on-chip self-calibrating Die learning machine to reduce costs. A Low-Noise Amplifier (LNA) was designed and fabricated in IBM's 130nm RF CMOS process, where the dataset for ML was generated after fabrication. They have generated a huge dataset of 444,528 samples, which consumes a huge time. [107] proposes a one-shot off-chip self-calibration method using machine learning. In such a methodology, the best combination of tuning knobs can be even found in a unique test iteration using machine learning that includes both process and tuning variations. The technique is demonstrated on a 65nm RF power Amplifier. Since the calibration is post-fabrication, the test pattern generation would take more time. The calibration approach may fail in

the presence of defects within the circuit as they use non-intrusive sensors. There are other papers [108, 109] that don't use Machine learning-based optimisation. [108] proposes an analog/RF interference cancellation technique that can autonomously adapt itself to time-varying interference channels using a Least-mean square (LMS) adaptive loop. The above technique has been prototyped on a 0.5-to2.5-GHz full-duplex (FD) MIMO RX is designed and fabricated in a 65-nm CMOS process. Although the above technique has an edge over the ML optimisation technique over time and power, it is limited to the type of architecture. [109] is a LUT-based calibration. It also has the disadvantage of memory consumption and design architectural dependency.

All the above papers are limited to self-calibration, dealing only with process variation. The papers [110, 111] present a self-adaptive technique for tacking PVT variations. [110] introduces a simulation-based method for synthesizing analog circuits, aiming for minimal user effort and topology independence. Instead of relying on a commercially available simulator, the authors implement an accelerated simulator called SPASE, optimized for analog circuit synthesis. [111] proposes a simulation-based optimization approach named smart-multiple starting point that verifies the result for opamp, VCO and charge pump. The above self-adaptive references are simulation-based.

In the below chapter, we are proposing a simulation-based ML-driven self-adapting loop for the Cadence environment. The ML model predicts the trim bits for tuning the design with an accuracy of 0.99, even with a small dataset of 2k samples. The architecture has been verified on 2 LNA designs working at 1GHz and 25GHz each, respectively. Section 4.2 presents the architecture in detail and its implementation on two LNA circuits. Section 4.3 briefly discusses the ML technique, and Section 4.4 provides the results of the technique.

4.2 Proposed Architecture of the Loop

The proposed architecture, depicted in Fig 4.2, is accessed and simulated using Cadence schematic design tools, with the ADE-L window serving as the interface for simulation control.

Within the schematic, a control circuitry constantly observes the PVT conditions to adjust design parameters. This adjustment process relies on trim bits provided by the machine learning (ML) model, utilizing constant inputs such as PMON frequency, supply voltage, and temperature. A typical ADE-L window layout is shown in Fig 4.3, responsible for assigning values to variables, specifying analysis types, and selecting output expressions.

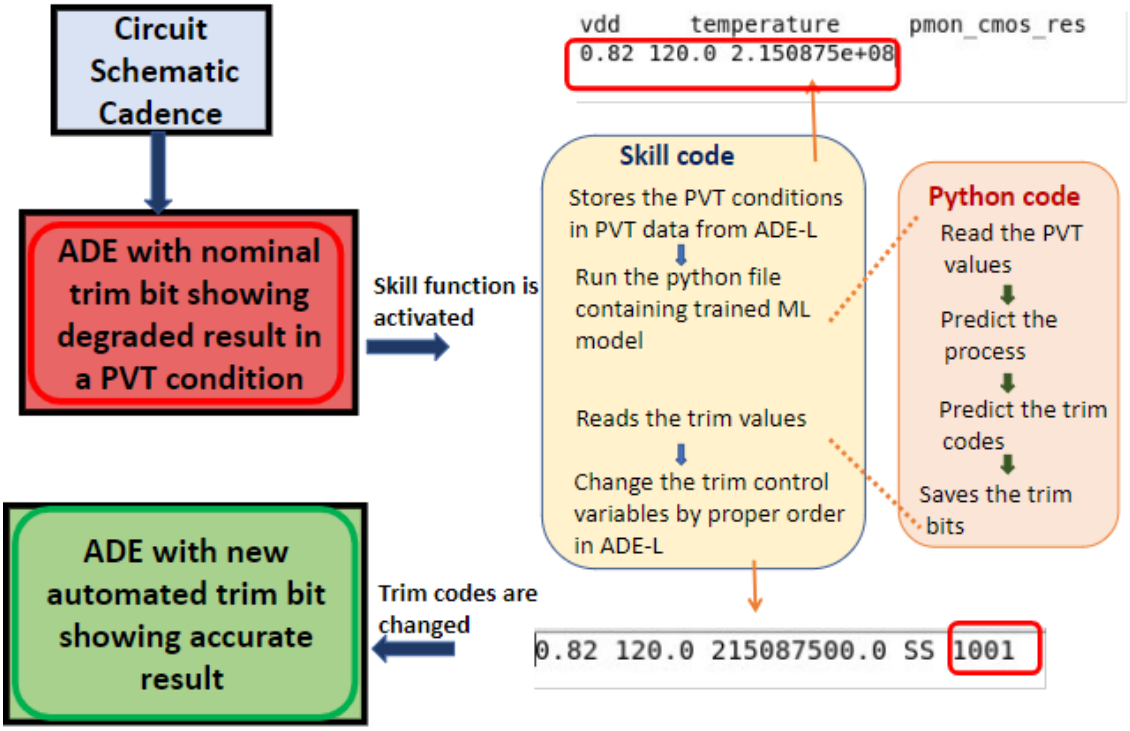


Figure 4.2: The proposed self-adaptation loop

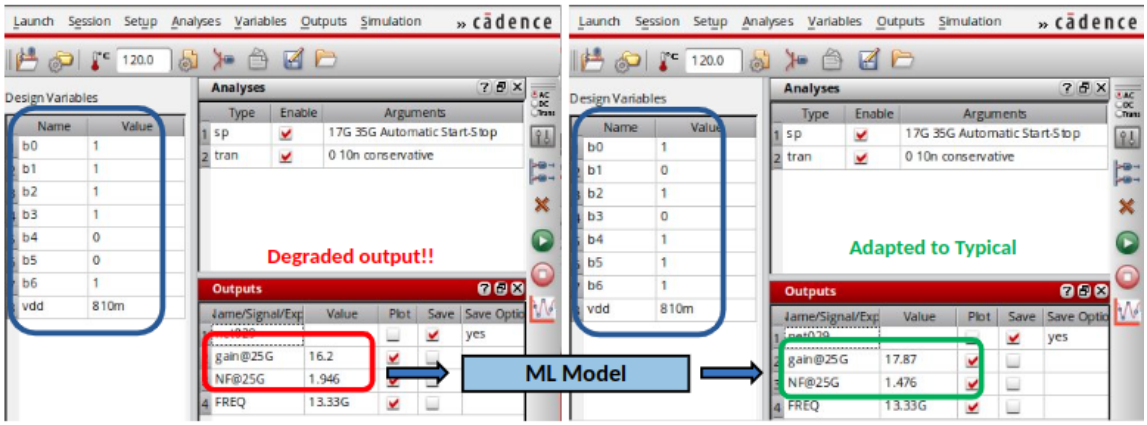


Figure 4.3: Sample ADE-L of cadence environment

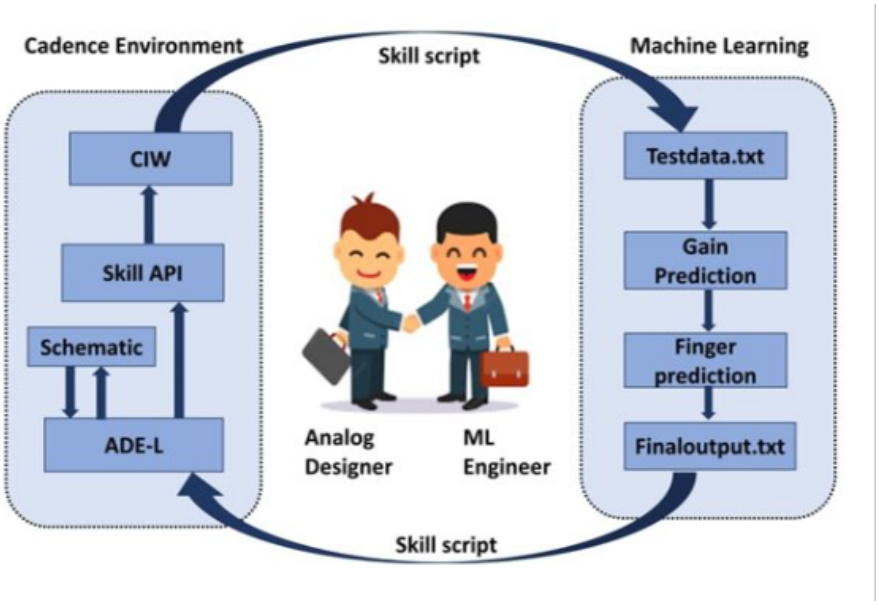


Figure 4.4: Skill code forming bridge between Analog design and ML model in CADENCE environment

For simulation purposes, these trim bits are treated as variables within the schematic. Thus, the schematic incorporates control circuitry that dynamically adjusts design variables based on trim bits received from the ADE-L window. However, using nominal trim bits

initially may yield suboptimal results. Therefore, the ADE-L window gathers process (P), voltage (V), and temperature (T) data, utilizing Skill functions to extract this information.

A Skill function stores these conditions in a file and invokes a Python script housing the pre-trained ML model. The Python script reads the conditions, executes the ML model, and predicts the optimal trim code. The Skill function then adjusts the design variables according to the newly predicted trim bits, facilitating accurate results under varying PVT conditions.

As depicted in Fig 4.4, the Skill code serves as a crucial bridge between the analog schematic and the ML model, enabling dynamic adaptation of the design parameters to ensure robust performance across different environmental conditions. The below chapter will discuss the circuits on which the loop has been tested.

4.2.1 Circuits Designing

In this study, we focus on low-noise amplifiers (LNAs) used in receivers, which can be affected by temperature changes. We use machine learning (ML) to adjust the biasing of LNAs based on temperature readings, ensuring they work well in different conditions. The gain of LNAs is crucial for their performance in various tasks. It relies on MOSFET characteristics and can vary due to different conditions, so we need to calibrate it carefully. Our self-adaptive LNA keeps its low-noise features even in extreme temperatures, ensuring it works reliably in tough environments.

4.2.1.1 Low Noise Amplifier Working at 1GHz

The resistive feedback topology in the Low-Noise Amplifier (LNA) design plays a key role in reducing noise. This configuration, using resistors in the feedback loop, contributes to minimizing unwanted noise in the amplifier. The resistive feedback technique helps achieve a balance between signal amplification and noise figure, ensuring that the amplifier adds as little noise as possible to the incoming signal. The second stage of the CS amplifier

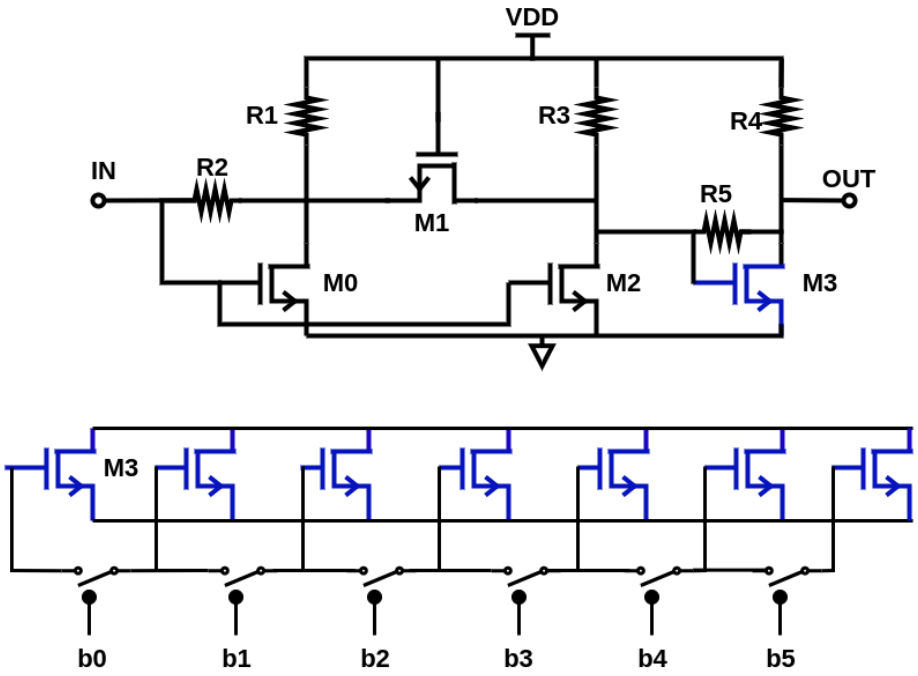


Figure 4.5: Resistive feedback LNA working at 1GHz

is added to increase the gain and maintain an output impedance of 50 Ohms. The LNA is designed using a resistive feedback technique, which replaces the inductors with resistors to achieve a smaller die area, better linearity, and higher gain. The proposed design includes a low-pass filter to improve the linearity of the LNA and a cascade configuration to increase the gain.

The designed LNA, as shown in Fig 4.5 achieves a gain greater than 14dB, an NF less than 3.21dB, and a linearity of -13dB for the required frequency of 1GHz in 60nm technology node.

The PVT spread of gain has been from 7dB to 20dB, which is reduced by using ML. To have the advantage of tuning the gain without having much effect on other parameters, the MOSFET at CS amplifier stage has been self-adapted using ML. The control circuit

comprises a 6-bit tuning to the multiplier of the MOSFET. The PVT spread of gain +/- 20% has been reduced to less than 1% using ML- self-adaptation.

4.2.1.2 Low Noise Amplifier Working at 25GHz

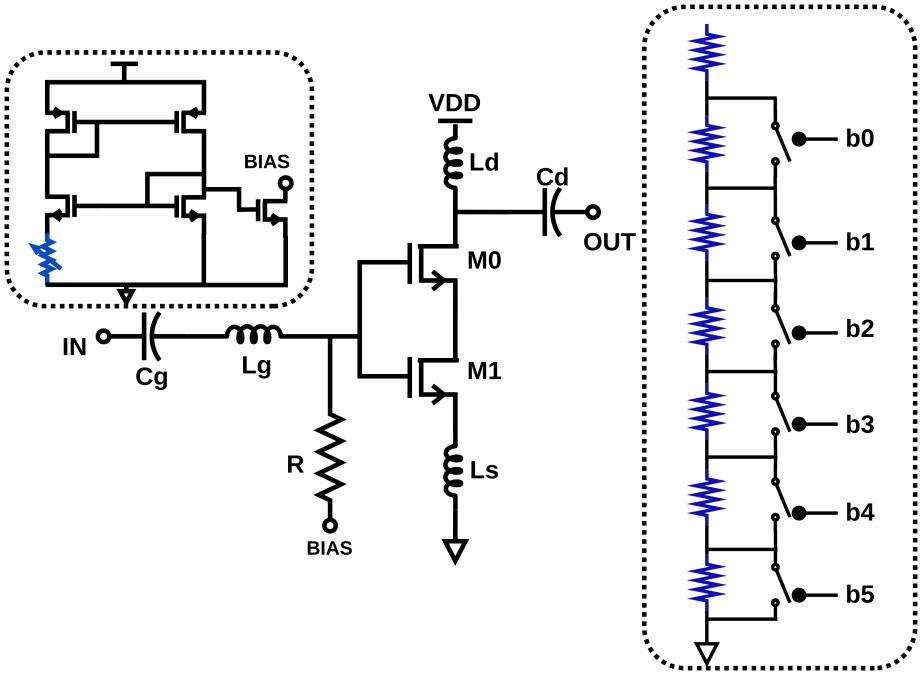


Figure 4.6: CS with source degeneration LNA working at 25GHz

We have also verified the methodology on Common source with source degenerated LNA as shown in Fig 4.6.

A common configuration for LNAs is the common source (CS) topology with source degeneration. This configuration offers several advantages in RF circuit design. Firstly, the addition of source degeneration helps improve the linearity and stability of the amplifier by providing negative feedback. This helps mitigate variations in transistor parameters and enhances the overall performance of the LNA, particularly in high-frequency applications. Secondly, the source degeneration resistor helps in setting the gain of the amplifier, mak-

ing it easier to control and optimize for specific design requirements. Additionally, this configuration provides better matching and impedance transformation, which is beneficial for interfacing with subsequent stages in the RF signal chain.

The characteristics of LNA are highly dependent upon the bias current flowing through it, which is given by a beta-multiplier circuit. Hence, the resistor of the beta-multiplier is tuned to achieve optimum results across various conditions. The ML model has been pre-trained to optimise two major outputs: Gain and NF.

The LNA is designed in 28nm technology node, with a gain of 18dB, NF of 3dB and an IIP3 of -15dB. The power dissipation of the design is 7.8mW. Both gain and NF are tuned simultaneously, verifying that IIP3 is greater than -20dB.

Before adaptation, the variation of Gain is from 15.443dB to 19.542dB, NF is from 1.0154dB to 2.484dB, and IIP3 is from -19.23dB to -8.005 dB. The PVT conditions encompass a supply variation of +/-10% across SS, TT, and FF process corners, as well as temperatures ranging from -40°C to 125°C.

4.3 Machine Learning Algorithm for Self Adapting

Both the LNAs above use the LGBM machine-learning algorithm [112]. "LGBM" stands for Light Gradient Boosting Machine, which is a type of machine learning model. It belongs to the family of gradient-boosting algorithms and is known for its efficiency and effectiveness in handling large datasets and high-dimensional features. LGBM is particularly popular in various machine-learning competitions and real-world applications because it trains quickly and produces accurate predictions. It works by building an ensemble of weak learners (typically decision trees) sequentially, with each subsequent learner focusing on the mistakes made by the previous ones. This iterative process continues until the model achieves optimal performance. LGBM incorporates several optimizations to enhance speed and efficiency, making it a powerful tool for various tasks such as classification, regression, and ranking.

The training details include the utilization of the LGBM algorithm with Mean Squared Error (MSE) serving as the cost function. The parameters for different components are specified as follows:

1. **LNA working at 1GHz:**

   Gain: Learning rate of 0.12, bagging fraction set to 0.05, with a total of 50 leaves, R2Score of 0.99.

   LNA Fingers: Learning rate of 0.1, bagging fraction set to 0.8, with a total of 5 leaves, R2Score of 0.99.

2. **LNA working at 25GHz:**

   Gain: Learning rate of 0.12, bagging fraction set to 0.05, with a total of 50 leaves, R2Score of 0.979.

   NF: learning rate of 0.15, bagging fraction as 0.8, no. of leaves of 10, R2Score of 0.99.

   LNA Fingers: Learning rate of 0.15, bagging fraction set to 1, with a total of 10 leaves, R2Score of 0.99.

   Fig 4.7 shows the ML results for 1GHz LNA and Fig 4.8 results for 25GHz LNA.

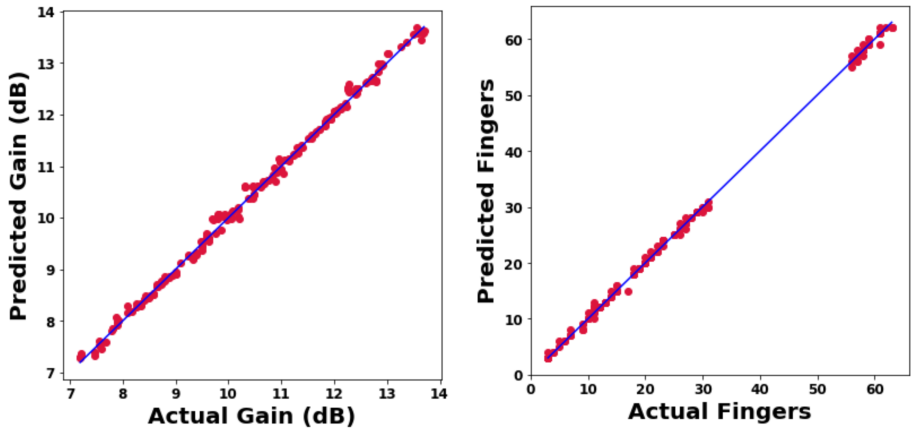


Figure 4.7: ML training output graphs of LNA working at 1GHz

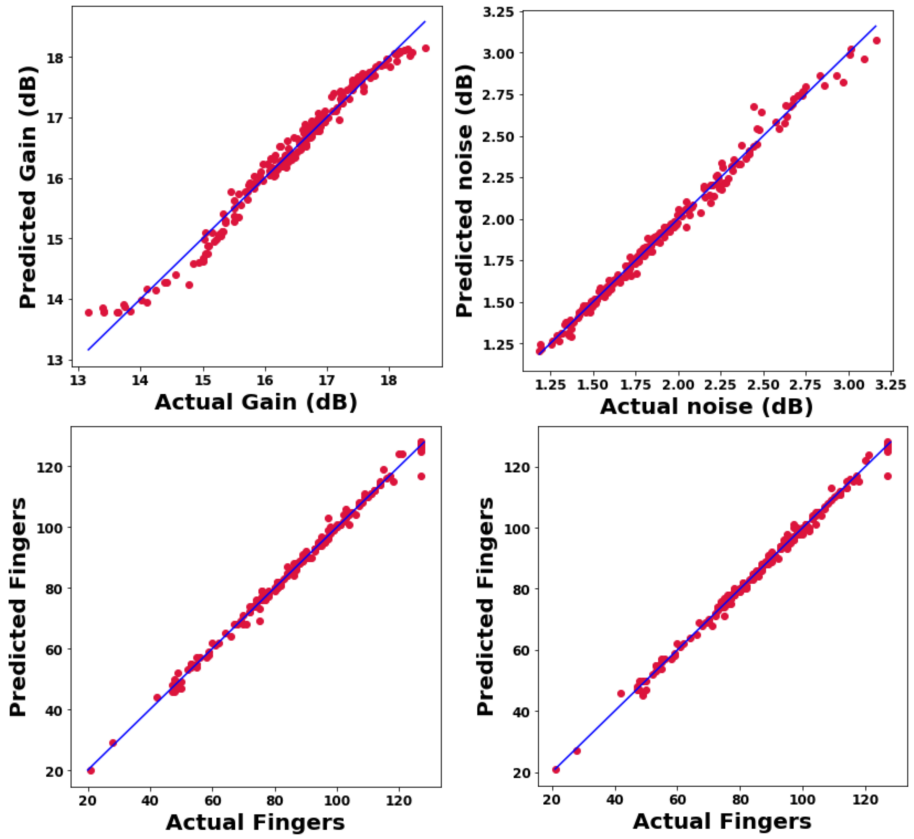
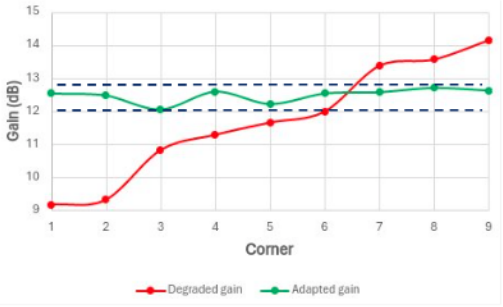


Figure 4.8: ML training output graphs of LNA working at 25GHz

4.4 Results and Discussion

For 1Ghz LNA the variation of gain from 10dB to 14dB has reduced to 12.43-23.65dB, making the variation less than 2%. The results are shown in Fig 4.9. For 25GHz LNA,



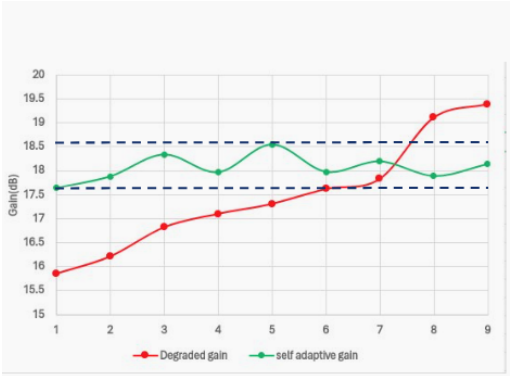
Corner	Conditions	Degraded gain	Adapted gain
1	FF, 1.1V, 100^{0}C	9.168	12.53
2	FF, 0.95V, 90^{0}C	9.31	12.47
3	TT, 1.1V, 120^{0}C	10.82	12.04
4	FF, 0.9V, -40^{0}C	11.28	12.59
5	SS, 1.1V, 120^{0}C	11.65	12.21
6	TT, 0.99V, 60^{0}C	11.98	12.53
7	SS, 0.97V, 35^{0}C	13.37	12.57
8	TT, 0.9V, -40^{0}C	13.56	12.7
9	SS, 0.9V, -40^{0}C	14.14	12.62

Figure 4.9: Resistive feedback LNA working at 1GHz gain results

the gain variation has been reduced to 17.48 - 18.97dB, while the NF has a range of 1.2-1.6 dB. These results have been achieved by maintaining an IIP3 of -20dB. The results of gain and NF are shown in Fig ‘4.10 and Fig 4.11. The loop for 25GHz is shown in Fig 4.10.

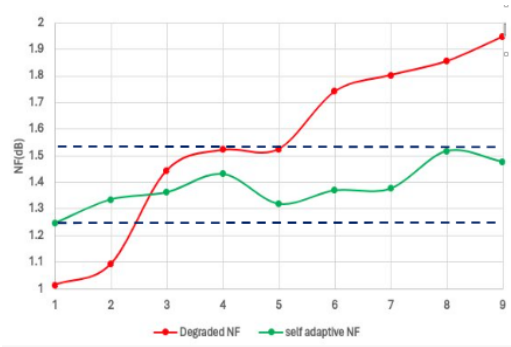
The self-adaptation loop is shown in Fig 4.12

The concept has been verified on a Tx- Driver, VCO, Mixer and transmitter driver whose results can be seen in Fig 4.13, 4.14, 4.15 respectively.



Corner	Conditions	Degraded gain	Adapted gain
1	SS, 810mV, -40^{0}C	15.84	17.63
2	TT, 810mV, 120^{0}C	16.2	17.87
3	SS, 860mV, 0^{0}C	16.81	18.33
4	FF, 810mV, 45^{0}C	17.09	17.96
5	SS, 930mV, 80^{0}C	17.3	18.54
6	FF, 870mV, 50^{0}C	17.61	17.97
7	FF, 990mV, 120^{0}C	17.82	18.19
8	TT, 970mV, -25^{0}C	19.1	17.88
9	TT, 990mV, -40^{0}C	19.38	18.13

Figure 4.10: LNA working at 25GHz Gain results



Corner	Conditions	Degraded NF	Adapted NF
1	TT, 990mV ,-40^{0}C	1.013	1.245
2	TT, 970mV, -25^{0}C	1.092	1.334
3	FF, 870mV, 50^{0}C	1.444	1.361
4	FF, 990mV, 120^{0}C	1.521	1.43
5	FF, 810mV, 45^{0}C	1.524	1.318
6	SS, 860mV, 0^{0}C	1.74	1.368
7	SS, 810mV, -40^{0}C	1.802	1.375
8	SS, 930mV, 80^{0}C	1.854	1.516
9	TT, 810mV, 120^{0}C	1.946	1.476

Figure 4.11: LNA working at 25GHz NF results

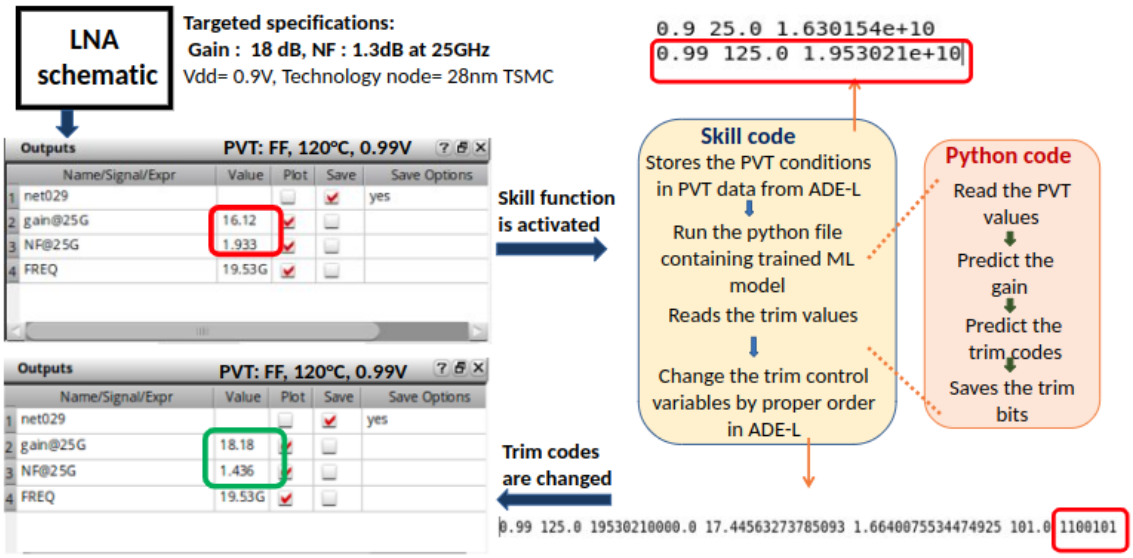
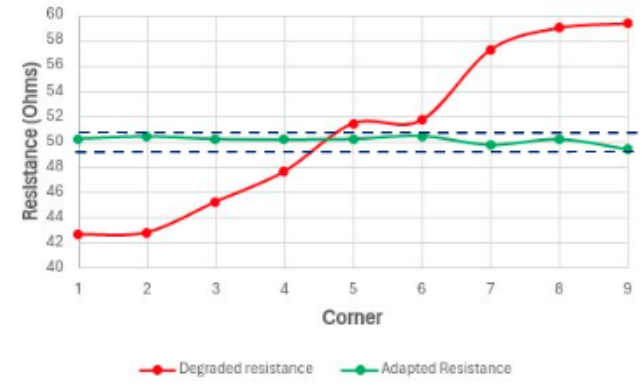


Figure 4.12: 25GHz LNA self adaptation loop

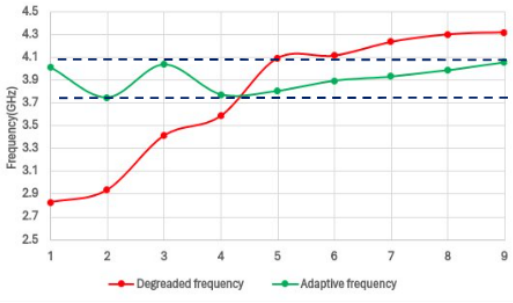


Corner	Conditions	Degraded Resistance	Adapted Resistance
1	FF, -40°C, 810mV	42.62	50.21
2	FF, 0°C, 890mV	42.78	50.38
3	FF, 120°C, 990mV	45.21	50.18
4	TT, -40°C, 990mV	47.61	50.14
5	TT, 100°C, 970mV	51.42	50.18
6	TT, 70°C, 870mV	51.67	50.42
7	SS, -40°C, 810mV	57.25	49.71
8	SS, 120°C, 990mV	58.98	50.16
9	SS, 60°C, 850mV	59.34	49.37

Figure 4.13: TX- driver results

4.5 Conclusion

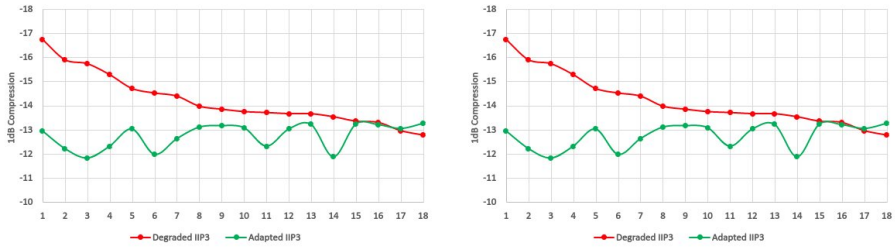
In conclusion, the implementation of self-adaptive techniques in the design of low-noise amplifiers (LNAs), voltage-controlled oscillators (VCOs), and transmitter circuits has demonstrated significant benefits in terms of performance, robustness, and adaptability. Through the utilization of self-adaptive algorithms, these circuits have exhibited the



Corner	Conditions	Degraded frequency	Adapted frequency
1	SS, -5°C, 940mV	2.825	4.009
2	SS, 10°C, 890mV	2.933	3.744
3	SS, 80°C, 870mV	3.409	4.033
4	SS, 125°C, 810mV	3.58	3.77
5	FF, -40°C, 810mV	4.088	3.801
6	TT, 125°C, 810mV	4.11	3.89
7	FF, -25°C, 850mV	4.23	3.927
8	FF, -40°C, 990mV	4.296	3.982
9	TT, 125°C, 930mV	4.316	4.052

Figure 4.14: VCO results

capability to dynamically adjust their operating parameters in response to changing environmental conditions, variations in process, voltage, and temperature (PVT), and other factors. The results from the two designs of LNAs, VCOs, and transmitter circuits showcase improved efficiency, enhanced linearity, and superior reliability across a range of operating conditions. Moreover, the self-adaptive approach has enabled these circuits to perform optimally in challenging environments, such as temperature extremes and varying input signals. Overall, the successful integration of self-adaptation techniques in the design of these circuits underscores their potential to revolutionize RF front-end design, paving the way for more resilient and adaptive wireless communication systems in the future.



Number	Condition	Degraded IIP3	Adapted Iip3
1	1.7V ,50^{0}C ,SS	-7.585	-4.268
2	1.78V , 40^{0}C, SS	-6.897	-3.099
3	1.82V ,100^{0}C,SS	-6.626	-3.228
4	1.84V , 60^{0}C, SS	-6.353	-3.093
5	1.9V ,110^{0}C, SS	-5.946	-3.213
6	1.76V ,-25^{0}C, FF	-5.027	-2.909
7	1.63V , 85^{0}C, TT	-4.965	-3.057
8	1.95V ,10^{0}C, FF	-4.449	-3.256
9	1.65V ,5^{0}C, TT	-4.407	-3.213

Number	Condition	Degraded IIP3	Adapted Iip3
10	1.84V ,35^{0}C, FF	-4.065	-3.096
11	1.77V , 40^{0}C, FF	-3.998	-3.315
12	1.74V, -35^{0}C, TT	-3.844	-3.317
13	1.7V, -10^{0}C, TT	-3.755	-3.11
14	1.81V , 60^{0}C, FF	-3.711	-3.199
15	1.75V , 95^{0}C, FF	-3.363	-3.335
16	1.88V, 120^{0}C, TT	-3.262	-3.267
17	1.8V, 20^{0}C, TT	-3.247	-3.136
18	1.94V, 105^{0}C, TT	-2.51	-3.211

Number	Condition	Degraded 1dB Compresion	Adapted 1dB Compresion
1	1.7V ,50^{0}C ,SS	-16.73	-12.95
2	1.78V , 40^{0}C, SS	-15.89	-12.22
3	1.82V ,100^{0}C,SS	-15.73	-11.83
4	1.84V , 60^{0}C, SS	-15.27	-12.32
5	1.9V ,110^{0}C, SS	-14.70	-13.03
6	1.76V ,-25^{0}C, FF	-14.51	-11.98
7	1.63V , 85^{0}C, TT	-14.39	-12.63
8	1.95V ,10^{0}C, FF	-13.97	-13.11
9	1.65V ,5^{0}C, TT	-13.85	-13.17

Number	Condition	Degraded 1dB Compresion	Adapted 1dB Compresion
10	1.84V ,35^{0}C, FF	-13.74	-13.09
11	1.77V , 40^{0}C, FF	-13.71	-12.32
12	1.74V, -35^{0}C, TT	-13.66	-13.03
13	1.7V, -10^{0}C, TT	-13.66	-13.22
14	1.81V , 60^{0}C, FF	-13.53	-11.88
15	1.75V , 95^{0}C, FF	-13.35	-13.24
16	1.88V, 120^{0}C, TT	-13.30	-13.21
17	1.8V, 20^{0}C, TT	-12.96	-13.05
18	1.94V, 105^{0}C, TT	-12.77	-13.26

Figure 4.15: Mixer results

Chapter 5

Conclusion & Future Work

In conclusion, the design and implementation of the circuits presented in this thesis represent significant advancements in low-power and adaptive analog and RF circuitry. The circuits and methodologies presented in this thesis represent significant advancements in analog and RF circuit design, offering innovative solutions to address the challenges of low-power operation, wide temperature ranges, and post-fabrication variations. These contributions could drive the development of energy-efficient and adaptive electronic systems, paving the way for future advancements in IoT, bioelectronics, and beyond.

Part 1 of the thesis focused on developing innovative voltage and current reference circuits tailored for ultra-low-power applications across varying temperature ranges. The circuits presented include a low-supply sensitive current/voltage reference without the use of amplifiers and resistors, a supply-insensitive gate-leakage-based voltage/current reference circuit, and a gate-leakage based sub-bandgap voltage reference explicitly designed for low-power IoT systems. These circuits offer remarkable performance characteristics, such as ultra-low power consumption, wide temperature operation, and high accuracy, making them well-suited for various energy-efficient electronic applications.

Part 1 of the thesis also introduced a high-frequency, cost-effective, on-chip CMOS Vector Network Analyzer (VNA) tailored for bio-molecule detection. This VNA represents a

significant contribution to bioelectronics, offering a powerful and efficient tool for analyzing susceptible and specific biological samples.

Part 2 of the thesis focused on developing machine learning-driven self-adaptive loops for analog and RF circuits to mitigate post-fabrication Process, Voltage, and Temperature (PVT) variations. These self-adaptive loops harness the power of machine learning algorithms to adjust circuit parameters and configurations in real-time, optimizing performance, power efficiency, and reliability across varying operating conditions. Furthermore, the thesis introduced a novel PVT sensor designed to interface with the self-adaptive loop, providing accurate and real-time feedback on environmental conditions to ensure robust and adaptive circuit operation.

Future work

The future work from the circuits and methodologies presented in this thesis holds great promise for advancing the state-of-the-art in analog and RF circuit design, fostering innovation, and addressing the evolving challenges and opportunities in diverse application domains. These potential directions include:

1. Optimization for Specific Applications: Further optimization of the presented circuits and methodologies tailored for specific application domains could be explored. For instance, in the case of ML-driven self-adaptive loops, fine-tuning the machine learning algorithms to accommodate the unique requirements of different analog and RF circuits or application scenarios could enhance performance and adaptability.

2. Integration into System-Level Designs: Investigating the integration of the developed circuits and methodologies into larger system-level designs is another promising avenue. This could involve incorporating low-power references and self-adaptive loops into integrated systems, such as IoT devices, wireless sensor networks, or biomedical implants, to demonstrate their performance in real-world applications.

3. Enhancement of Accuracy and Robustness: Further research could improve the presented circuits and methodologies' accuracy, robustness, and reliability. This could involve refining modelling techniques, implementing error-correction mechanisms, or exploring novel circuit topologies to enhance performance under varying operating conditions, environmental factors, and fabrication variations.

4. Exploration of Advanced Materials and Technologies: Investigating the application of advanced materials and emerging semiconductor technologies could unlock new possibilities for enhancing circuit performance and energy efficiency. For instance, exploring novel materials with unique electrical properties or leveraging advancements in nanotechnology and quantum computing could lead to developing next-generation analog and RF circuits with unprecedented capabilities.

5. Validation through Prototyping and Experimentation: Conducting prototyping and experimental validation of the presented circuits and methodologies in real-world environments is essential to assess their practical feasibility and performance. This could involve fabricating prototype circuits, conducting comprehensive characterization experiments, and benchmarking against existing state-of-the-art solutions to validate their effectiveness and potential for commercialization.

6. Exploration of Novel Applications: Lastly, exploring novel application areas and use cases for the developed circuits and methodologies could open up new avenues for research and innovation. This could involve investigating their applicability in emerging fields such as quantum computing, neuromorphic computing, or sustainable energy systems, where energy efficiency, adaptability, and reliability are paramount.

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