A 443pW Accumulation-Mode Gate-Leakage Based Bandgap Reference for IoT Applications

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A 443pW Accumulation-Mode Gate-Leakage Based Bandgap Reference for IoT Applications

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***Abstract*—The paper presents a sub-nW bandgap reference (BGR) that exploits the temperature variation of gate-leakage current in thin oxide devices operating in the accumulation region to generate the reference voltage. The incorporation of gate-leakage transistors scales down the power consumption of the BGR to pico-watt level without using any large physical resistors or sophisticated techniques, thereby making it suitable for IoT applications. The BGR is designed in TSMC 65nm technology and occupies an area of $0.009mm^2$. Post layout simulation results show nominal and worst-case accuracies of $23ppm/^oC$ and $44ppm/^oC$ respectively in the temperature range of -40^oC to 100^oC. Without any trimming, an inaccuracy ($\pm 3\sigma$) of 3% is observed for the reference voltage, showing its resilience to process variations. It also exhibits a typical line sensitivity of 0.063%/V in a supply range of 1.5V-3.8V and a PSRR of -65dB at DC and 1.8V supply. The power consumption is observed to be 443pW at 1.5V supply and nominal temperature.**

I. Introduction

The gaining popularity and rapid development of the Internet-of-Things (IoT) has spawned several applications such as environmental, biomedical, military, smart homes, etc. The systems designed for these applications are often powered by miniaturized batteries, which have limited energy storage volume. This limitation in the energy budget renders the power consumption of the system a critical factor in deciding the system's lifetime. Duty-cycling is a widely adopted strategy to reduce the average power of the system, thereby effectively managing the energy provided by the battery. However, the system mostly stays in sleep mode and hence the overall power consumption is limited by the blocks which contribute to the sleep-mode power consumption. Voltage references are among such blocks which are typically always turned on and contribute to the standby power consumption. Hence, it becomes imperative for the voltage references to comply with the stringent power constraints, thus providing a motivation to design pico-watt voltage references. Since bandgap references are the most reliable voltage references due to their robustness to process, supply and temperature, it is worthwhile to design bandgap references for the sub-nW regime.

Conventional bandgap references have micro-watt power consumption [1]–[4], which precludes their use in low-power IoT applications. To alleviate this issue, bandgap references whose static power consumption is in the order of nano-watts [5]–[8], have been proposed in the state-of-the-art. However, their power consumption is still high for the targeted applications. Moreover, large physical resistors are used in [6]–[8] to scale down the power consumption to nano-watt level, thereby increasing the silicon area. [9] proposes a sub-10nW BGR but again incorporates large resistors. [10] proposes a dynamic BGR by adopting a sample-and-hold method for reducing the overall power consumption to 2.98nW. However, it uses large sampling capacitors in addition to large resistors, thereby increasing the area drastically. The driving force to reduce the power consumption further has resulted in the design of pico-watt bandgap reference voltage ($\sim$1.2V) generators [11], [12]. They, however use native oxide devices (NVT transistors) to generate the reference voltage, which are not provided by many foundries. Moreover, [12] has significant process spread and requires trimming, thereby increasing the cost.

This paper proposes a bandgap reference which consumes sub-nW power without using large physical resistors, native oxide devices or any other sophisticated techniques which increase either area or power. It rather incorporates thin oxide devices which are made to operate in accumulation region and the accumulation-mode gate-leakage current characteristics are used in generating the reference voltage. Rest of the paper is organized as follows. Section II deals with the design of the proposed bandgap reference by deriving a simplified expression for the accumulation-mode gate-leakage current. Section III shows the results for the designed reference and finally section IV concludes the paper.

II. Design and Analysis of the Proposed Bandgap Reference

Fig.1 depicts the architecture of the proposed bandgap reference. Transistors M1-M6 and M7-M10 are regular thick oxide PMOS and NMOS devices respectively while M11-M15 are thin oxide PMOS transistors. Due to the extremely small oxide thickness, tunnelling currents of the order of fA to pA flow through the gate of these transistors [13]. They are made to operate in the accumulation region, in which the simplified expression for the gate-leakage current can be derived as shown in the following sub-section. Q1, Q2 and Q3 are vertical PNP transistors or parasitic BJTs. A capacitor implemented using NMOS thick oxide transistor M16, is used at the output of the voltage reference to suppress the supply noise at higher frequencies. A start-up circuit [14] has been used to avoid any degenerate bias conditions in the circuit.

A. Derivation for accumulation-mode gate-leakage current

The simplified expression for accumulation-mode gate-leakage current can be deduced by using the gate-tunnelling current model for the thin-oxide devices given in [15]. The gate tunnelling current consists of four components, namely, gate-to-substrate current (I_{gb}), gate-to-channel current (I_{gc}) and gate-to-source/drain currents (I_{gs} and I_{gd}). Of these components, I_{gb} can be ignored in bulk technologies, as it is negligible compared to the total gate-leakage current [16],

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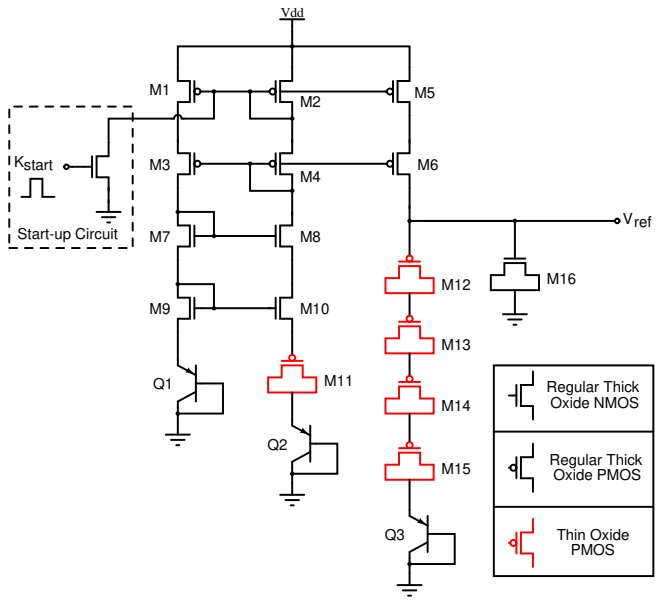

Fig. 1. Proposed Bandgap Reference

[17]. The component I_{gc} can also be neglected as it is a function of $V_{sg} - |V_{th}|$ (for PMOS), whose negative value (since the transistor is in accumulation region) forces its magnitude to be several orders less than that of the overall gate-leakage current. Owing to the symmetric connections of the source and drain of the transistor to its bulk, the components I_{gs} and I_{gd} will be equal to each other. Hence, the total gate-leakage current I_{tot} can be given as twice the gate-to-source/drain current (I_{gs}/I_{gd}) [15] :

$$I_{tot} = k_1.V_{sg}.V'_{sg}.exp[-k_2.(AIGSD - BIGSD.V'_{sg}).(1 + CIGSD.V'_{sg})] \quad (1)$$

where k_1 = 2*$W_{eff}.(DLCIG).A.T_{oxRatioEdge}$ and k_2 = $B.(TOXE).(POXEDGE)$. Here, W_{eff} is the effective width of the transistor and DLCIG, A, $T_{oxRatioEdge}$, B, TOXE, and POXEDGE are modelling constants for a given technology which are independent of temperature. The expression for the term V'_{sg} in the eq.1 is given by :

$$V'_{sg} = \sqrt{(V_{sg} - V_{fbsd})^2 + 0.0001} \quad (2)$$

where V_{fbsd} is the flat-band voltage between gate and S/D diffusions calculated by the below expression :

$$V_{fbsd} = \frac{k_B T}{q} log\left(\frac{NGATE}{NSD}\right) + VFBSDOFF \quad (3)$$

Again, NGATE, NSD and VFBSDOFF are modelling constants. The values of NGATE, NSD and VFBSDOFF in the designed technology node are observed to be 181.2E, 100E and 0 respectively. Substituting their values in eq.3, the value of V_{fbsd} turns out to be 6.67mV at room temperature. Considering the least $|V_{sg}|$ across M11-M15 to be 40mV, V_{fbsd} cannot be neglected in comparison with $|V_{sg}|$. However, the term 0.0001 can be neglected under these conditions for which $V_{sg'}$ becomes equal to $V_{sg} - V_{fbsd}$. The values of AIGSD, BIGSD and CIGSD are observed to be 4.96m, 0.207m and 4.264m respectively. From these values, it can be deduced that $AIGSD >> BIGSD.V_{sg'}$ and $CIGSD.V_{sg'} << 1$, considering the maximum value of $|V_{sg}|$ across M11-M15 to be 350mV. Hence, the terms $BIGSD.V_{sg'}$ and $CIGSD.V_{sg'}$ can be neglected as they contribute to a maximum error of 6% in I_{tot}. Equation 1 can be finally approximated as :

$$I_{tot} = KV_{sg}(V_{sg} - V_{fbsd}) \quad (4)$$

where K = $k_1.exp(-k_2.AIGSD)$. To validate this approximated equation, we plot the error between the simulated gate-leakage current and the estimated current from eq.4 w.r.t magnitude of V_{sg} in different process corners (shown in Fig.2). It can be observed that the maximum error is 6% w.r.t variation in V_{sg} across all process corners.

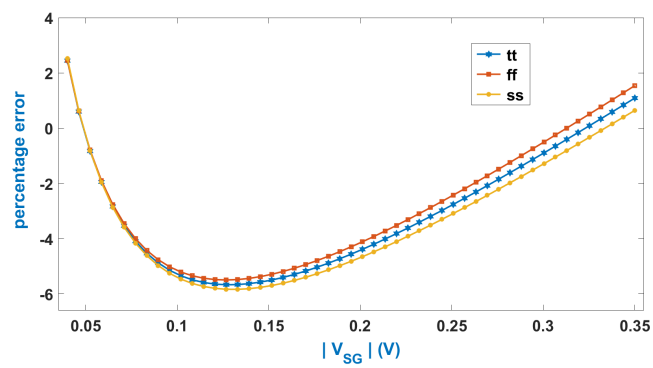

Fig. 2. % error between simulated and estimated results vs $|V_{sg}|$

B. Temperature Compensation

From Fig.1, V_{sg} across M11 is equal to $V_{EB2} - V_{EB1}$. Considering the I-V characteristics of a BJT, V_{sg} across M11 can be further simplified as $V_T \ln\left(\frac{I}{I_{S2}}\right) - V_T \ln\left(\frac{I}{I_{S1}}\right)$. Here, transistor Q2 consists 'n' parallel units of Q1, which implies $I_{S2} = nI_{S1}$. So the V_{sg} across M11 can be written as $V_T \ln\left(\frac{1}{n}\right)$ and from eq.4, current in M11 is given by :

$$I_{tot} = K_1 V_T ln(n)(V_T ln(n) + V_{fbsd}) \quad (5)$$

where K_1 is a function of effective width W_{eff} of M11. Current in the circuit can also be given by the gate-leakage current flowing through transistors M12-M15 (same current through all the branches). Note that M12-M15 have same widths and lengths but not equal to those of M11. The expression for gate-leakage current in M12-M15 is given by :

$$I_{tot} = K_2\left(\frac{V_{ref} - V_{EB3}}{4}\right)\left(\frac{V_{ref} - V_{EB3}}{4} + V_{fbsd}\right) \quad (6)$$

where K_2 is a function of effective widths W_{eff} of M12-M15. Since V_{ref} is a higher voltage of value $\sim$ 1.2V, V_{fbsd} in eq.6 can be neglected in comparison to the term $(V_{ref} - V_{EB3})/4$. Note that instead of using four transistors (M12-M15), a single transistor can be used. However, the width of that transistor should be kept very low, which will cause large effect on the output voltage due to mismatch of transistors. In some technology nodes, it is also not possible to decrease

the width beyond a certain extent. Hence, considering the area and mismatch trade-off, four transistors have been used. From eq.5 and eq.6, the final expression for V_{ref} can be given by :

$$V_{ref} = V_{EB3} + 4K_3V_T \tag{7}$$

where K_3 is a temperature independent constant given by :

$$K_3 = \sqrt{\left(\frac{K_1(ln(n))^2 + K_1 ln(n) log\left(\frac{NGATE}{NSD}\right)}{K_2}\right)} \tag{8}$$

The derivative $\left(\frac{\partial V_{ref}}{\partial T}\right)$ should be equated to zero for getting temperature invariancy. Using the expression for $\left(\frac{\partial V_{EB}}{\partial T}\right)$ (for Q3) from [18], the expression for $\left(\frac{\partial V_{ref}}{\partial T}\right)$ can be given by :

$$\frac{\partial V_{ref}}{\partial T} = \frac{V_{EB3} - (4 + m_{Q3}V_T - \frac{E_g}{q})}{T} + 4K_3\left(\frac{k_B}{q}\right) \tag{9}$$

From eq.9, it can be observed that by properly sizing the transistors M11-M15, a temperature compensated voltage reference can be obtained. Transistor M11 is sized such that the current in each of the branches is ∼100pA. M12-M15 are then sized according to eq.9.

III. Results and Discussion

The proposed bandgap reference is implemented in TSMC 65nm technology and various post-layout and Monte-Carlo simulation results are shown in this section. Fig.3 shows the variation of the bandgap reference voltage w.r.t temperature in extreme process corners. The observed TCs of the bandgap reference in these corners are $23ppm/^oC$, $41ppm/^oC$ and $31ppm/^oC$ in all TT, all SS and all FF corners respectively. For statistical validation of the bandgap reference, Monte-Carlo simulations are run (1000 runs for both process and mismatch) for the reference voltage and the temperature coefficient (TC) of the BGR. The results for these are shown in Fig.4 and Fig.5 respectively. Although the simulation is run for 1000 samples, Fig.4 shows the variation of the reference value w.r.t temperature for 50 samples (including the worst case corners) for the sake of clarity. The maximum inaccuracy ($\pm 3\sigma$) considering temperature, process and mismatch variations is observed to be 3%. Fig.5 shows the Monte-Carlo simulation result for TC of the bandgap reference. The mean and standard deviation in the TC are observed to be $23ppm/^oC$ and $6.745ppm/^oC$ respectively, with the maximum TC being $44ppm/^oC$. From the results of Fig.4 and Fig.5, it can be concluded that the bandgap reference is process-invariant and one-point calibration can be used for applications where the variations need to be further reduced. Fig.6 shows the PSRR of the bandgap reference in different process corners. The observed PSRRs at DC are -65dB, -64dB and -66dB in all TT, all SS and all FF corners respectively. At higher frequencies, the PSRR is observed to be around -35dB. The supply rejection at higher frequencies can be improved further by simply increasing the width and length of the MOS capacitor M16 at the cost of increase in area. Fig.7 shows the line-sensitivity of the bandgap reference in different process corners. In a wide supply range of 1.5V - 3.8V, the line sensitivities are observed to be 0.063%/V, 0.12%/V and 0.48%/V in all TT, all SS and all FF corners respectively. The variation in the total current is observed to increase by only 2.338x times w.r.t temperature in the temperature range of -40^oC to 100^oC. On the other hand, it increases by only 1.006x times w.r.t supply voltage when the latter varies from 1.5V - 3.8V. For the start-up circuit used, the observed settling times for 90% and 95% of the steady state value are 45ms and 78ms respectively. Although the start-up time appears to be high, it is quite comparable to the start-up times of state-of-the-art pico-watt self-biased blocks [19]. Fig.8 shows the layout of the proposed bandgap reference from which the area is calculated to be $0.009mm^2$. Finally, Table I in Fig.9 compares various specifications of the proposed bandgap reference with the state-of-art bandgap references.

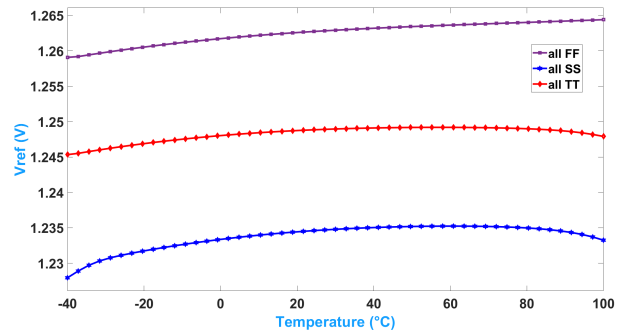

Fig. 3. Proposed bandgap reference in different corners

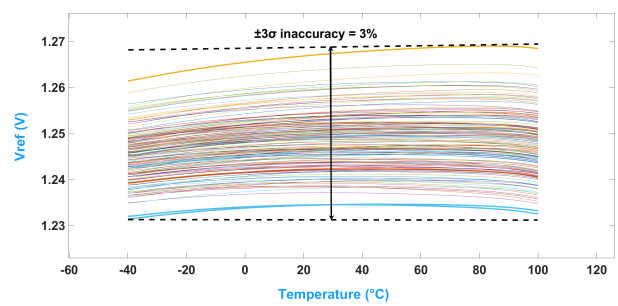

Fig. 4. Monte-Carlo simulation result for the BGR value w.r.t temperature

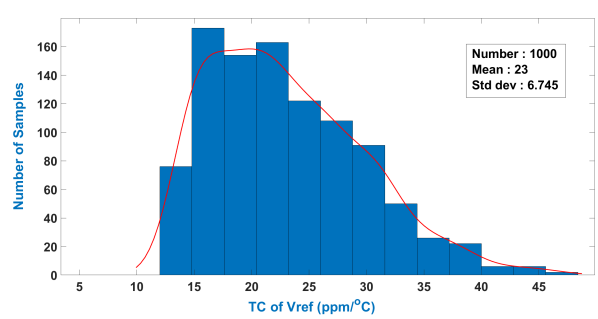

Fig. 5. Monte-Carlo simulation result for the TC of BGR

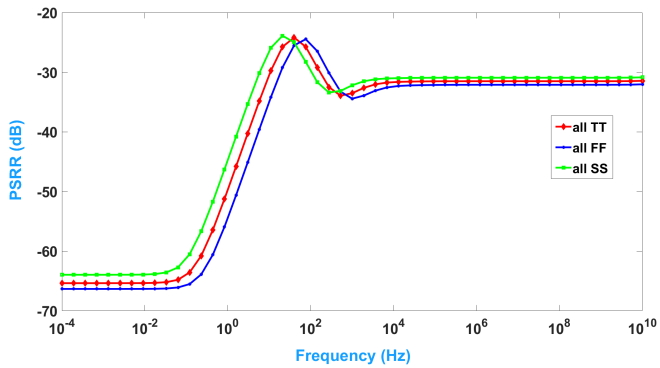

Fig. 6. PSRR of the BGR at different process corners

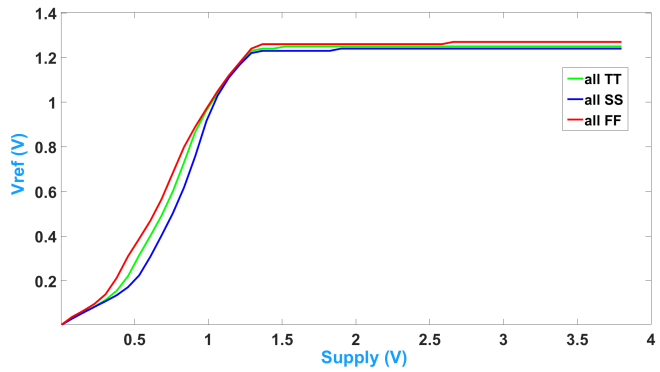

Fig. 7. Line sensitivity of the BGR in different process corners

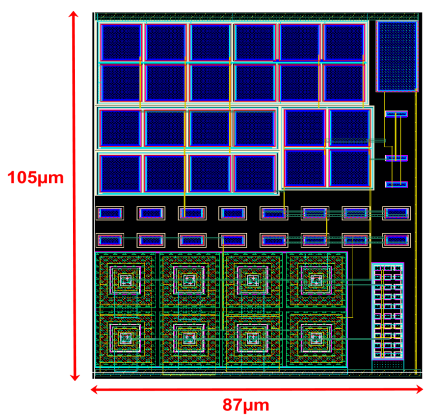

Fig. 8. Layout of the BGR

IV. Conclusion

A sub-nW bandgap reference is proposed that uses thin oxide PMOS transistors instead of large resistors, to save area while scaling down the power consumption. These thin-oxide PMOS transistors are operated in accumulation region and a rigorous mathematical analysis is performed to get a simplified expression for accumulation mode gate-leakage current. The temperature variation of this current is exploited in the generating the reference voltage, which is robust to process variations showing an untrimmed inaccuracy ($\pm 3\sigma$) of 3%. It also achieves a good line sensitivity of 0.063%/V in a supply range of 1.5V-3.8V, without using any native oxide transistors, which are not available in many foundries.

Specifications	This Work	[1]	[7]	[10]	[11]	[12]
Technology	**65nm**	160nm	180nm	180nm	180nm	180nm
Type	**BJT**	BJT	BJT	BJT	CMOS	CMOS
Res/Cap/NVT Devices	**Not Used**	Used	Used	Used	Used	Used
Vref (V)	**1.245**	1.0875	1.2	1.19	1.25	1.17
Temp Range (°C)	**-40 to 100**	-40 to 125	-45 to 125	-20 to 100	0 to 100	0 to 170
TC (ppm/°C)	**23 (MC run)**	5 – 12 (measured)	32.7	24.74	8 – 53	32 – 106
3σ Inaccuracy (@ 27°C)	**1.5%**	±0.75%	0.63%	0.432%	2.4%	1.7%
Calibration	**No**	No	1 - point	1 - point	No	1 - point
Supply Range	**1.5V – 3.8V**	1.8±10%	2V – 5V	NA	1.4V – 3.6V	1.8V – 3.6V
Line Sensitivity (%/V)	**0.063**	NA	0.058	0.062	0.31	0.09
PSRR	**-65dB @ DC**	-74dB @ DC	-85dB @100Hz	-67dB @ 100Hz	-41dB @ 100Hz	-38dB @ 100Hz
Power Consumption	**443pW @ 1.5V**	99uW @ 1.8 V	192nW @ 2V	2.98nW	33.6pW @ 1.6V	136.8pW @1.8V
Area (mm^2)	**0.009**	0.12	0.063	0.98	0.0025	0.0081

Fig. 9. Table 1 : Comparison With State-of-the-Art Architectures

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