67ppm/■C, 66nA PVT Invariant CurvatureCompensated Current Reference for Ultra-LowPower Applications

by

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***Abstract*—This work presents a highly accurate current reference of 66nA for ultra-low power applications. A very low figure-of-merit (FOM) of 1.3501ppm/°C^2 is achieved on consuming a minimal quiescent current of 199.37nA. To cancel out process variations, the current subtraction technique is employed and a β-multiplier is used to compensate for mobility (μ) and threshold voltage (V_{th}). In addition, curvature compensation technique backed by PTAT and CTAT current cancellation is adopted to attain a lower temperature coefficient (TC). Hence, an imperceptible variation of accuracy with temperature and supply variations across all process corners is attained. An adopted trimming scheme further minimizes the overall process spread to $\pm$1.515% without compromising on accuracy. Accordingly, a TC of 67.04ppm/°C over a wide temperature range of -50°C to 100°C is obtained. Furthermore, 1.413%/V line sensitivity (LS) in the supply range of 1.38V to 3V is observed. Low power consumption of 275.13nW@1.38V facilitates its use in high-performance low power applications.**

***Index Terms*—FOM, curvature compensation, Line Sensitivity, Proportional to Absolute Temperature (PTAT), Complementary to Absolute Temperature (CTAT), ZTC**

I. Introduction

Thriving demand for energy harvesters [1], biomedical devices like Cochlear implants [2], gastric electrical stimulator [3], etc. led to a greater requirement for circuits engrossing less quiescent current. To support these applications there is a necessity to design ultra-low power analog and mixed-signal modules like Op-Amps, Oscillators, ADC's, DAC's, etc. Current reference is one of the critical blocks involved in these above mentioned modules. Designing high accurate (PVT invariant) current reference (nA range) with low power consumption in scaled CMOS technologies has been a major challenge for analog designers.

In the literature survey, distinct techniques have been proposed [4]–[11] to enhance the performance across PVT variations. Ueno *et al.* [5] has reduced the active area ($0.015mm^2$) to a great extent by biasing MOSFET as a resistor in $\beta-$multiplier. But the power consumption (1μW) and TC (520ppm/°C) of the generated 96nA @ 1.8V reference is high. Hirose *et al.* [6] used the technique of current subtraction where power consumption (88.53nW) is remarkably low with an outstanding supply regulation (0.046%/V). But the achieved TC (1190ppm/°C) in -20°C to 80°C range is considerably high. Bendali *et al.* [7] used the concept of biasing the MOSFET at ZTC to generate 144.3μA. With a low supply voltage (1V), a TC of 185ppm/°C in the limited temperature range (0-100°C) is achieved. Osipov *et al.* [8] used the first-order temperature compensation technique to generate 1.05μA. A satisfactory TC of 143ppm/°C is attained but the minimum voltage of 2.2V is required. Lee *et al.* [9] and Jain *et al.* [10] used the concept of dividing PTAT voltage with resistor of PTAT temperature dependency to boost the accuracy but these designs involved op-amp as an integral part. Mohamed *et al.* [11] proposed a current reference based on curvature compensation scheme which minimized the TC to 40ppm/°C. But the power consumed is 820.8nW and the supply range (1.2V to 2V) is limited.

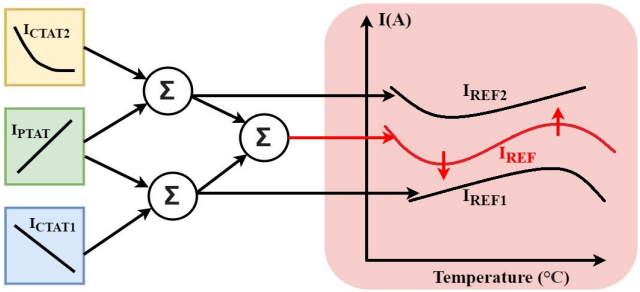

Fig. 1. Block diagram of the proposed architecture

In the light of this background, a curvature compensated current reference for wide temperature and supply range is proposed. As shown in Fig. 1, PTAT current is added to the CTAT current resulting in I_{REF1}. Similarly, a non-linear CTAT current is added to PTAT current resulting in I_{REF2}. Finally, I_{REF1} and I_{REF2} are summed up to get curvature compensated current reference (I_{REF} as shown in Fig. 1). This brief is organized as follows. Section II explains the proposed architecture, Section III summarizes the obtained results and Section IV draws the conclusions.

II. Proposed Architecture

The proposed architecture has three considerable segments as shown in Fig. 2.

A. PTAT current generator (I_{PTAT})

To generate PTAT current, a β-multiplier circuit is used as shown in Fig. 2 (I_{PTAT}-GENERATOR). Current through the

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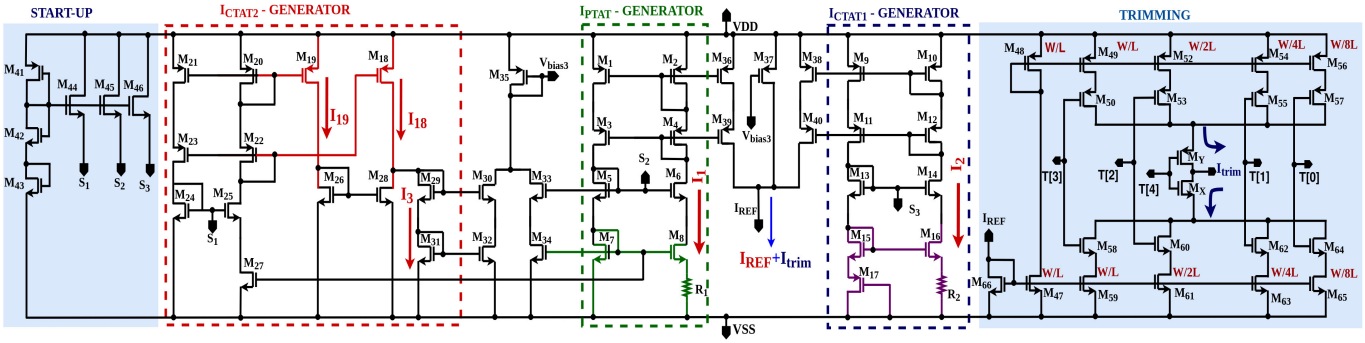

Fig. 2. Circuit diagram of the proposed Current Reference

poly resistor R1 is given by:

$$\frac{V_{GS_7} - V_{GS_8}}{R_1} = I_1 \tag{1}$$

Current through the MOSFET in sub-threshold region for V_{DS}>0.1V [5], [12] is given by:

$$I_D = \mu C_{ox} \frac{W}{L} (\eta - 1) V_T^2 exp(\frac{V_{GS} - V_{th}}{\eta V_T}) \tag{2}$$

where μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, η is the sub-threshold slope factor, $V_T = \frac{K_B T}{q}$ is the thermal voltage, K_B is the Boltzmann constant, q is the elementary charge, T is the temperature and V_{th} is the threshold voltage of a MOSFET.

Hence from (1) and (2), current I_1 is given as:

$$I_1 = \frac{\eta V_T ln \frac{K_8}{K_7}}{R_1} + \frac{\delta V_{th}}{R_1} \tag{3}$$

where δV_{th} = V_{th_7} - V_{th_8}, K_7 and K_8 are the sizes of M_7 and M_8 respectively. In (3), the second term (δV_{th}/R_1) is negligible in comparison with first term. Hence,

$$I_1 = \frac{\eta V_T ln \frac{K_8}{K_7}}{R_1} \tag{4}$$

(4) illustrates that I_1 is independent of process parameters (μ, V_{th}) and supply voltage. The poly resistance can be modelled as $R_1 = R_0(1 + \alpha \cdot T)$ [13], [9] where, α is a process independent temperature coefficient. Differentiating (4) with respect to temperature results in:

$$\frac{1}{I_1} \frac{\partial I_1}{\partial T} = TC_{I1} = \frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R_1} \frac{\partial R_1}{\partial T} \tag{5}$$

(4) and (5) concludes that the current I_1 can be adjusted to have PTAT behaviour (as shown in Fig. 3) by appropriate sizing of M_7 and M_8. Hence, I_1 = I_{PTAT}.

B. CTAT current generator-1 (I_{CTAT1})

To generate CTAT current, the circuit shown in Fig. 2 (I_{CTAT1}-GENERATOR) is proposed. MOSFET's M_9 - M_{16} forms the Widlar current source which contributes for supply independence. M_{17} is a diode connected MOSFET whose V_{SG} appears across R_2 (as $V_{GS_{15}} \approx V_{GS_{16}}$). Therefore,

$$I_2 = \frac{V_{SG_{17}}}{R_2} \tag{6}$$

The CTAT behaviour of V_{SG} in a diode connected MOSFET is well explained in [14]. It is modelled as $V_{SG} = V_{SG_o} - \kappa_{V_{SG}} T$ where, V_{SG_o} is the V_{SG} at 0K and $\kappa_{V_{SG}}$ is the temperature coefficient of V_{SG}. Differentiating (6) with respect to temperature results in:

$$\frac{1}{I_2} \frac{\partial I_2}{\partial T} = \frac{1}{V_{SG_{17}}} \frac{\partial V_{SG_{17}}}{\partial T} - \frac{1}{R_2} \frac{\partial R_2}{\partial T} \tag{7}$$

$$TC_{I_2} = TC_{V_{SG_{17}}} + (-1 \cdot TC_{R_2}) \tag{8}$$

From (8), it is evident that generated current exhibits negative temperature coefficient (Fig. 3a). Hence, I_2 = I_{CTAT1}.

C. CTAT current generator-2 (I_{CTAT2})

To achieve the curvature compensation as shown in Fig. 1, another CTAT current with non-linear temperature dependency is generated. MOSFET's M_{21} - M_{25} (Fig. 2) forming a β-multiplier contributes for supply independence. M_{27} is biased with a supply independent node voltage V_{GS7} ($\leq V_{th27}$) to ensure its operation in sub-threshold region. Besides, M_{18} and M_{19} are biased with $V_{GS_{20}}$ + $V_{GS_{22}}$ and $V_{GS_{20}}$ respectively such that $I_{18} > I_{19}$. Hence, these MOSFET's (M_{18} and M_{19}) perform a critical role in current subtraction thereby eliminating process variations whose mathematical analysis is presented below. Subtracted current I_3 = I_{18} - I_{19} is given by,

$$I_3 = \beta(K_{18} \exp \frac{V_{GS_{18}} - V_{th_{18}}}{\eta V_T} - K_{19} \exp \frac{V_{GS_{19}} - V_{th_{19}}}{\eta V_T}) \tag{9}$$

where, β = μC_{ox}, K_{19} and K_{18} are the sizes of M_{19} and M_{18} respectively. Temperature dependency of mobility as given in [5] shows that $\mu \propto T^{-m}$ where, m is mobility temperature exponent. Hence, the current $I_3 \propto \beta$ has non-linear negative temperature dependency ($\therefore$ I_3 = I_{CTAT2}). To validate the process independency, (9) is differentiated with respect to process and resultant is equated to zero [15].

$$\frac{\partial I_3}{\partial P} = 0 \tag{10}$$

On simplification, the resultant can be approximated as,

$$\frac{K_{19}}{K_{18}} = \exp(\frac{V_{GS_{18}} - V_{GS_{19}}}{\eta V_T}) \tag{11}$$

Therefore, M_{19} and M_{18} are biased such that $V_{GS_{18}}$ - $V_{GS_{19}}$ = $0.5\eta V_T$ and their sizes are chosen accordingly (K_a = $1.68K_b$) thereby resulting in cancellation of process variation. Moreover, any supply variations across M_{18} and M_{19} are eliminated due to current subtraction.

Table I : PERFORMANCE SUMMARY AND COMPARISONS WITH RELATED WORKS

PARAMETERS	THIS WORK	[11]	[16]	[17]	[6]	[5]	[8]
Technology (μm)	**0.18**	0.18	0.18	0.35	0.35	0.35	0.35
Supply Range (V)	**1.38 - 3**	1.2 - 2	1.2 - 1.8	1.9 - 3.6	1.3 - 3	1.8 - 3	1.2 - 3.6
I_{REF} (nA)	**66**	142.5	92.3	16000	9.95	96	1050
TC(ppm/°C)	**67.04**	40	179.9	105	1190	520	143
Temperature Range(°C)	**-50 - 100**	-40 - 85	-40 - 85	0 - 110	-20 - 80	0 - 80	-40 - 120
Line Sensitivity (%/V)	**1.413**	1.45	7.5	4	0.046	0.2	2.73
I_{total} / I_{REF}	**3.0209**	4.8	4	2	6.844	3.47	1.9523
FOM($ppm/°C^2$)	**1.3501**	1.54	6.59	1.9	81.44	22.56	N/A
Area(mm^2)	**0.098**	0.02	0.007	0.065	N/A	0.012	0.057
Power(nW)	**275.13**	820	670	60800	88	1000	4510
Trimming	**Yes**	No	No	Yes	No	No	No

D. Temperature compensation

Two current references I_{REF1} (= I_{PTAT} + I_{CTAT1}) and I_{REF2} (= k.I_{PTAT} + I_{CTAT2}) with opposite curvatures are generated as shown in Fig. 3a and 3b which are in turn summed up proportionately to get curvature compensated current reference. From (4) and (6), I_{REF1} can be written as:

$$I_{REF1} = \frac{1}{R_1}\eta V_T \ln\frac{K_8}{K_7} + \frac{V_{GS_{17}}}{R_2} \tag{12}$$

In (12), the sizes of M_7 and M_8 are adjusted accordingly thereby resulting in I_{REF1} with the curvature as shown in Fig. 3a. From (4) and (9), I_{REF2} can be written as:

$$I_{REF2} = \frac{k}{R_1}\eta V_T \ln\frac{K_8}{K_7} + \beta(K_{18}exp\frac{V_{GS_{18}} - V_{th_{18}}}{\eta V_T} - K_{19}exp\frac{V_{GS_{19}} - V_{th_{19}}}{\eta V_T}) \tag{13}$$

Hence, I_{REF2} with the curvature as shown in Fig. 3b is obtained by appropriate sizing of M_7, M_8, M_{18} and M_{19}. Finally, α_1.I_{REF1} and α_2.I_{REF2} are added up to result in curvature compensated I_{REF} (Fig. 4) where k, α_1 and α_2 are scaling factors.

In order to avoid the zero current operating condition of self-biased circuits, a start-up circuit shown in Fig. 2 is employed [18]. Though the slope of I_{REF} is unvaried due to the introduced compensation, the amplitude of I_{REF} still varies in different process corners as shown in Fig. 6a. Hence, a trimming circuit is additionally employed (Fig. 2) to reduce this process spread.

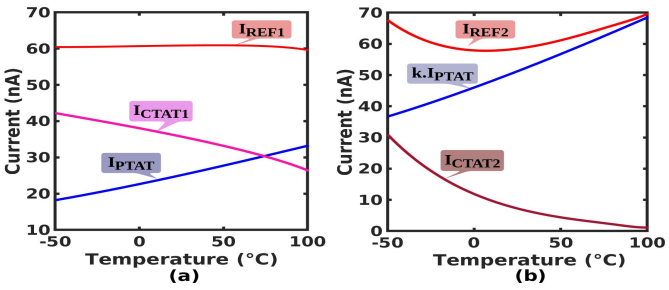

Fig. 3. Temperature Sensitivity of
(a) I_{REF1} = I_{PTAT}+I_{CTAT1} (b) I_{REF2} = k.I_{PTAT}+I_{CTAT2}

III. Results and Discussion

The proposed circuit has been implemented in TSMC 180nm technology. The temperature sensitivity (over the range of -50°C to 100°C at 1.38V supply) and LS (over the range of 1.38V to 3V at 27°C) of I_{REF} in TT corner are plotted as shown in Fig. 4 and 5 respectively. Hence, a TC of 67.04 ppm/°C and LS of 1.413%/V is noted. Furthermore, the TC and LS of I_{REF} is monitored across all possible skewed corners (Fig. 6a and 6b). An average TC and LS of 66ppm/°C and 1.52%/V is observed respectively.

A 5-bit trimming circuit [19] is employed to minimize the process spread. The value of I_{REF} with all possible trim codes is plotted in different process corners as shown on Fig. 7. From this, we can infer that the trim codes for I_{REF} = 66nA are 01010, 11001, 00000 and 10011 in SS, FS, SF and FF respectively. The trimming circuit is inactive for trim codes 01111 and 10000 (Fig. 2). The temperature sensitivity of I_{REF} in TT, SS, FF, SF and FS after trimming is plotted as shown in Fig. 8.

To test the robustness of the design with PVT variations, monte-carlo simulation on I_{REF} at 27°C and TC at a supply of 1.38V is done for 1000 samples (Fig. 9a and 9b). The mean (μ) of 66.25nA and 65.92ppm/°C and a standard deviation (σ) of 2.65nA and 11.3ppm/°C are obtained for I_{REF} and TC respectively. Also, FOM is examined for the total assessment of proposed design in terms of TC, temperature range, I_{REF} and I_q [11].

$$FOM(\frac{ppm}{°C^2}) = \frac{TC(ppm/°C)}{Temp.Range(°C)} \cdot \frac{I_q(nA)}{I_{REF}(nA)} \tag{14}$$

The monte-carlo simulation is performed on FOM for 1000 samples where μ and σ are observed to be 1.816ppm/°C^2 and 0.432ppm/°C^2 respectively.

The variation of I_{REF} with load resistance is shown in Fig. 10b from which it is evident that the proposed I_{REF} can

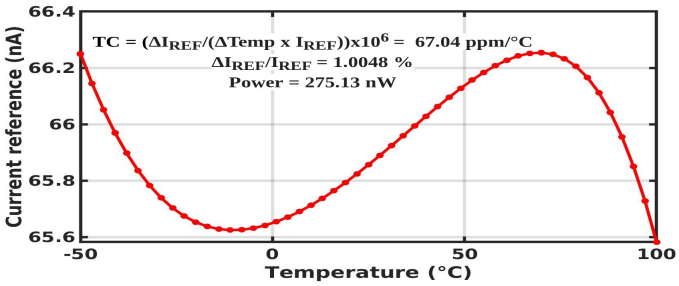

Fig. 4. I_{REF} as a function of temperature @ TT corner

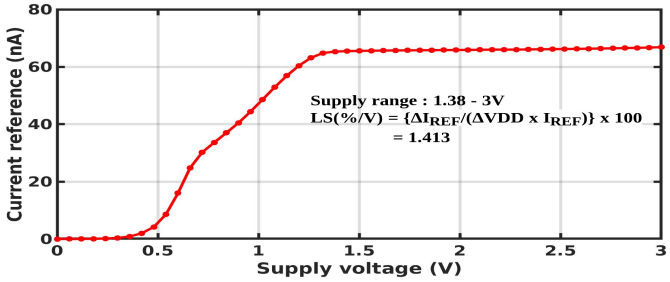

Fig. 5. I_{REF} as function of supply voltage @ TT corner

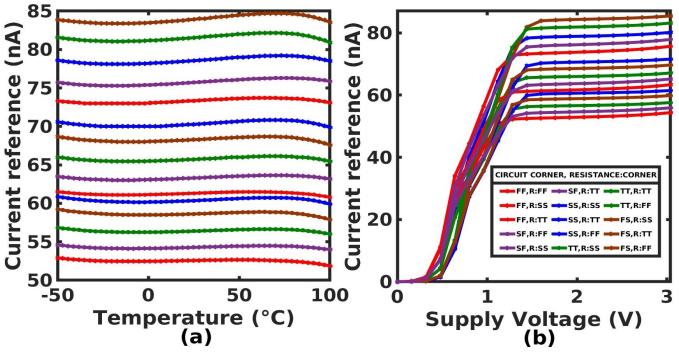

Fig. 6. (a) I_{REF} vs Temp. (b) I_{REF} vs supply

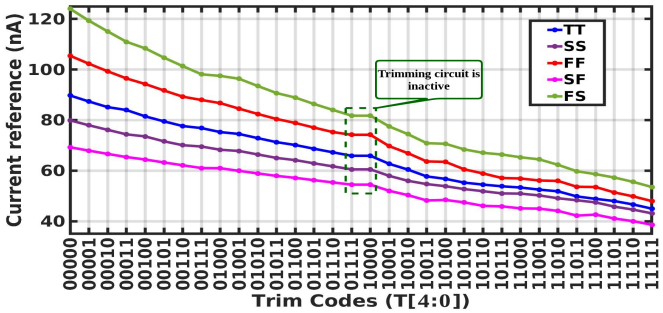

Fig. 7. I_{REF} variation with trim codes

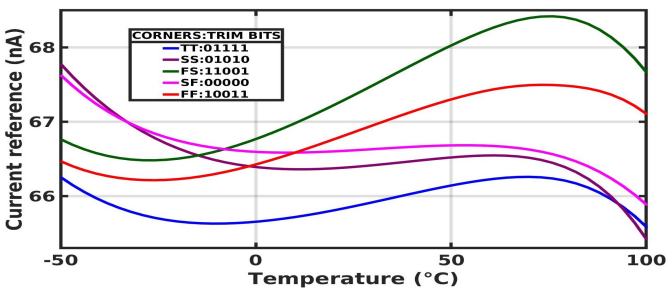

Fig. 8. I_{REF} vs Temp. @Trimmed

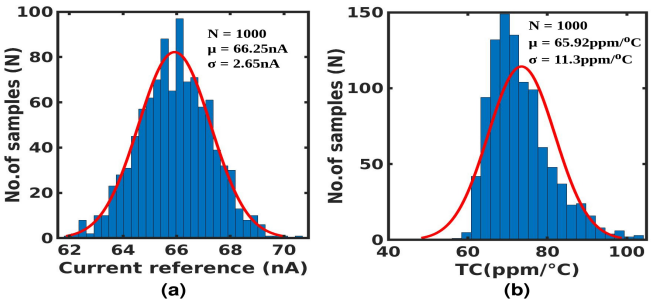

Fig. 9. Monte-Carlo for (a) I_{REF} (b) TC

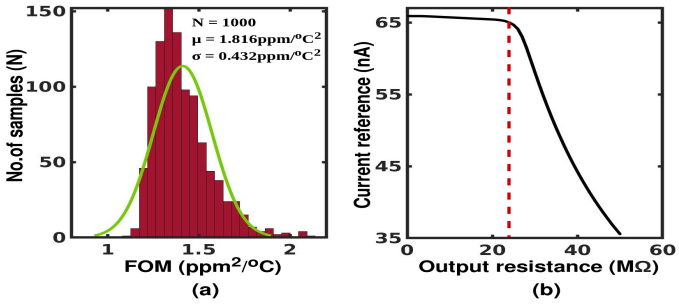

Fig. 10. (a) Monte-Carlo for FOM (b) I_{REF} vs load resistance

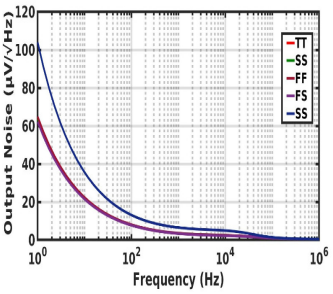

Fig. 11. Output Noise

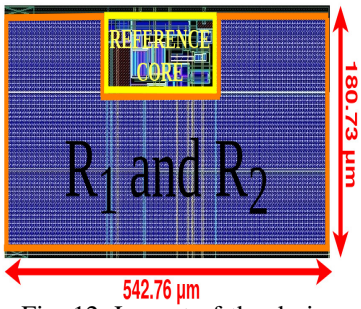

Fig. 12. Layout of the design

support the loads up to 22MΩ. Besides, a noise analysis is also presented for different process corners as shown in Fig. 11. An optimized layout is done for the proposed design as shown in Fig. 12. The design occupies an active area of 0.098mm^2. Additionally, Table I presents the comparison of the proposed architecture with recent endeavors. It is evident that the proposed work provides a relatively stable current for wide temperature and supply voltage range across all the process corners.

IV. CONCLUSION

A highly stable ultra-low power CMOS current reference using curvature compensation scheme is proposed. It is able to achieve relatively low temperature coefficient with unaltered slope in all possible skewed corners. The design can work for a minimum supply voltage of 1.38V which makes it attractive for low voltage applications. Moreover, it operates over a wide range of temperature and supply voltage. From the obtained specifications, it can be concluded that the proposed design is reliable for high precision low-power applications.

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