Design of 2.87 GHz Frequency Synthesizer with Programmable Sweep for Diamond Color Defect based CMOS Quantum Sensing Applications

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Design of 2.87 GHz Frequency Synthesizer with Programmable Sweep for Diamond Color Defect based CMOS Quantum Sensing Applications

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Abstract—Recently, diamond color defect based quantum sensing applications such as nitrogen-vacancy (NV) center magnetometry have emerged in CMOS technology, which use optically detected magnetic resonance (ODMR) for sensing magnetic field strengths (|$B_0$|) from different environmental physical quantities. For ODMR based sensing, CMOS quantum sensors seek an on-chip 2.87 GHz microwave (MW) signal generator. Moreover, in order to sense smaller $|B_0|$, these CMOS quantum sensors also require that MW signal should be swept with sufficiently small step-size near 2.87 GHz. In this work, we present a fractional-N synthesizer based 2.87 GHz MW-generator (MWG) with an extremely small programmable sweep-step size for improved sensitivity of $|B_0|$ measurements in CMOS NV magnetometry. The proposed MWG is implemented in 180 nm CMOS technology and simulations were done to validate the proposed design. Post-layout simulation results show that the proposed MWG achieves a minimum sweep-step size of 50 kHz, which can be used to sense $|B_0| < 0.9$ µT and exhibits a phase noise of -114.5 dBc/Hz at an offset of 1 MHz near 2.87 GHz center frequency.

Index Terms—Quantum-sensing, nitrogen-vacancy, magnetometry, ODMR, colour-defect, diamond, CMOS, sensitivity

I. INTRODUCTION

Quantum sensing has a wide array of applications in material science, mesoscopic physics and life science. Nitrogen-Vacancy (NV) centre in diamond behaves as an isolated electronic spin system that can be used in quantum sensors [1]. When a vacancy replaces the adjacent carbon pair in a diamond lattice, the nitrogen atom and the vacancy form an NV centre. The NV defect has its ground level in a spin triplet state whose sub-levels are split in energy into a singlet ($m_s = 0$) and a doublet of degenerate levels ($m_s = \pm 1$) separated by 2.87 GHz [2]. When an external magnetic field is applied on the NV ground state spin triplet, a Zeeman shift of energy $\gamma_e B_z$ is induced, where $B_z$ represents the magnetic field component along the NV symmetry axis. As shown in Fig. 1(a), optically detected magnetic resonance (ODMR) technique can be used in NV-based sensing to measure static or slow varying $|B_z|$ [1], [2]. In ODMR, NV electron spin transitions are excited by a microwave signal ($f_{RF}$) near 2.87 GHz and diamond is irradiated with a green light, which produces a red light proportional to $|B_z|$ and having photon frequency $\Delta f_p$ given in Eq. (1) [1], which is detected using a photo-diode.

$$\Delta f_p = f_+ - f_- = 2\gamma_e |B_z|$$ (1)
Section IV presents post-layout simulation results followed by the conclusion in section V.

II. ARCHITECTURE OVERVIEW AND DESIGN CONSIDERATIONS

A. Architecture overview

From Eq. (1), to detect $|B_2| < 1 \mu T$, $\Delta f_p$ of 56 kHz is needed, which requires that MWG signal should be varied near 2.87 GHz with a resolution $<56$ kHz. For this, as shown in Fig. 1(b), a phase-locked loop (PLL) based fractional-N frequency synthesizer has been presented in this work, which contains a crystal oscillator (XO) to generate reference signal ($f_{ref}$), phase/frequency detector (PFD), a charge pump (CP), a loop filter (LPF), a voltage controlled oscillator (VCO) and a programmable divider. Important considerations of MWG design are discussed in the following subsection.

B. Design considerations

a) Low gain VCO: For $< 1 \mu T$ sensitivity, VCO shown in Fig. 1(b) should be able to achieve frequency resolution ($\Delta f$) of 50 kHz with low phase noise while providing a sufficiently wide tuning range. For low frequency resolution, the gain of the VCO ($K_{VCO}$) can be estimated by Eq. (4)

$$\Delta f = K_{VCO} \times \Delta V_{cont}$$

(2)

where, $\Delta V_{cont}$ is the change in control voltage at VCO input. Very small values (few 100’s $\mu V$) of $\Delta V_{cont}$ are more prone to noise, whereas larger values (10’s of mV) will require extremely low $K_{VCO}$. Considering this, a value of 1 mV is considered for $\Delta V_{cont}$, which requires a VCO with $K_{VCO} = 50$ MHz/V at $f_{RF} = 2.87$ GHz. To achieve this low $K_{VCO}$ requirement, there are two choices for the VCO realization - 1) LC VCO or 2) ring VCO with CMOS inverters. LC VCO choice results in increased chip area and possibility of degradation of field homogeneity in the sensing area [1] due to the magnetic coupling between on-chip inductor and $|B_2|$. Therefore, as shown in Fig. 1(b), an M-stage ring oscillator (RO) topology is chosen in the proposed work, for which, oscillation frequency ($f_{RF}$) can be given by Eq. (3).

$$f_{RF} = \frac{1}{2M \tau_d}$$

(3)

In Eq. (3), $\tau_d (\propto C_T)$ is the delay of each stage, where $C_T$ is the total capacitance at each node. Gain of the ring VCO can be expressed by Eq. (4) given below.

$$|K_{VCO}| = \frac{\partial f_{RF}}{\partial V_{cont}} = \frac{1}{2M \tau_d^2 \frac{\partial \tau_d}{\partial V_{cont}}} = 2M f_{RF}^2 \frac{\partial \tau_d}{\partial V_{cont}}$$

(4)

Eq. (4) gives important insights about designing low gain ring VCO - 1) by minimizing M and 2) by making $C_T$ a weaker function of $V_{cont}$ to reduce $\frac{\partial \tau_d}{\partial V_{cont}}$.

b) Programmable divider: In order to obtain a resolution of $\Delta f$ near $f_{RF}$, the divider must divide by $(N + 1)$ for a fraction $x$ of the cycles of reference signal having frequency $f_{ref}$ and divide by $N$ for the remaining cycles, which are related as shown in Eq. (5) [5].

$$f_{RF} + \Delta f = (N + x)f_{ref}$$

(5)

Using Eq. (5), under locked condition ($f_{RF} = N \times f_{ref}$), $x = \frac{\Delta f}{f_{ref}}$. As depicted in Fig. 1(b), a modulus control signal is generated by considering $x = \frac{p}{q}$, where $p$ and $q$ are the number of total reference cycles and number cycles for which the modulus signal is low, respectively. This modulus control signal programs the divider for fractional-N operation and switches the center frequency of the VCO. Very low $f_{ref}$ will require high N resulting into more area and dynamic power consumption, whereas very high $f_{ref}$ will make $x$ too small, which will require more number of reference cycles for fractional-N operation. Considering these points, we chose $f_{ref} \approx 90$ MHz, which gives N=32.

III. DESIGN IMPLEMENTATION

This section of the paper elucidates the design details of different modules of the proposed MWG.

A. Low gain ring VCO design

Fig. 2 depicts the proposed ring VCO. As suggested in section-II-B, the proposed VCO uses the minimum number (M=3) of CMOS inverter stages with varactor and a capacitor bank at each node. As shown in the figure, each capacitor bank contains a fix capacitance ($C_{fix}$) and parallel combination of 6 unit capacitance ($C_u$), which are realized using MIM capacitors. $C_u$ is used for the coarse tuning of the VCO and is controlled by a 6-bit signal ($A_5...A_0$), which is generated by the control logic shown in the figure. MOS varactors are controlled by $V_{cont}$ and facilitate the finer tuning of $f_{RF}$ [6]. Varactors with minimum size have been used for having the least value of $\frac{\partial f_{RF}}{\partial V_{cont}}$ for low $K_{VCO}$ as shown in Eq. (4). In the proposed VCO design, $A_0$ is connected to supply, $A_2$, $A_3$, $A_4$ and $A_5$ are connected to ground while $A_1$ is connected to the modulus control signal. The capacitor bank MIM capacitors sizes are selected such that two bands are centered at 2.87 GHz and 2.87+$f_{ref}$ GHz and the other bands are such that the overall tuning range is maximized near 2.87 GHz.

B. Frequency Divider

As shown in Fig. 3(a), the programmable divider of the proposed MWG consists of three True Single-Phase Clock (TSPC) D flip-flops and a 4/5 prescaler that clocks the TSPC stages controlled by $MC_1$, which is NOR of the input of each of the TSPC stages and the modulus control signal [7]. Each TSPC stage acts as divide by 2 unit. The 4/5 prescaler shown in Fig. 3(b) consists of TSPC stages and the required NAND
Table I shows the values of post-layout simulated tuning ranges and \( K_{\text{VCO}} \) of the proposed VCO for different control signals. As shown in the table, the proposed VCO achieves an overall tuning range of 2.515 - 3.069 GHz and attains \( K_{\text{VCO}} \leq 50 \text{ MHz/V} \) near 2.87 GHz, which also facilitates the fractional-N operation for fine frequency sweeping.

As shown in Fig. 6(a), the proposed VCO also achieves significantly low \( K_{\text{VCO}} \leq 52 \text{ MHz/V} \) across all tuning ranges.

**IV. POST LAYOUT SIMULATION RESULTS**

Fig. 5 shows the layout of the proposed MWG in 180 nm CMOS technology, which occupies about 273\( \mu \)m \( \times \) 152\( \mu \)m. Table I shows the values of post-layout simulated tuning ranges and \( K_{\text{VCO}} \) of the proposed ring VCO for different control signals. As shown in the table, the proposed VCO achieves an overall tuning range of 2.515 - 3.069 GHz and attains \( K_{\text{VCO}} \leq 50 \text{ MHz/V} \) near 2.87 GHz, which also facilitates the fractional-N operation for fine frequency sweeping.

As shown in Fig. 6(a), the proposed VCO also achieves significantly low \( K_{\text{VCO}} \leq 52 \text{ MHz/V} \) across all tuning ranges.

**C. PFD/CP/LPF/XO**

Fig. 4(a) shows the block diagram of the PFD, which consists of two D-flip-flops and an AND gate [9]. The two flip-flops shown in Fig. 4(a) have their inputs connected to supply and clocked by the reference signal \( f_r \) and divider output \( (\text{Div}) \), respectively. They generate the Up and Down pulses for driving the charge pump (CP) according to the phase difference in the reference and divider output signals [5]. Fig. 4(b) shows the topology used to realize CP based on the dynamic current-matching technique, which minimizes current mismatches by using additional feedback transistors that compensate for the channel length modulation [10]. As shown in figure, the loop filter comprised of \( R_1 \), \( C_1 \) and \( C_2 \) [9]. Fig. 4(c) shows the Pierce oscillator topology, which is used to realize the crystal oscillator to generate external reference in the proposed MWG [11].
Fig. 7. Post-layout simulation results showing (a) PLL signals in locked state (b) DFT of PLL output locked at 2.87 GHz and (c) PLL phase noise plot shown in Table I. Moreover, as shown in the figure, variation in $K_{VCO}$ values across the bands is also very small (<16 MHz/V). Fig. 6(b) shows that the VCO phase noise at a 1 MHz offset near 2.87 GHz frequency $<$ -90.6 dBc/Hz across the process corners. Fig. 7(a) shows the transient response of the proposed MWG in phase locked state. Fig. 7(b) presents the DFT plot showing the proposed MWG in phase locked state. Fig. 7(b) presents the DFT plot showing $f_{RF} = 2.87$ GHz synthesized by the proposed MWG. Fig. 7(c) shows that the phase noise of the 2.87 GHz MWG signal is -114.5 dBc/Hz at an offset of 1 MHz. The proposed MWG consumes about 11.14 mW of power from a 1.8 V supply.

To get a frequency shift of 50 kHz in $f_{RF} = 2.87$ GHz, modulus control of the divider is programmed for $x = \frac{1}{7175}$. Value of $x$ implies that the programmable divider must divide by 33 for 4 cycles every 7175 cycles and divide by 32 for the remaining 7171 cycles. Similarly, $x = \frac{8}{7175}$ for 100 kHz shift. The time period (T) of the 89.6875 MHz crystal oscillator is 11.1498 ns, which gives timing information for the divide by 33 (N+1) control as $4 \times T$ and divide 32 (N) control as $7171 \times T$. Similarly, for 100 kHz shift timing for divide by 33 and 32 control signals are $8 \times T$ and $7167 \times T$, respectively. Fig. 8(a) and 8(b) show DFT plots for 50 kHz and 100 kHz shifts in $f_{RF} = 2.87$ GHz obtained using the corresponding modulus control signals, respectively. Table II presents the performance summary and comparison of the proposed design with other works. As shown in the table, proposed MWG achieves lower $K_{VCO}$ and frequency resolution as compared to the other works while providing significant improvement in the magnetic field sensitivity.

V. CONCLUSION

In this work, a 2.87 GHz microwave signal generator (MWG) with a minimum sweep-step size of 50 kHz has been presented for NV-ODMR based CMOS quantum sensing applications to detect $< 1 \mu T$ magnetic field strengths ($|\vec{B}|$). Conventionally, for ODMR, the 2.87 GHz signal is frequency modulated using an external source, which drastically increases power consumption and system complexity. This work presented MWG with on-chip programmable sweep capability to generate microwave signals close to 2.87 GHz for improved sensitivity of $|\vec{B}|$ measurement in NV-ODMR. The proposed MWG has been implemented in 180 nm CMOS technology and its operation is validated by post-layout simulations, which show that it achieves a phase noise of -114.5 dBc/Hz at an offset of 1 MHz near 2.87 GHz frequency, while consuming 11.14 mW from 1.8 V supply. Post-layout simulations also show that the proposed MWG has a tuning range of 2.515 to 3.069 GHz with a low gain VCO that exhibits $K_{VCO} < 51.67$ MHz/V and can be used to sense $|\vec{B}| < 0.9 \mu T$, which is much lower as compared to the other existing works.

TABLE II

<table>
<thead>
<tr>
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<td>13.42†</td>
<td>1245.23‡</td>
<td>13.42†</td>
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<td>$K_{VCO}$ (MHz/V)</td>
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<td>180</td>
<td>740</td>
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<td>50</td>
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<td>Phase Noise (dBc/Hz)</td>
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<td>-88 @ 3kHz</td>
<td>-90 @ 1.5kHz</td>
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<td>Power (mW)</td>
<td>&gt;12.5**</td>
<td>&gt;12.5**</td>
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<td>&gt;12.5**</td>
<td>10</td>
<td>6.4</td>
<td>11.14</td>
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* Frequency range is not given so the given center frequency is mentioned. Calculated using the $K_{VCO}$ value assuming 1mV steps in $V_{cont}$. † Reported 245 nT/$\sqrt{Hz}$, 32 $\mu T$/V/$\sqrt{Hz}$, 245 nT/$\sqrt{Hz}$ and 73 $\mu T$/V/$\sqrt{Hz}$ in the given noise bandwidth. ‡ The $K_{VCO}$ values are calculated using the tuning range and control voltage range. ** Estimated using charge pump current and supply voltage values given.
REFERENCES


