A Compact, Power Efficient, Self-Adaptive and PVT Invariant CMOS Relaxation Oscillator

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A Compact, Power Efficient, Self-Adaptive and PVT Invariant CMOS Relaxation Oscillator

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***Abstract*—This brief presents a novel PVT-invariant CMOS relaxation oscillator for Real-Time Clock (RTC) applications. The proposed design is compatible to work in a low supply voltage domain of SoC. The PVT invariance is achieved by a unique circuit implementation of introducing a self-adaptive mechanism that dynamically modifies the time constant of the oscillator core. Moreover, the design is accompanied by a digital calibration unit for further process compensation. Besides, the introduced supply independent bias circuit has greatly improved the supply regulation of the oscillator frequency. In addition, the design utilizes a complementary to absolute temperature (CTAT) current for temperature compensation. Area efficiency is enhanced by replacing bigger passive device i.e, resistor with an adaptive MOS resistor. The obtained results show that the minimum temperature coefficient (TC) of 31.236ppm/$^\circ$C is achieved over a range of -40°C to 100°C. The resultant phase noise of -140dBc/Hz@1MHz is observed. The design has achieved a good power efficiency of 1.65nW/KHz at room temperature without a calibration unit. The line sensitivity (LS) of 0.1159%/V is noted in the range of 0.7V to 1.2V. Nevertheless, the entire system occupies an active area of 0.0509mm^2 with a power consumption of 90nW@0.7V. Also, the leakage current of the complete system is $<$54pA. Therefore, the proposed design aims at providing a production-friendly, ease of integration and low-cost solution.**

***Index Terms*—Compact, Self-adaptive, Current bias, PTAT, CTAT, RTC, TC, LS, SoC, IoT, Relaxation oscillator**

I. Introduction

From compact sensors to advanced multi-core smartphones, various IoT devices hold precision and power efficiency as critical factors [1]. Efficient management of switch on-off time acts as a key to minimize the power consumption. Therefore, maintaining accurate time is crucial for such type of devices. This is embraced by an on-chip RTC to retain reliable information of event occurrences. In addition, RTC's interrupt management to alert the micro-controller host evaluates the robustness of the device. An RTC maintains a precise track of time by counting the oscillator cycles. Ultimately, the oscillation frequency (32.768KHz) is bounded by a speculation of time resolution and low power. Although the stable and precise nature of crystal oscillators (XOs) serve the purpose [2], they have few downsides. For being bulky, expensive and having high power consumption, the replacement of XOs is highly recommended [3]. Focused research has been carried out for years on CMOS based oscillator architectures with sophisticated compensation techniques for reducing PVT variations. However, boosting the stability at low frequencies with low complexity, area and power have been a major challenge for next-generation IoT applications.

Few prior works [4]–[7] have proposed low frequency ($\approx$32.7KHz) designs with an exceptional performance in power (nW). These architectures have greatly reduced the temperature and supply dependencies but still the minimum supply voltage requirement is $\geq$1V. This induces compatibility issues with low supply IoT nodes. In [8] and [9], authors have reported a good power efficiency of 1.66nW/KHz and 0.93nW/KHz with minimum supply voltage of 0.85V and 0.4V respectively. [9] exploited the comparator's temperature-dependent delay to achieve frequency stability but for constrained temperature range (-20°C to 70°C). The comparator's offset and delay acts as a key hindrance to low power design. However, some recent works [6], [10]–[13] have overcome this drawback with the remarkable offset cancellation schemes. The design in [14] has adopted the half-period pre-charge compensation scheme to enhance TC in a wide temperature range (-55°C to 125°C). On top of that, architecture in [14] has low power (51nW), low supply (0.5V) and low frequency (32.7KHz) but the process variations are not considered.

In view of this background, an area and power efficient CMOS oscillator with PVT compensation is put forward to cater a wider range of low voltage IoT applications. The architectural details and simulation results are elaborated in section II and III respectively with conclusions are drawn in IV.

II. Circuit Configuration

A. Architecture Overview

The proposed architecture is shown in Fig. 1. A CMOS-based offset compensated relaxation oscillator is used as a core (Fig. 1a). The conventional RC oscillator designed for low power applications requires a resistance of higher value which occupies more area. In addition to this the presence of temperature-dependent sources like a) RC time constant b) Delay due to inverter, schmitt trigger and comparator c) leakage currents through switches makes the frequency (f_{clk}) temperature sensitive. Consequently, a PTAT (proportional to absolute temperature) behavior of the oscillator's frequency is noted as explained in [15]. To cancel out the PTAT temperature dependence of f_{clk}, a proportional amount of CTAT current (I_{CTAT}) is pushed into the oscillator core.

To enhance the area efficiency, the resistor is replaced by a MOSFET (Fig. 1a) biased in triode region with the aid of a

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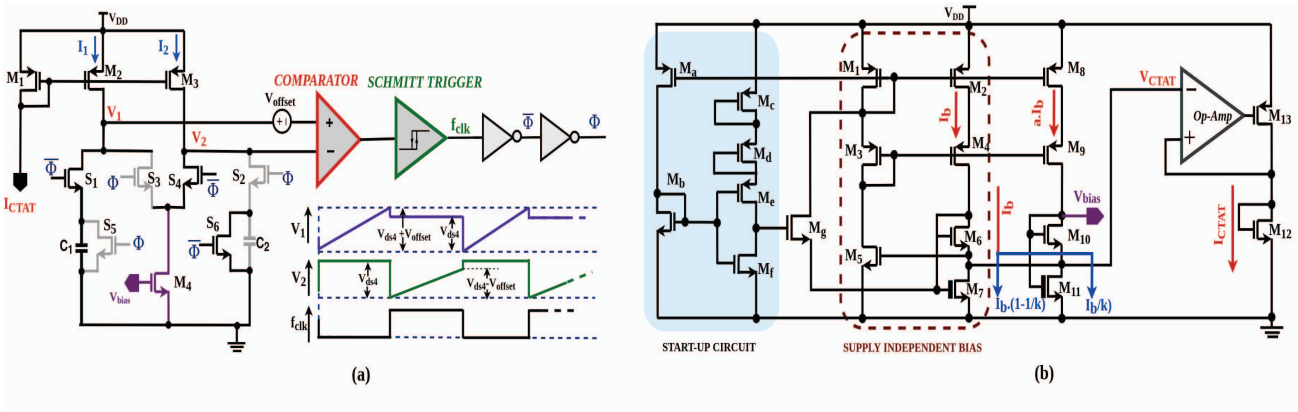

Fig. 1. Schematic of Proposed Architecture (a) Oscillator Core (b) Bias Generator

temperature and supply independent bias voltage (V_{bias}). This V_{bias} is generated by the introduced current mixing technique (Fig. 1b). Supply variations can be reduced either directly through the use of voltage regulator or indirectly through the architectural design [16]. A common supply independent biasing circuit employed to generate V_{bias} and I_{CTAT} (Fig. 1b) aided in improving line sensitivity of frequency. Process dependency of capacitor and I_{CTAT} directly effect the period of oscillation. These variations are mitigated partly through a self-tracking bias compensation and completely through a one-time digital calibration setup (Fig. 2) as explained in the subsequent sections.

The comparator's offset (V_{offset}) compensated CMOS oscillator shown in Fig. 1a requires one-cycle of start-up time to generate f_{clk}, ϕ and $\overline{\phi}$ which are responsible for controlling the switches (S_1, S_2, S_3, S_4, S_5 and S_6). A schmitt trigger is added to mitigate the glitches occurring in the generated clock. The complete operation of the oscillator (Fig. 1a) can be explained in two phases. In phase 1, ϕ = 0 turns on S_1 and S_4. Hence, V_1 ramps up to V_{ds4} + V_{offset} while V_2 = V_{ds4}. The comparator inverts ϕ when V_1 overtakes V_2. In phase 2, ϕ = 1 turns on S_2 and S_3. Hence, V_1 = V_{ds4} while V_2 ramps up to V_{ds4} - V_{offset} compensating the effect of offset. The duration of two phases can be written as,

$$t_{phase1}(\phi = 0) = (V_{ds4} + V_{offset})\frac{C_1}{I_1} + t_d \quad (1)$$

$$t_{phase2}(\phi = 1) = (V_{ds4} - V_{offset})\frac{C_2}{I_2} + t_d \quad (2)$$

Here C_1 = C_2 = C, I_1 = I_2 = I and t_d is the combined delay of comparator (t_{dc}), schmitt trigger and inverter (t_{di}). The duration of clock pulse (t_{clk}= t_{phase1}+ t_{phase2}) is given by,

$$t_{clk} = (2V_{ds4})\frac{C}{I} + 2t_d \quad (3)$$

Hence, the effect of comparator's offset is compensated.

B. Bias Generation for Oscillator Core

To generate supply insensitive V_{bias} and I_{CTAT}, there is a requirement of supply independent current (I_b) which is realized by M_1-M_7 as shown in Fig. 1b. To generate I_b in the order of nano-amperes, M_5 should be biased in sub-threshold region. This is achieved by biasing M_5 with the output voltage of cascode pair formed by M_6 and M_7. M_2 and M_4 senses the supply variations which are attenuated by M_5 through the feedback formed by M_5-M_7. For proper operation in sub-threshold region, the high impedance transistors M_2, M_4, M_5, M_8 and M_9 should absorb at least $V_{DS} \approx 4V_T$. Therefore, the minimum supply voltage requirement is bounded to 0.7V (approximately). The drain current equation of the MOSFET biased in sub threshold region is given by [17]:

$$I_D = I_S(W/L)\exp(\frac{V_{GS} - V_{th}}{\eta V_T})(1 - \exp(\frac{-V_{DS}}{V_T})) \quad (4)$$

For $V_{DS} > 4V_T$, I_D is almost independent of V_{DS} which is given by,

$$I_D = I_S(W/L)\exp(\frac{V_{GS} - V_{th}}{\eta V_T}) \quad (5)$$

$$V_{GS} = V_{th} + \eta V_T \ln(\frac{I_D}{I_S(W/L)}) \quad (6)$$

where $I_S = \mu(\eta - 1)C_{ox}V_T^2$, V_{th} is the threshold voltage of transistor, V_T is the thermal voltage, μ is mobility and η is the sub-threshold slope factor.

From the circuit (Fig. 1b), the core equation can be written as [18],

$$V_{GS7} = V_{GS5} + V_{GS6} \quad (7)$$

By substituting (6) in (7), on simplification, the current (I_b) is obtained as,

$$I_b = \frac{(W/L)_5(W/L)_6\eta\mu C_{ox}V_T^2}{(W/L)_7}\exp(\frac{\Delta V_{th}}{\eta V_T}) \quad (8)$$

where $\Delta V_{th} = V_{th5} + V_{th6} - V_{th7}$. Since the circuit is self-biased, a start-up circuit is used to avoid undesired biasing condition.

The proposed current mixing (Fig. 1b) between supply independent bias and cascode pair (M_{10}, M_{11}) provides flex-

ibility to control TC of V_{bias} whose mathematical analysis is presented below. The current flowing M_{11} is given by:

$$I_{D11} = (aI_b + \frac{I_b}{k}) = I_S(W/L)_{11} \exp(\frac{V_{GS11} - V_{th11}}{\eta V_T}) \quad (9)$$

$$V_{bias} = V_{GS11} = V_{th11} + \eta V_T \ln(\frac{I_b(a + \frac{1}{k})}{I_S(W/L)_{11}}) \quad (10)$$

On substituting (8) in (10),

$$V_{bias} = \underbrace{V_{th11} + \Delta V_{th}}_{\text{CTAT}} + \underbrace{\eta V_T \ln(\frac{(a + \frac{1}{k}).(W/L)_5(W/L)_6}{(W/L)_7(W/L)_{11}})}_{\text{PTAT}} \quad (11)$$

Hence, V_{bias} can be adjusted to have low temperature sensitivity (Fig. 6a) by varying the sizes of M_5, M_6, M_7 and M_{11}.

In addition, I_{CTAT} is generated by applying a CTAT voltage (V_{CTAT}=V_{ds9} ≈320mV) across a diode connected MOSFET (M_{12}) with the help of op-amp in negative feedback configuration (Fig. 1b).

$$V_{CTAT} = V_{ds7} = \underbrace{\eta V_T \ln \frac{(W/L)_7}{(W/L)_6}}_{\text{PTAT}} + \underbrace{(V_{th6} - V_{th7})}_{\text{CTAT}} \quad (12)$$

By assigning $(W/L)_7$=$(W/L)_6$ in (12), an accurate CTAT voltage is generated. Hence, I_{CTAT} is given by,

$$I_{CTAT} = V_{CTAT}.(R_{out,M_{12}})^{-1} \quad (13)$$

where, $R_{out,M_{12}}$ is the output resistance of M_{12}. An approximate CTAT current is generated as shown in Fig. 6b which is obvious from (13).

C. Temperature Compensation

The combined delay t_d (comparator, schmitt trigger and inverters) is observed to have negative temperature dependency (f_{clk} is having PTAT behaviour as explained earlier). The delay of comparator (t_{dc}) mainly relies on finite bandwidth (τ_{BW}) and switching threshold of the buffer stage followed by the comparator (τ_{SW}). The negative temperature dependency of the t_{dc} can be approximated as: $t_{dc} = t_{dc0}$ (1-AT) [9]. In addition, the delay of the inverter (t_{di}) can be written as $t_{di} = t_{di0}$ (1+BT) [19]. By considering the dominant dependence of the combined delay (t_d) on comparator's delay t_{dc}, overall delay can be considered as:

$$t_d = t_{d0}(1 - PT) \quad (14)$$

By taking negative temperature dependency into consideration, (13) can be written as:

$$I_{CTAT} = V_{CTAT}.(R_{out,M_{12}})^{-1} = I_0(1 - QT) \quad (15)$$

Where A, B,P and Q are temperature coefficients. From (14),(15) and (3):

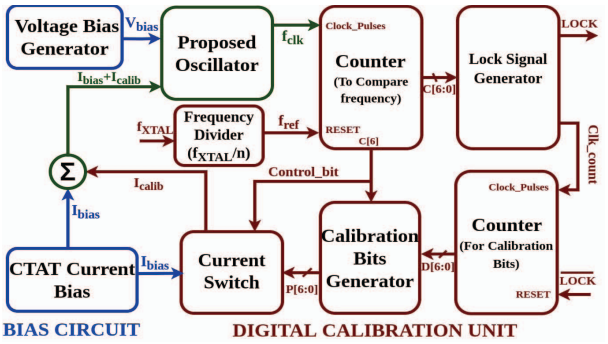

Fig. 2.Block Diagram of Proposed Architecture

$$t_{clk} = \underbrace{(2V_{ds4})\frac{C}{I_0(1 - QT)}}_{\text{T}^+} + \underbrace{2t_{d0}(1 - PT)}_{\text{T}^-} \quad (16)$$

In (16), the terms T^+ and T^- exhibit positive and negative temperature dependencies respectively. To compensate T^-, T^+ is adjusted by varying the slope of V_{CTAT} (from (12) and (13)) which thereby resulted in f_{clk} with minimum temperature dependence (Fig. 7(b)).

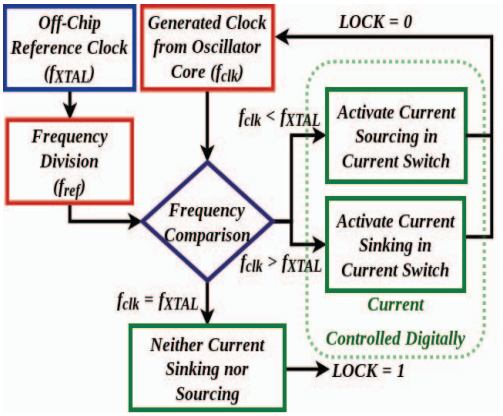

Fig. 3. Digital Calibration Algorithm

D. Process Compensation

1) Self-Tracking Bias Compensation: From (3), it is clear that any process variations in C, I and V_{ds4} have a great influence on t_{clk}. The effective resistance (R_{on,M_4}) of M_4 is nothing but V_{ds4}/I, in which I (=k.I_{CTAT}) tends to decrease in slow-slow (SS) corner and increase in fast-fast (FF) corner (Fig. 5b). Therefore, R_{on,M_4} increases and decreases in SS and FF respectively.

To drive M_4 into the triode region, V_{bias} which is invaded to process variations is applied at its gate (Fig. 1). V_{bias} tends to increase in SS and decrease in FF (Fig. 5a).

Therefore, the influence of process variations on I_{CTAT} are in turn compensated by the process dependency of V_{bias} which adaptively modifies the R_{on,M_4} (thereby reducing the effect of process variation on V_{ds4}). Hence, the introduced self-tracking bias compensation aids in scaling down the effect of process variation on oscillator's frequency to an extent.

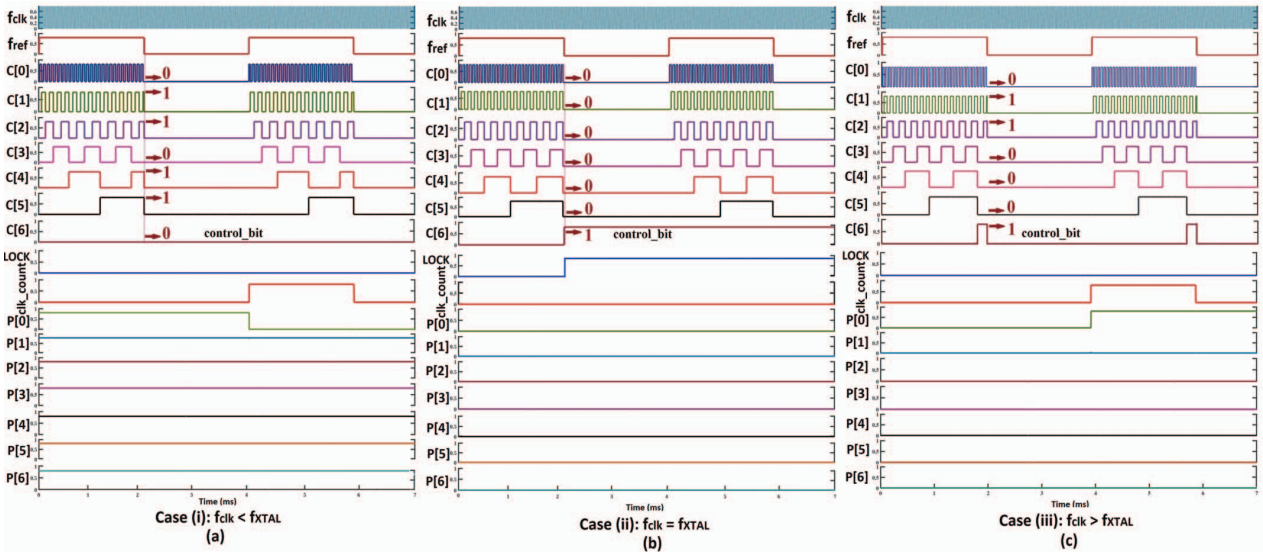

Fig. 4. Waveforms of digital calibration unit

2) One-Time Calibration: Even though the compensation scheme explained previously contributes in reduction of process variations, the effect of other process dependent parameters and mismatches still exists. Consequently, there is a requirement of complete elimination of these variations which is accomplished by a digital calibration unit shown in Fig. 2. The proposed digital calibration algorithm illustrated in Fig. 3 can be explained in three steps.

(i) Sensing the generated frequency: The frequency of an off-chip crystal oscillator (f_{XTAL} =32.7KHz) is given as an input to a frequency divider network to generate a reference pulse (f_{ref}) of frequency f_{XTAL}/n. This f_{ref} acts as a reset signal for the counter as shown in Fig. 2. Analyzing the range of frequency variation before calibration, the requirement of 7-bit calibration is identified to get a decent accuracy thereby making n = 2^7 and f_{ref} = 255.45Hz. The generated clock (f_{clk}) is then applied to the 7-bit synchronous counter whose output is C[6:0]. This represents the count of clock pulses in the corresponding active period of f_{ref}.

(ii) Frequency Comparison: If C[6:0] = 1000000 ($\because f_{clk}/f_{ref}$ = 128), then the desired frequency ≈32.7KHz is obtained. Hence, the LOCK signal is activated which in turn terminates the calibration process (Fig. 4b). In case C[6:0] $<$ 1000000, it implies that $f_{clk} <$ 32.7KHz (Fig. 4a). Similarly, in the other case if C[6:0] $>$ 1000000 then $f_{clk} >$ 32.7KHz (Fig. 4c). In both the cases LOCK = 0, clk_count is generated (Fig. 2) and the calibration process advances to next step (Fig. 3).

(iii) Current Controlling: Whenever $f_{clk} \neq$ 32.7KHz and LOCK = 0, the 7-bit synchronous counter for generating calibration bits (D[6:0]) is triggered with the help of clk_count (Fig. 2). The generated control_bit (= C[6]) is responsible for deactivating the current source part when C[6] = 1 and current sink part when C[6] = 0 (Fig. 3). The calibration bits P[6:0] are assigned to be either D[6:0] in case of sinking or $\overline{D[6:0]}$ in case of sourcing to ensure the step-by-step controlling starting from minimum amount of current (Fig. 10). The presence of both current sink and current source circuits (Fig. 5) decreases the no. of calibration bits (up to 50%) which in turn helps in reducing the no. of counts and achieves more accuracy in less time.

III. Results And Discussion

The proposed oscillator with auto-calibration unit is implemented in TSMC 180nm technology. The TC of V_{bias} and I_{CTAT} is monitored across different corners as shown in Fig. 6a and 6b. The LS of frequency with compensation is plotted as shown in Fig. 7 in a supply range of 0.7V to 1.2V. LS of 0.1159%/V, 0.2016%/V and 0.1879%/V is observed in TT, SS and FF corners respectively. The frequency variation without compensation is observed to be PTAT as shown in Fig. 8a. The impact of self-tracking bias compensation and CTAT current biasing can be noted from Fig. 8b. Further reduction in TC of f_{clk} in various process corners with the help one-time digital calibration can be noticed from Fig. 9. Hence, the design achieved a TC of 31.236ppm/°C, 52.34ppm/°C and 80.87ppm/°C in TT, SS and FF corners respectively at 0.7V supply. To verify the performance of digital calibration unit, the variation of frequency and lock signal with respect to time are monitored. Fig. 10a and 10b clearly depicts the accurate adjustment of frequency during $f_{clk} >$ 32.7KHz and $f_{clk} <$ 32.7KHz respectively. The simulated phase noise is observed to be -61.69dBc/Hz, -90.79dBc/Hz, -140dBc/Hz at 1KHZ, 100KHz and 1MHz respectively at 27°C as shown in Fig. 11.

Furthermore, Fig. 12 presents the montecarlo analysis for 1000 samples on f_{clk}. Mean (μ) and standard deviation (σ) are noted to be 32.776kHz and 500.023Hz respectively with a 3σ inaccuracy of 1.525%. Fig. 13 shows the layout of the proposed design which occupies an active area of 0.0509mm^2. Finally, the performance comparison of proposed design with prior works in presented in Table 1.

TABLE 1 : PERFORMANCE SUMMARY AND COMPARISONS WITH PRIOR WORKS

SPECIFICATIONS	THIS WORK	ISCAS [4] (2017)	APCCAS [5] (2016)	ESSCIRC [6] (2013)	ESSCIRC [8] (2018)	JSSC [13] (2016)
Technology (nm)	**180**	65	180	180	180	180
Frequency (KHz)	**32.7**	32.5	32.67	32.55	32.7	18.5
Minimum supply (V)	**0.7**	1.1	1	1	0.85	0.95
Temperature Range(°C)	**-40 to 100**	-40 to 80	N/A	-40 to 100	-40 to 80	-40 to 90
TC(ppm/°C)	**31.236**	138	N/A	120	99.5	27
Line Sensitivity (%/V)	**0.1159@ 0.7 - 1.2V**	1.39@ 1.1 - 1.3V	N/A	1.1@ 1.0 - 1.8V	0.886@ 0.85 - 1.85V	<5@ 0.95 - 1.05V
Phase noise @ 10KHz @ 1MHz	**-80dBc/Hz -140dBc/Hz**	N/A N/A	N/A N/A	-71dBc/Hz N/A	N/A N/A	N/A N/A
Process Sensitivity (σ/μ)%	**1.52**^{*2}	1.9	1.36^{*1}	1.39	0.83	N/A
Power Efficiency (nW/KHz)	**1.65**^{*1}	8.33	2.6	14.5	1.66	7
Power (nW)	**54**^{*1} **90**^{*2}	271	85^{*1} 190^{*2}	472	54.2	130
Area(mm^2)	**0.0164**^{*1} **0.0509**^{*2}	0.022	0.097	0.021	0.105	0.032
Calibration Unit	**yes**	no	yes	no	no	no
Result Type	**Simulated**	Simulated	Simulated	Measured	Measured	Measured

^{*1}=without calibration ^{*2}=with calibration

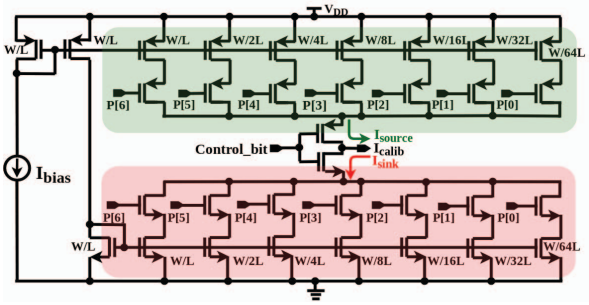

Fig. 5. Current Switch

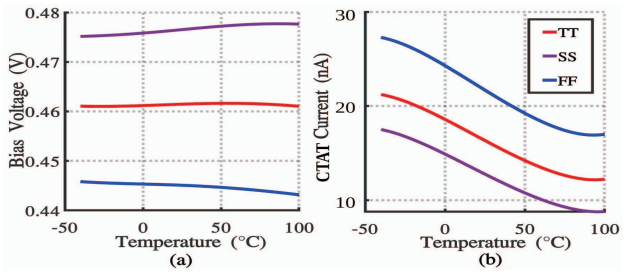

Fig. 6. Temperature Sensitivity of (a) V_{bias} (b) I_{CTAT}

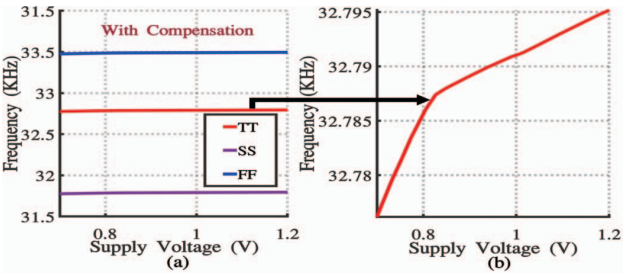

Fig. 7. Line Sensitivity of frequency

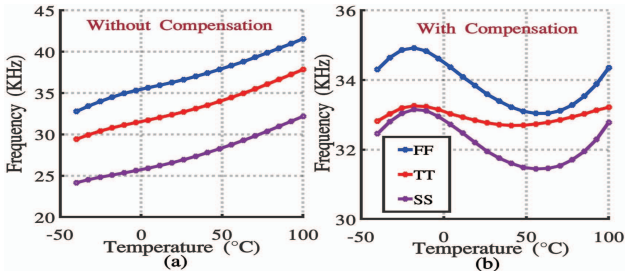

Fig. 8. TC (a) without (b) with Compensation

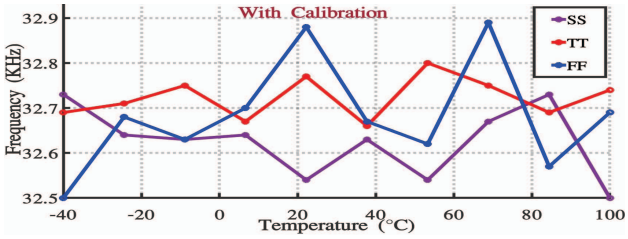

Fig. 9. Frequency vs Temperature with calibration

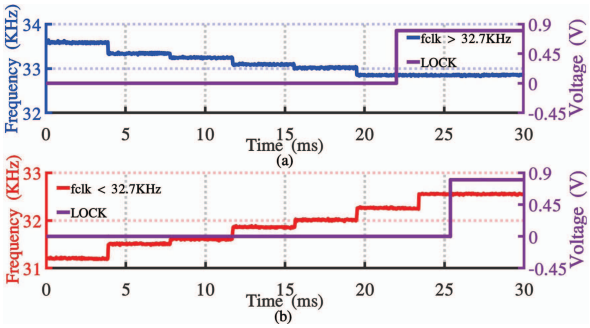

Fig. 10. Calibration (a) $f_{clk} > 32.7$KHz (b) $f_{clk} < 32.7$KHz

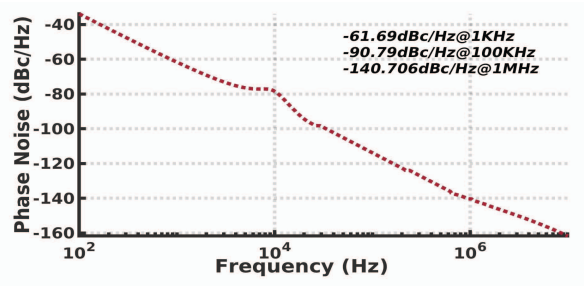

Fig. 11. Phase Noise Analysis

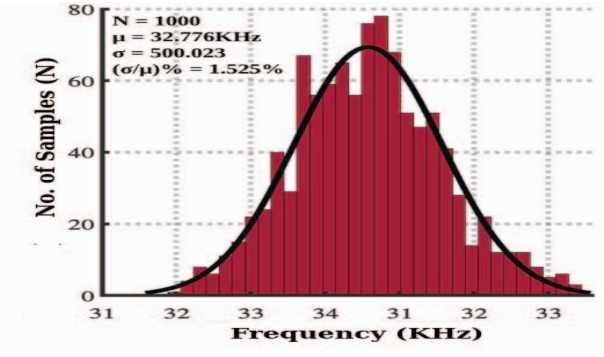

Fig. 12. Monte carlo for f_{clk}

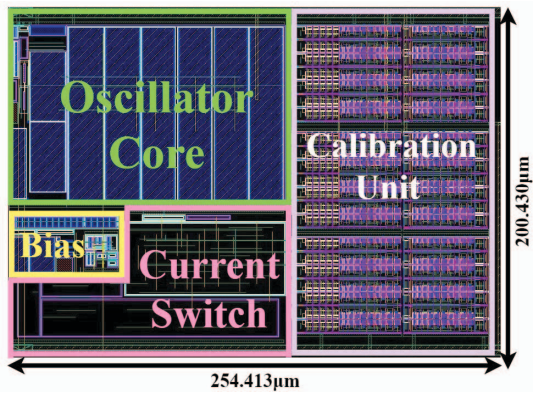

Fig. 13. Layout of Proposed Design

IV. CONCLUSION

A compact self-adaptive CMOS oscillator design has been demonstrated. The proposed innovative circuit solution shows a better power efficiency compared to nearest prior arts. The use of resistor is avoided in the presented architecture which enhanced the area efficiency. A huge improvement in LS is achieved through the designed supply insensitive bias current and voltage. Therefore, low power (90nW) and low supply voltage (0.7 V) attributes make the design compatible with IoT based RTC applications.

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