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A 2.75-2.94 GHz Voltage Controlled Oscillator with Low Gain Variation for Quantum Sensing Applications

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Abstract—Quantum sensing applications such as nitrogen vacancy based magnetometry require phase locked loops (PLL), which can synthesize microwave frequencies in a narrow band near 2.87 GHz. Moreover, it is also required that the PLLs should have low noise and low jitter for high stability and fast settling time. These requirements seek low phase noise voltage controlled oscillator (VCO) with small variation in its gain ($K_{VCO}$) within the desired tuning range. In this paper, we present a technique for designing a low phase noise VCO with low $K_{VCO}$ and small $K_{VCO}$ variation. To validate the proposed technique, an LC VCO has been designed and implemented in 0.18 µm CMOS process and post layout simulation results are presented. The simulation results show that the proposed LC VCO achieves $K_{VCO}$ variation of ±3.82% in the frequency range of 2.75 - 2.94 GHz and exhibits a phase noise of -118.64 dBc/Hz at an offset of 1 MHz, while consuming 9 mW of power from a 1.8 V supply.

Index Terms—VCO, low phase noise, $K_{VCO}$ variation, quantum sensing, oscillator

I. INTRODUCTION

Phase Locked Loops (PLL) are commonly used for high frequency carrier synthesis in wired and wireless transceivers. Recently, quantum sensing applications have also emerged that demand low noise PLLs with high stability and small settling time for microwave frequency generation. For example, nitrogen vacancy based magnetometry applications seek low noise, narrow bandwidth microwave generators near 2.87 GHz with very fine frequency resolution [1]. These low noise PLLs seek voltage controlled oscillators (VCO) with low gain ($K_{VCO}$) and small variation in its gain [2]. Therefore, there is a need to develop VCOs with low variation in $K_{VCO}$ for quantum sensing applications. In this paper, we present - 1) a technique with detailed analysis to reduce the variation in $K_{VCO}$ of LC oscillators, 2) design and implementation of an LC VCO with low $K_{VCO}$ variation in 180 nm CMOS technology and 3) post-layout simulation results to validate the proposed technique for LC VCO design of low $K_{VCO}$ with reduced $K_{VCO}$ variation.

The paper is organized as follows: section II presents the background of this work and review of prior related works. In section III architecture of the VCO and detailed analysis of the proposed low $K_{VCO}$ variation technique is presented. The circuit implementation and simulation results are discussed in section IV and the conclusion is presented in section V.

II. BACKGROUND AND PRIOR WORKS

A. Background

Fig. 1 depicts the block diagram of a PLL, which contains a phase frequency detector (PFD) followed by a charge pump, a loop filter and a voltage controlled oscillators (VCO) [3]. Eq. (1) shows the closed loop transfer function of the PLL [3].

$$ H(s) = \frac{I_p K_{VCO}}{s^2 + \frac{I_p K_{VCO}}{2\pi C_1} R_1 s + \frac{I_p K_{VCO}}{2\pi C_1}} $$

In Eq. (1), the denominator is of the form $s^2 + 2\zeta \omega_n s + \omega_n^2$ and the damping factor ($\zeta$) and natural frequency ($\omega_n$) are represented by equations (2) and (3), respectively, where $I_p$ is the charge pump current, $C_1$ is loop filter capacitance and $R_1$ is loop filter resistance.

$$ \zeta = \frac{1}{2} \sqrt{\frac{I_p C_1 K_{VCO}}{2\pi}} $$

$$ \omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}} $$

$\zeta$ and $\omega_n$ determine the stability of the PLL as well as the phase noise performance [4]. For the loop to remain stable, the value of $\zeta$ should be near unity [4]. The settling speed can be measured using the quantity represented in Eq. (4).

$$ \frac{1}{\zeta \omega_n} = \frac{4\pi}{R_1 I_p K_{VCO}} $$

Fig. 1. Charge-pump PLL

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Important characteristics of the PLL such as phase noise performance and loop characteristics are determined by its VCO. The VCO phase noise ($\phi_{\text{out}}^2$) shaped by the PLL is given by Eq. (5) [4].

$$\phi_{\text{out}}^2 = \frac{\omega^4}{(\omega^2 - \omega_0^2)^2 + 4\zeta^2\omega_0^2\omega^2} \left( \frac{\alpha}{\omega^4} + \frac{\beta}{\omega^2} \right)$$  \hspace{1cm} (5)

where $\alpha$ and $\beta$ are factors which contain information about the noise injected and the Q value, respectively. For a PLL in operation, values of $I_p$, $C_1$, and $R_1$ are fixed and the only scope for large variations is in $K_{VCO}$. From equations (2) - (5), it can be inferred that for given $I_p$, $C_1$ and $R_1$, large variations in $K_{VCO}$ will degrade the PLL stability, settling time and the phase noise performance. In order to ensure operation of the PLL in its desired dynamics, variations in $K_{VCO}$ should be minimized. There have been several techniques proposed in the past to reduce the $K_{VCO}$ variation [5]-[10], which are discussed in the following subsection.

B. Literature review

As shown in Fig. 2(a), [5] uses a switched varactor array connected in parallel with a capacitor bank ($C_{\text{bank}}$) that is used to compensate the variation in $K_{VCO}$ when there is change in value of $C_{\text{bank}}$. When a $C_{\text{bank}}$ structure is connected in series with the varactor, it has higher value of $K_{VCO}$ at higher value of $C_{\text{bank}}$ and when $C_{\text{bank}}$ structure is connected in parallel with the varactor, it has a lower value of $K_{VCO}$ at higher value of $C_{\text{bank}}$. Therefore, as shown in Fig. 2(b), [6] and [7] propose the use of the series and parallel $C_{\text{bank}}$ structure such that their opposite impact on value of $K_{VCO}$ minimizes its variation. As shown in Fig. 2(c), [8] proposes the use of bias shifted inversion mode MOS varactor connected in parallel with conventional accumulation mode MOS Varactor.

For reduced gain variation in ring oscillators, [9] proposed a cross-coupled pair with capacitive degeneration and [10] proposed using peak inductors.

In this work, we present a technique to control $C_{\text{bank}}$ and $V_{\text{bias}}$ simultaneously for reduced $K_{VCO}$ variation in an LC oscillator. The proposed VCO architecture and its detailed analysis is presented in the following subsection.

III. PROPOSED ARCHITECTURE AND DETAILED ANALYSIS

A. Architecture of the Proposed LC VCO With Low $K_{VCO}$ Variation

Fig. 3(a) shows the block diagram of the proposed LC VCO. It consists of an NMOS cross coupled pair with a tail current source, a main tank, an auxiliary tank and a digital to analog converter (DAC). As shown in Fig. 3(a), the main tank is comprised of an inductor ($L$) and switched capacitor bank in parallel. As shown in Fig. 3(a), $C_{\text{bank}}$ structure is controlled by an N-bit digital control signal, which is used for the coarse tuning of the oscillator. Same N-bit signal controls the DAC, which generate the desired bias voltage for varactor capacitance change in the auxiliary tank. As shown in Fig. 3(b), the auxiliary tank consists of MOS varactors, where the voltages at the drain/source and gate terminals of the varactor are denoted by $V_{\text{bias}}$ and $V_{\text{tune}}$, respectively. The capacitors $C_p$ in Fig. 3(b) behave as blocking capacitors to ensure stable biasing of the varactors. MOS varactors have been utilized for the fine tuning of the oscillation frequency in the proposed VCO. This is achieved by changing varactor capacitance with its gate-source voltage ($V_{gs}$).

B. Detailed Analysis for $K_{VCO}$ and its variation

a) Consideration for low $K_{VCO}$: Frequency of the proposed LC VCO topology shown Fig. 3(a) can be given by Eq.
Consider the MOS varactor in Fig. 3(c), which is similar in design to the MOS varactor used in the proposed LC VCO topology. The capacitance of the varactor is given by Eq. (9)

$$C_v = \frac{1}{\sqrt{C_{ox} + \frac{2(V_{gs} - V_{fb})}{qN_a\epsilon_s}}} \tag{9}$$

where, $V_{fb}$ is the flat band voltage of the device and $V_{gs}$ is the gate to source voltage of the varactor, which is given by Eq. (10).

$$V_{gs} = V_{tune} - V_{bias} \tag{10}$$

For mathematical simplicity, the source voltage of this MOS varactor in Eq. (10) is assumed to be equal to $V_{bias}$, which is the mean value of source voltage. For further analysis, we define $V_z$ as shown in Eq. (11).

$$V_z = V_{bias} + V_{fb} \tag{11}$$

Thus, the capacitance of varactor in Fig. 3(c) is obtained by substituting Eq. (10) and Eq. (11) in Eq. (9) to obtain the expression given in Eq. (12).

$$C_v = \frac{1}{\sqrt{C_{ox} + \frac{2(V_{bias} - V_z)}{qN_a\epsilon_s}}} \tag{12}$$

where parameters $C_{fb}$, $C_{ox}$ and $V_{tune}$ represents the flat band voltage of the varactor, oxide capacitance per unit area of the varactor and tuning voltage respectively.

The partial differential of capacitance of MOS varactor with respect to the tuning voltage is obtained in Eq. (13).

$$\frac{\partial C_v}{\partial V_{tune}} = -\frac{1}{qN_a\epsilon_s} \times \frac{1}{(C_{ox} + \frac{2(V_{bias} - V_z)}{qN_a\epsilon_s})^{1.5}} \tag{13}$$

If the points where the difference between $V_{tune}$ and $V_z$ is high, Eq. (13) implies that the change in capacitance of MOS varactor with respect to change in tuning voltage is low, which decreases the $K_{VCO}$ variation, but these points will have low $K_{VCO}$, resulting in very low tuning range. There is a clear tradeoff between tuning range and $K_{VCO}$ variation. Tuning range is more preferred in this short frequency range and therefore, the selected operating points are chosen where the difference between $V_{tune}$ and $V_z$ is low, which will achieve significant tuning range with bearable $K_{VCO}$ variation.

The proposed design methodology attains moderate $K_{VCO}$ variation in a short frequency range, but as larger tuning ranges are required in most applications involving PLLs to ensure locking and reasonable settling times, the VCO makes use of a variable $C_{bank}$ whose values can be switched to obtain outputs in different frequency bands. For an operating point which has a low value of output oscillation frequency, the value of $C_{bank}$ should be high. Eq. (8) shows that the value of $K_{VCO}$ is low at these operating points. Likewise, for an operating point with a high value of oscillation frequency, the $K_{VCO}$ value will be high. By substituting Eq. (13) in Eq. (8), the expression of $K_{VCO}$ is obtained as given by Eq. (14).
IV. DESIGN IMPLEMENTATION AND SIMULATION RESULTS

A. VCO Implementation

Fig. 4(a) shows the complete schematic of the proposed LC VCO with low $K_{VCO}$ variation, which has been implemented in 0.18$\mu$m 6-metal layer CMOS technology. Fig. 4(b) shows the layout of the VCO, which occupies an area of 421.52 $\mu$m x 346.34 $\mu$m. As shown in the Fig. 4(a), oscillator core is implemented with a cross-coupled pair and the tank has been realized with capacitor bank containing total 16 unit capacitance ($C_x$), inductor ($L$), MOS varactors ($C_V$) and blocking capacitances ($C_b$). The capacitor banks ($C_{bank}$) are placed parallel to the inductors ($L$) to get shifts in the output frequency and produce a wide band of overall output frequencies. The fixed capacitance has been realized using a MIM capacitor ($C_{fixed}$) and has a value of 1.09 pF, while each unit capacitance was realized using a combination of MIM capacitors and has an effective value of 20 fF. A 16-bit digital control signal is used to control this operation and the switches used in the capacitor bank are PMOS switches. $C_b$ is taken to be of the order pF while $C_c$ is of the order 10 fF. The blocking capacitors ($C_b$) are MIM capacitors of value 1.15 pF used to provide stable bias voltage to the varactor. The resistances ($R$) are current limiting resistors of 1 k$\Omega$ used to limit the current from the control sources. The MOS varactors used are minimum sized for attaining low $K_{VCO}$ and have a variable capacitance value in the range 21.87 fF - 61.88 fF. The inductors used are symmetric spiral inductors with a quality factor of 5.59. $V_{bias}$ is controlled by using DAC [11] whose input is the same 16-bit digital control signal controlling the $C_{bank}$. These two components are used in conjecture to minimize the variations in $K_{VCO}$, where $V_{bias}$ changes according to the change in $C_{bank}$ values.

B. Simulation Results

This subsection presents the post-layout simulation results of the proposed design shown in Fig 4(a), which has been implemented in 180nm CMOS process. The proposed VCO consumes 5 mA current from a 1.8 V supply. $V_{tune}$ is swept from 300 mV to 800 mV and the output is taken at one of the cross coupled pair gates. Fig. 5 shows the variation

\[
K_{VCO} = \frac{1}{4\pi N_a \varepsilon_s \sqrt{L}} \times \frac{1}{\left(\frac{1}{C_{ox}^2} + \frac{2(V_{tune} - V_z)}{qN_a \varepsilon_s}\right)^{1.5}} \times \left(C_{bank} + C_v\right)^{1.5}
\] (14)

We define the term $Var_{K_{VCO}}$ as given by Eq. (15), which is derived from Eq. (14) by removing all constants and some simplifications.

\[
Var_{K_{VCO}} = \left(\frac{1}{C_{ox}^2} + \frac{2(V_{tune} - V_z)}{qN_a \varepsilon_s}\right)
\] (15)
of VCO frequency for the lowest (near 2.75 GHz), highest (near 2.94 GHz) and center (near 2.83 GHz) frequency bands. Simulation results shown in Fig. 5 depicts that the VCO tuning range is 190 MHz (2.75 - 2.94 GHz) around 2.87 GHz center frequency with $K_{VCO}$ variation in each band is < 20 MHz/V. We also observed a decrease in the tuning range from 2.85 GHz - 3.12 GHz from schematic simulation to 2.75 GHz - 2.94 GHz in post-layout simulations. Table I presents the VCO frequency bands with varying $C_{\text{bank}}$ and corresponding $V_{\text{bias}}$ values along with the peak $K_{VCO}$ and $K_{VCO}$ at tuning voltage of 550 mV where the peak $K_{VCO}$ is the highest $K_{VCO}$ value seen for a particular combination of $C_{\text{bank}}$ and $V_{\text{bias}}$. $K_{VCO}$ variation shown in Table I is also plotted in Fig. 6, which shows that variation in $K_{VCO}$ of 3.82%. Fig. 6 also depicts the degradation of the $K_{VCO}$ variation to 6.57% without a significant increase in tuning range when $V_{\text{bias}}$ tuning is disabled and the $K_{VCO}$ variation across process corners with the slow process corner variation of 8.57%. This is a significant improvement in $K_{VCO}$ variation reduction as compared to other related works, which demonstrate a variation in the range of 40 MHz/V - 600 MHz/V [5] - [10]. Fig. 7 shows the variation in phase noise at 1 MHz offset with the change in $C_{\text{bank}}$ values. Minimum phase noise of -118.638 dBc/Hz is obtained for 1.1 pF value of $C_{\text{bank}}$, which corresponds to the highest frequency range (near 2.94 GHz). As shown in Fig. 7, phase noise degrades as the capacitance is increased, which is expected due to the increased losses in $C_{\text{bank}}$ switches. Fig. 8 shows the variation in phase noise performance considering all the active and passive components across the different process corners for minimum $C_{\text{bank}}$ value. As shown in the figure, phase noise at 1 MHz offset at 2.94 GHz center frequency is < −117 dBc/Hz across the corners.

Table II presents the performance summary and comparison of the proposed design with other recently reported work. As shown in the table, $K_{VCO}$ variation is minimum in the proposed VCO as compared to the other works. Moreover, phase noise is also better as compared to the other works. Our design has a low tuning range compared to others as our proposed architecture is aimed at low $K_{VCO}$ design specific for NV magnetometry, where reduced tuning range is

![Fig. 5. Variation of VCO output frequency and peak $K_{VCO}$ values with $V_{\text{tune}}$ for a lowest, highest and middle band](image1)

![Fig. 6. $K_{VCO}$ variation across frequency bands](image2)

![Fig. 7. Phase noise variation across frequency bands](image3)
desirable. There is a clear trade-off between the tuning range, $K_{VCO}$ value and power consumption. For lower $K_{VCO}$, the tuning range decreases. However, the overall tuning range of the VCO can be increased by using a bigger capacitor bank with more unit capacitance as per the requirement, which will consume more power. For a fair comparison of VCO performance considering the $K_{VCO}$ variations ($\Delta K_{VCO}$ in %), we propose a new figure-of-merit (FoM), which is shown in Eq. (16).

$$FoM = \frac{\left(\frac{\Delta f}{f}\right)^2}{P_D C \times PN \times \Delta K_{VCO} (\%)}$$  \hspace{1cm} (16)

As shown in table II, FoM of the proposed design is significantly higher than the other designs except [8] which has higher FoM owing to its exceptionally low power consumption at lower technology node.

V. CONCLUSION

In this work, we presented a technique to design an LC VCO with low gain and reduced gain variation, which are often needed in highly sensitive quantum sensing applications. A new FoM has been also defined in this work to capture the effect of $K_{VCO}$ variations on VCO performance. The proposed LC VCO is designed in 180 nm CMOS technology. Post layout simulation results show that it consumes 5 mA current from 1.8 V supply and exhibits a phase noise and FoM of -118.64 dBc/Hz and 172.44 dBc/Hz, respectively at 1 MHz offset at center frequency of 2.94 GHz. The proposed LC VCO achieves a tuning range of 2.75 - 2.94 GHz and exhibits low $K_{VCO}$ (< 38 MHz/V) with low $K_{VCO}$ variation (< 20 MHz/V) of 3.82%, which are much better than the other previously reported works.

REFERENCES