A Sub-nW, 8T Current Reference ConsumingConstant Power w.r.t Process Temperature

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Abstract—The paper presents an eight transistor (8T) picowatt current reference with a novel method of rectifying the problem of exponential power increase w.r.t temperature in traditional sub-nW references. The proposed current reference is obtained by modifying the traditional beta-multiplier architecture to scaledown the power consumption without sacrificing area. The constancy of power consumption w.r.t temperature is achieved by exploiting the voltage-current characteristics of a leakage transistor in the modified architecture. The proposed current reference, implemented in UMC 55nm technology, occupies an area of $0.00035mm^2$. It is designed for a current of 60pA and achieves an accuracy of 19 $ppm/{}^{0}C$ over a wide temperature range of $-55^{\circ}C$ to $125^{\circ}C$. The reported line sensitivity for the current reference is 0.07%/V in the supply range of 1.2V - 4V. Post-trim results show a constant power consumption of 144pW w.r.t temperature and process variations @1.2V supply.

I. INTRODUCTION

Internet of things forms a new class of computing, in that the data is driven by sensory interfaces, improving data accuracy and reducing human effort [1]. The evolving trends in shrinking the IoT devices and scaling down their power consumption led to a next class of computing, termed as Internet-of-Tiny-Things (IoT²) [2]. These ultra low power tiny devices, in conjunction with miniaturized batteries, open windows for a wide range of applications including biomedical, environmental and surveillance due to their lower form factor and longer lifetime.

Although active power consumption of these devices is taken care of by duty cycling, sleep mode power is a major concern in scaling down the power consumption. This poses constraints on 'Always on references' which occupy large portions of sleep mode power consumption. For eg. current references in watchdog timers must work with pico-watt power budget to reduce the overall sleep mode power consumption. Apart from ultra low power and low form factor requirements, these references are desired to be immune to supply variations.

Conventional current references are either variants of beta multipliers or based on cancelling temperature characteristics of voltage and resistance using an op-amp [3]–[5]. These architectures require resistance of 1Gohm to scale down the power consumption to pico-watts, thereby occupying very large area. [6] reports a 20pA current reference without using any resistance. However, they use the voltage reference as in [7] which suffers from the exponential increase in power consumption w.r.t temperature. At typical conditions, [7] reports post trim power consumption of 29pW at $20^{\circ}C$, while at $80^{\circ}C$ it consumes 2.5nW (i.e 80x increase in power consumption). This power consumption gets worsened further with process

variations. Similarly, other state-of-the-art pico watt voltage references also suffer from the power shoot up with temperature and process variations [8]-[10]. Though the current reference is trimmed to source/sink constant current with process and temperature variations, the underlying disadvantage of the voltage biasing circuit shoots up the power consumption. This paper proposes a current reference whose power consumption including the trimming circuitry is constant w.r.t temperature and process variations. The proposed current reference has been designed for 60pA, making it suitable for biasing various circuits (e.g. for biasing op-amps [11], [12]). The total posttrim current consumption is 120pA which is constant with temperature, process and supply variations. To the best of the authors knowledge, this is the first pico-watt current reference to resolve the exponential power consumption problem. Rest of the paper is organized as follows. Section II shows the circuit level implementation of the proposed current reference including the proposed trimming circuitry. Results are shown in section III. Finally, conclusions are drawn in section IV.

II. PROPOSED CURRENT REFERENCE

A. Design of the Current Reference



Fig. 1: Proposed current reference including W/L of transistors

The proposed current reference is shown in Fig 1. Transistors M2, M4 - M7 are regular thick oxide devices. M1 and M3 are native oxide devices and M0 is a thinner oxide device whose tunneling based gate leakage characteristics are exploited by operating it in the strong inversion region. A detailed explanation of the gate leakage is provided later.

A closer look at the circuit reveals that the proposed current reference is a modified version of the conventional beta multiplier architecture. The two main modifications include the replacement of a large physical resistor with a leakage transistor (thinner oxide device) and the use of native oxide device instead of a thick oxide device. The leakage transistor helps in scaling down the power consumption to pico-watts without compromising on area, since a large resistor (\sim 1Gohm) has been replaced by a single transistor. The use of native oxide devices is associated with the elimination of startup circuit since the architecture is a self-biased arrangement of transistors. In modern foundries, native oxides are widely available and do not incur additional mask steps [13]. Hence, the native oxide has been used as it doesn't incur any extra cost. The property of near-zero threshold voltage of the native oxide device is used in eliminating the use of a start-up circuit. This is explained as follows. Even if the circuit is struck at a degenerate bias point $(M_1, M_2 \text{ gates struck at ground and } M_6,$ M_7 gates struck at V_{DD}), the native oxide device turns on (as its threshold voltage is almost zero) and restores the operating point. Hence, the need of extra hardware and extra power consumption due to the start-up circuit is eliminated. Other modifications in the circuit include addition of transistors M_3 , M_4 and M_5 . Transistor M_3 is used as cascode device to enhance the supply rejection of the reference. Transistors $M_4 - M_7$ form a self-cascode current mirror. This kind of a current mirror is chosen because of its high output impedance and lower voltage headroom.

In an abstract way, the proposed current reference relies on the idea of obtaining a constant gate leakage by applying a suitable bias voltage at the gate of the leakage transistor. Gate leakage unlike other leakages increases marginally with temperature for a constant applied gate voltage [14]. So, if we apply a CTAT voltage to the gate of leakage transistor, we get a constant gate leakage current. This CTAT voltage is achieved by taking the difference between the threshold voltages of thick oxide and native oxide devices. A detailed analysis of the gate leakage is provided along with rigorous mathematical derivations to validate the abstract idea.

The gate tunneling current in the leakage transistor consists of Gate-to-Substrate Current (I_{gb}) , Gate-to-Channel Current (I_{gc}) and Gate-to-Source/Drain Currents $(I_{gs} \text{ and } I_{gd})$ [15]. However, in bulk technologies, the gate-to-substrate current is several orders of magnitude less than gate-to-channel and gate-to-S/D currents [16]. Hence, it is neglected. The currents I_{gs} and I_{gd} account for less than 3% change in the total gate leakage. Hence, they are also neglected. The dominant component of gate tunelling current is the gate-to-channel current (I_{gc}) given by [15]:

$$I_{gc} = W_{eff}L_{eff}.A.T_{oxRatio}.V_{gse}.V_{aux}.exp[-B.TOXE (AIGC - BIGC.V_{oxdepinv}).(1 + CIGC.V_{oxdepinv})]$$
(1)

Where W_{eff} , L_{eff} are effective width and effective length of the mosfet respectively. V_{aux} is a fitting function of the tunneling carrier density and available states. $V_{oxdepinv}$ is the voltage across the gate oxide in depletion/inversion region. Mathematical expressions for V_{aux} and $V_{oxdepinv}$ are given below. The parameters A, $T_{oxRatio}$, B, TOXE, AIGC, BIGC, CIGC, NIGC in eq.1 and eq.2 are constants for a given technology and are independent of temperature.

$$V_{aux} = NIGC.v_t.log\left(1 + exp\left(\frac{V_{gse} - V_{TH}}{NIGC.v_t}\right)\right)$$
(2)
$$V_{orderiny} = K_{1or}\sqrt{\phi_s} + (V_{as} - V_{th})$$
(3)

$$V_{oxdepinv} = K_{1ox} \sqrt{\phi_s} + (V_{gs} - V_{th}) \tag{3}$$

where ϕ_s is the surface potential equal to $V_{gs} - V_{oxdepinv}$. The term V_{gse} in eq.1 and eq.2 is the effective gate-source voltage across the channel. In bulk technologies, the difference between applied gate-source voltage and the effective gatesource voltage across the channel is negligible due to the lower extracted series resistance [17]. So the term V_{gse} is equal to V_{gs} . Now, an emphasis is made on the values of NIGC, AIGC, BIGC and CIGC to approximate eq.1 and eq.2. From [15], the values of NIGC, AIGC, BIGC and CIGC for an NMOS transistor are 1, 0.0136, 0.00171 and 0.075 respectively. Assuming gate leakage transistor to be in strong inversion ($V_{gs} - V_{TH}$ is 150mV to 200mV) and substituting NIGC = 1, we get $exp(V_{gse} - V_{TH}/NIGC.v_t) >> 1$. Substituting this in eq.2, we approximate V_{aux} in eq.4 as :

$$V_{aux} = log(e) * (V_{gs} - V_{th}) \tag{4}$$

The variation of the exponential term in equation 1 is less than 10% assuming a 10% change in $V_{oxdepinv}$. This assumption is justified at the end of the section. Even though $V_{oxdepinv}$ changes by a significant amount (i.e 10%), the overall variation in the exponential term is less because of the small values of BIGC and CIGC. Hence, the exponential term in eq.1 can be approximated by a linear fit curve given by $f(V_{oxdepinv}) = K_2(1 + aV_{oxdepinv})$, where a is a constant whose value is very small. So eq.1 can be finally simplified as :

$$I_{gc} = K * K_2 * V_{gs} (V_{gs} - V_{th}) (1 + aV_{oxdepinv})$$
 (5)

where $K = W_{eff} * L_{eff} * A * T_{oxRatio} * log(e)$. Eq.5 is differentiated w.r.t temperature to get the temperature coefficient of the gate leakage current. The temperature coefficient is then equated to zero to get a temperature compensated gate leakage current. The mathematical expression is given by :

$$aV_{gs}(V_{gs} - V_{th})\frac{\partial V_{oxdepinv}}{\partial T} + (V_{gs} - V_{th})(1 + aV_{oxdepinv})\frac{\partial V_{gs}}{\partial T} + V_{gs}(1 + aV_{oxdepinv})\left(\frac{\partial V_{gs}}{\partial T} - \frac{\partial V_{th}}{\partial T}\right) = 0 \quad (6)$$

The expression for $\frac{\partial V_{oxdepinv}}{\partial T}$ in eq.6 is obtained by differentiating eq.3 w.r.t temperature.

$$\frac{\partial V_{oxdepinv}}{\partial T} = \frac{\partial V_{gs}}{\partial T} - \frac{\partial V_{th}}{\partial T} * K_3 \tag{7}$$

where K_3 is given by :

$$K_3 = \left(\frac{2\sqrt{V_{gs} - V_{oxdepinv}}}{2\sqrt{V_{gs} - V_{oxdepinv}} + k_{1ox}}\right) \tag{8}$$

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Substituting eq.7 into eq.6 and simplifying further, we get :

$$\frac{\partial V_{gs}}{\partial T} = \frac{\partial V_{th}}{\partial T} * K_4 \tag{9}$$

where K_4 is given by :

$$K_{4} = \frac{aK_{3}V_{gs} + \frac{V_{gs}}{V_{gs} - V_{th}}(1 + aV_{oxdepinv})}{aV_{gs} + \frac{V_{gs}}{V_{gs} - V_{th}}(1 + aV_{oxdepinv}) + (1 + aV_{oxdepinv})}$$
(10)

From eq.9 and eq.10, we draw the following inferences. Since the temperature coefficient of V_{th} is negative, the required temperature coefficient of V_{qs} should also be negative (K_4 is a positive quantity which is evident from eq.10). Hence, V_{gs} (equal to V_{bias}) should be a CTAT voltage with a slope which can be calculated from eq.9 and eq.10. Note that the slope should have a very less dependence on process and temperature variations, because the dominant process and temperature dependent term $(V_{qs}/V_{qs}-V_{th})$ in K_4 appears in both numerator and denominator. To summarize, the required V_{bias} (refer Fig.1) should be a CTAT voltage whose slope can slightly vary with temperature and process to get a current reference with process invariant temperature coefficient. The expression for V_{bias} in the circuit can be deduced by equating the currents in transistors M1 and M2 which are collectively given by the well known sub-threshold current equation [18]:

$$I = \mu_1 C_{OX1} \frac{W_1}{L_1} (m_1 - 1) V_T^2 exp\left(\frac{V_{GS1} - V_{th1}}{m_1 V_T}\right)$$
$$= \mu_2 C_{OX2} \frac{W_2}{L_2} (m_2 - 1) V_T^2 exp\left(\frac{V_{GS2} - V_{th2}}{m_2 V_T}\right) \quad (11)$$

Here, the dependency of V_{DS} on the currents is ignored by applying the condition $V_{DS} > 4V_T$. Taking logarithm on both sides and simplifying equation 11, we get :

$$\frac{V_{GS2}}{m_2} - \frac{V_{GS1}}{m_1} = \frac{V_{th2}}{m_2} - \frac{V_{th1}}{m_1} + V_T ln \left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right)$$
(12)

The observed values of m_1 and m_2 are 1.1 and 1.05 respectively. To avoid complications in solving eq.12, we neglect the 5% error between m_1 and m_2 and consider them to be approximately equal (to m). This leads to eq.13.

$$V_{GS2} - V_{GS1} = V_{th2} - V_{th1} + mV_T ln \left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right)$$
(13)

Realizing that V_{GS2} - V_{GS1} = V_{bias} , we get eq.14

$$V_{bias} = V_{th2} - V_{th1} + mV_T ln \left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right)$$
(14)

Considering the temperature coefficients of V_{th1} to be k_1 and V_{th2} be k_2 ($k_1 > k_2$), the temperature dependency of V_{bias} can then be expressed as :

$$\frac{\partial V_{bias}}{\partial T} = k_2 - k_1 + m \frac{k}{q} ln \left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1} \right)$$
(15)

From eq.15, it is evident that by properly sizing M1 and M2, a CTAT voltage of desired slope can be achieved. As deduced earlier, this slope is independent of temperature and process variations. From eq.14 and eq.15, we have calculated the maximum change in V_{bias} and consecutively $V_{oxdepinv}$ with process and temperature variations. The maximum change in $V_{oxdepinv}$ is observed to be 7.7%, which justifies the linear fit assumption of the exponential term in eq.5.

B. Proposed Trimming Circuit



Fig. 2: Proposed Trimming Circuit

Although the temperature coefficient of current reference is less susceptible to process variations, the absolute value of the current reference varies with process. We propose the trimming circuit (as shown in Fig.2), where we switch on/off other leakage transistors depending on the trim bits, to bring back the current to its nominal value. Regular NMOS thick oxide devices are used as switches in the trimming circuitry due to their negligible gate leakage.

III. RESULTS AND DISCUSSION

The proposed current reference is implemented in UMC 55nm technology. Post trim simulations of the I_{ref} in various corners is shown in Fig. 3. In typical corner, the proposed reference achieves an accuracy of 19ppm, while in the worst corner FS, it achieves an accuracy of 85ppm. Fig. 4 shows the plot of I_{ref} with supply. The current reference works for a supply range of 1.2V - 4V with a very good line sensitivity of 0.07%/V. Fig. 5 shows the post trim power consumption w.r.t temperature and process variations. It can be deduced from Fig. 5 that the power consumption $(2*V_{DD}*I_{ref})$ is constant w.r.t temperature and process as the circuit doesn't involve any voltage biasing circuitry which suffers from the exponential increase in power consumption. Statistical performance of the current reference is validated through monte-carlo simulation and the results are shown in Fig.6. The average temperature coefficient is observed to be 73ppm, with a standard deviation of 50ppm. Fig. 7 shows a very low active area of $0.0003mm^2$. I_{ref} requires a start up time of 5ms for 100fF load capacitance.

IV. CONCLUSION

An 8T Current Reference with 19ppm accuracy and very good line sensitivity of 0.07%/V is proposed. The power consumption (144pW @1.2V) is constant with process and temperature. The current reference relies on applying a CTAT voltage to the gate of the leakage transistor to output a constant current. The idea is proven by rigorous mathematical analysis.

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Fig. 3: Post trim simulation of current I_{ref} w.r.t temperature in different process corners



Fig. 4: Line sensitivity of I_{ref}



Fig. 5: Post trim power consumption w.r.t temperature in different process corners

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Fig. 6: Montecarlo simulation of temperature coefficient



Fig. 7: Layout of proposed current reference

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