A 419pW Process-Invariant Temperature Sensor for Ultra-Low Power Microsystems

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***Abstract*—The paper presents a sub-nW BJT based temperature sensor for ultra-low power microsystems. The sensor is based on amplifying the difference between base-emitter voltages of BJTs using gate-leakage transistors. Implemented in UMC 65nm technology, the sensor occupies an area of $0.005mm^2$. It achieves a maximum non-linearity error of $0.12^oC(3\sigma)$ over the temperature range of -55^oC to 80^oC. Without any trimming, a worst case inaccuracy of $+0.36^oC/-1.61^oC$ is observed w.r.t process variations, depicting the process-invariant nature of the temperature sensor. It also achieves a low supply sensitivity of $0.56^oC/V$ over a wide supply range of 0.7V-3V. The power consumption of the sensor is 419pW at 27^oC and 0.7V supply.**

***Index Terms*—Beta-Multiplier, Ultra-Low Power Microsystems.**

I. Introduction

Ultra-low power wireless microsystems have demonstrated their feasibility in various IoT applications such as environmental monitoring, medical care and surveillance. These systems are often powered by miniaturized batteries or energy harvesters, which limit their total power consumption to tens of μW. Additionally, energy harvesters demand these systems to work for sub-1V supplies, while miniaturized batteries demand usability in a wide supply range precluding the need for a voltage regulator. Temperature sensors being an integral part of these systems, are desired to satisfy these demands. These temperature sensors often use a proportional-to-absolute-temperature (PTAT) sensing element to transduce the temperature to a voltage, which is then converted to a digital code. The overall system power consumption pushes the power budget of the temperature sensor to less than 10nW. This further constrains the power budget of the PTAT sensing element to sub-nW levels. Apart from these constraints, the PTAT sensing element is desired to be process-invariant to avoid multiple calibrations, thereby reducing the cost.

The past few decades have witnessed various types of temperature sensors. Most of the conventional temperature sensors incorporate Bipolar Junction Transistors (BJTs) [1]–[4] for generating a temperature dependent voltage (usually a Proportional-To-Absolute-Temperature (PTAT)). This is done by taking the difference between the base-emitter voltages (ΔV_{BE}) of two vertical PNP transistors. Although the obtained PTAT voltage is highly linear and process-invariant, the power consumption of the PTAT generator is of the order of μW, which makes them unsuitable for ultra-low power microsystems. Moreover, they do not work for lower supply voltages. As a result, MOSFET based temperature sensors have been introduced [5]–[8] in which the subthreshold region of operation has been exploited to generate PTAT voltages while consuming low power. Although the use of MOSFETs have facilitated the working of circuits at lower supplies, the temperature dependent voltages show a significant deviation w.r.t process variations (as in [5], [6]), demanding the need for one-point or two-point calibration techniques. Moreover, the power consumption of the PTAT generators is still high for the targeted applications [9]. [7] and [8] use architectures which generate process independent PTAT voltages. However, the architectures still consume nA currents and to scale down their current consumption to pA, impractical resistances of the order of $G\Omega$s must be used. To alleviate these issues, novel pico-watt PTAT sensing elements have been proposed in the literature [10]–[12]. Although these elements consume power in the order of pW, they suffer from the effect of process variations as the PTAT voltages are a function of threshold voltages of the transistors.

This paper proposes a pico-watt BJT based temperature sensor which generates a process-invariant PTAT voltage, thereby avoiding multi-point calibrations and reducing cost. The proposed sensor works for a wide supply range of 0.7V-3V and consumes power in the sub-nW range, thereby facilitating its usage with energy harvesters and miniaturized batteries. The rest of the paper is organized as follows. Section II discusses the circuit level implementation of the proposed sensor. Results are shown in section III and conclusions are drawn in section IV.

II. Design and Analysis of the Temperature Sensor

The proposed temperature sensor is shown in Fig. 1(a). T1 and T2 are vertical PNP transistors. M1, M2 and M3 are regular thick oxide PMOS transistors while M4-M10 are thin oxide PMOS transistors. These thin oxide devices are also known as gate-leakage transistors, as tunneling currents of the order of fA to pA flow through the gate of these devices [13]. They can serve as effective replacements for $G\Omega$ physical resistances due to their compact size and provision of sub-nA currents [14]–[16]. A single stage differential amplifier (with 52dB open loop gain) has been used to ensure the negative feedback in the loop (shown in Fig.1(b)). It is biased by a beta-multiplier circuit in which the physical resistance is replaced by a gate-leakage transistor to ensure sub-nW power consumption. A start-up circuit [17] has been used for the feedback loop and beta-multiplier (as shown in Fig.1) to avoid degenerate bias points in the temperature sensor.

The voltage V_{PTAT1} at the gate of transistor M4 is given by the difference between the base-emitter voltages of PNP transistors T1 and T2:

$$V_{PTAT1} = V_{EB1} - V_{EB2} \tag{1}$$

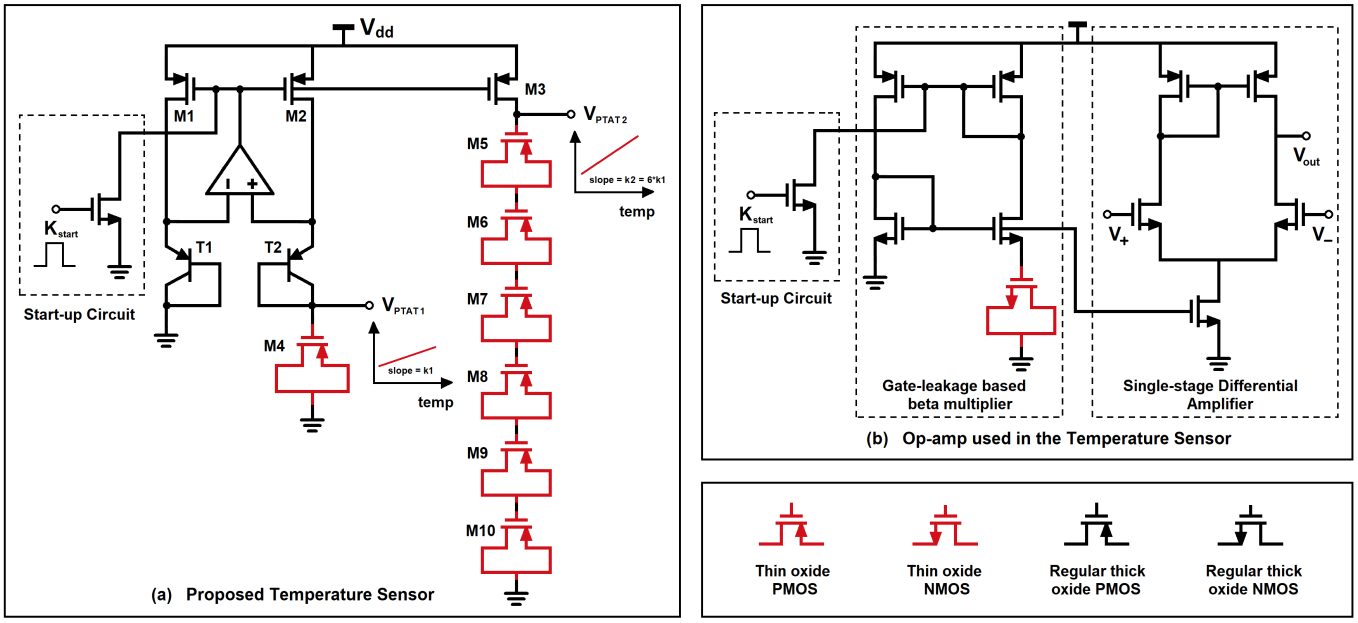

Fig. 1: Proposed Temperature Sensor

Considering the I-V relationship of a BJT, equation 1 can be re-written as :

$$V_{PTAT1} = V_T ln\left(\frac{I_{01}}{I_{S1}}\right) - V_T ln\left(\frac{I_{02}}{I_{S2}}\right) \tag{2}$$

Here, transistor T2 consists of n_1 parallel units, each identical to T1 and current in T1 is n_2 times that in T2. This implies that $I_{01} = n_1 I_{02}$ and $I_{S2} = n_2 I_{S1}$, which upon substitution in equation 2 leads to equation 3:

$$V_{PTAT1} = V_T ln(n) \tag{3}$$

where $n = n_1 * n_2$. The slope of V_{PTAT1} is equal to $(k/q)ln(n)$ and to achieve higher slope values, n must be impractically large [18]. For acceptable values of n (in this case, n is chosen to be 20), the PTAT voltage must be amplified in order to obtain higher slope values and thereby higher sensitivity to temperature. Since gate-leakage transistors can be visualized as resistances, the amplified voltage can be achieved by multiplying V_{PTAT1} by a factor equal to the ratio of equivalent resistance of the series combination of M5-M10 and resistance of M4. This is done as shown in Fig.1 where the expression for the amplified voltage V_{PTAT2} is given by :

$$V_{PTAT2} = \frac{R2}{R1}\left(V_T ln(n)\right) \tag{4}$$

where R1 is resistance of M4 and R2 is the equivalent resistance of the series combination of M5-M10. The aspect ratio of M4 is set in order to achieve a desired bias current of 80pA in M2 and M3. Transistors M5-M10 are replicated versions of M4 with all of them having same aspect ratios as that of M4. Since same current is made to flow through M4 and the stack M5-M10, by symmetry arguments it can be concluded that $R2 = 6R1$. Hence, V_{PTAT2} is an upscaled version of V_{PTAT1} by a factor of 6. Considering the trade-off between area and power consumption, the values of n_1 and n_2 are chosen to be 4 and 5 respectively. With these values, the slope of V_{PTAT1} turns out to be $260\mu V/^oC$, which on upscaling by a factor of 6 gives a slope of $1.56mV/^oC$ for V_{PTAT2}. The slope of V_{PTAT2} can further be amplified by adding more replicas of M4 to the series combination of M5-M10 with the trade-off of area occupancy.

Although gate-leakage transistors can be visualized as resistances, the tunneling currents show a significant variation w.r.t temperature depending upon the gate-source voltage [19]. From equation 4, it can be seen that for V_{PTAT2} to be an exact upscaled version of V_{PTAT1} without any degradation in its linearity, the ratio R2/R1 must be temperature and process invariant. This is theoretically true owing to the symmetry arguments (voltage across each transistor from M5-M10 equals V_{PTAT1}). To validate this argument, the ratio R2/R1 is simulated w.r.t temperature across different process corners and also verified statistically through monte-carlo simulations. The results for these are shown in section III. Once R2/R1 becomes temperature and process invariant, V_{PTAT2} inherits only the temperature and process variation of the term $V_{EB1} - V_{EB2}$. Since the difference of base emitter voltages is highly linear and independent of process variations, V_{PTAT2} would become a highly linear process-invariant PTAT voltage.

III. Results and Discussion

The temperature sensor is implemented in UMC 65nm technology. Fig.2 shows the ratio R2/R1 w.r.t temperature in typical and worst case corners while Fig.3 shows the Monte-Carlo simulations results (both process and mismatch) for R2/R1 at 27^oC. It can be seen from both these graphs that the maximum error in R2/R1 due to temperature variation is 0.59% and that due to process and mismatch variations ($\pm 3\sigma$) is 0.8%. These errors are negligible, showing that

the ratio R2/R1 is temperature and process invariant. This justifies that V_{PTAT2} inherits the linearity and process invariance of V_{PTAT1} as explained in section II. Fig.4 shows the variation of V_{PTAT2} w.r.t temperature in different corners while Fig.5 shows the non-linearity error w.r.t temperature in typical and worst case corners. The maximum non-linearity error is observed to be 0.025% (translates to 0.12^oC) which indicates that the temperature sensor is highly linear. Without any calibration, the deviations in the worst case corners from the typical value are +0.1%/-0.5% ($+0.36^oC/-1.61^oC$). To further validate the process invariance claim, monte-carlo simulations are run (both process and mismatch) for the slope of V_{PTAT2} at 27^oC (shown in Fig.6). From the reported mean and standard deviations, it can be seen that the maximum inaccuracy ($\pm 3\sigma$) in the slope of the temperature sensor due to process and mismatch variations is 2.4%. All the results from Fig.2 to Fig.6 depict that the temperature sensor is highly linear and process invariant. Fig.7 shows the line sensitivity of the temperature sensor in different process corners. An excellent line sensitivity of $0.56^oC/V$ is achieved in a wide supply range of 0.7V-3V. Fig.8 shows the start-up time of the temperature sensor, which is observed to be 15ms (considering that it has reached 95% of its steady state value). The reported start-up time is quite high, but comparable to the state-of-the-art pico-watt self-biased circuits [14]. Fig. 9 shows the layout of the proposed temperature sensor from which the area is calculated to be $0.005mm^2$. Finally, table I compares the state-of-the-art and proposed temperature sensors.

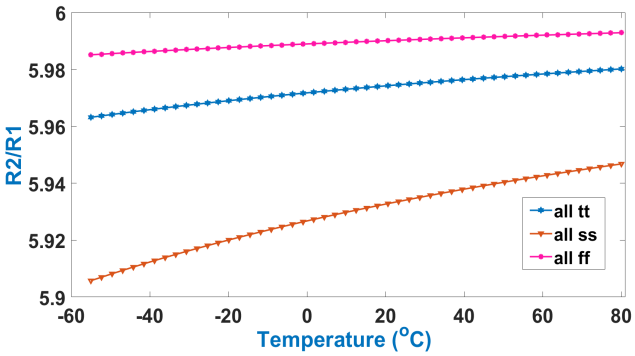

Fig. 2: R2/R1 w.r.t temperature across different corners

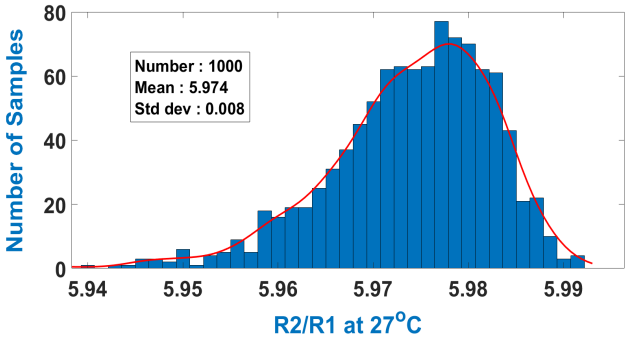

Fig. 3: Monte-Carlo simulation for R2/R1

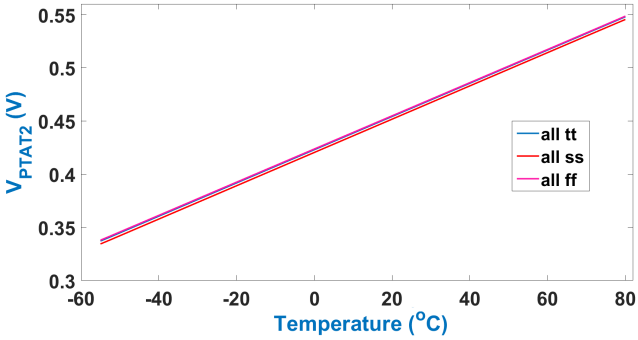

Fig. 4: V_{PTAT2} in different process corners

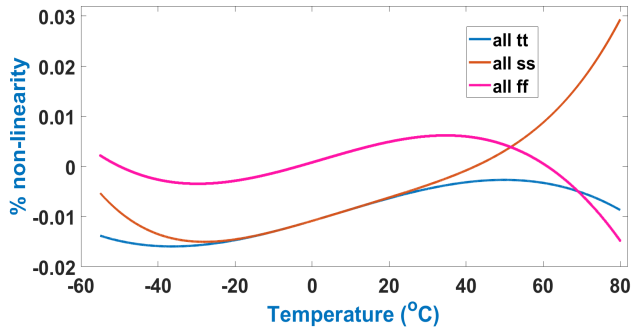

Fig. 5: % non-linearity in different process corners

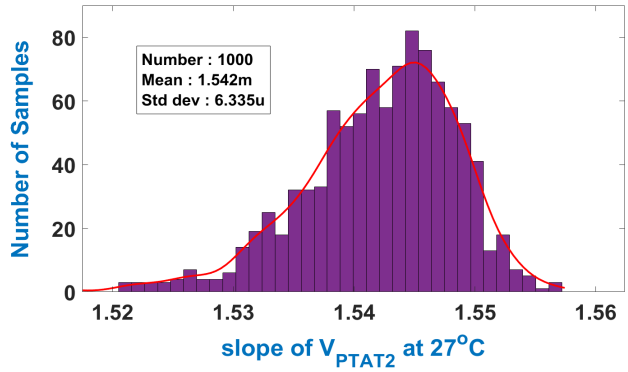

Fig. 6: MC simulation for slope of V_{PTAT2}

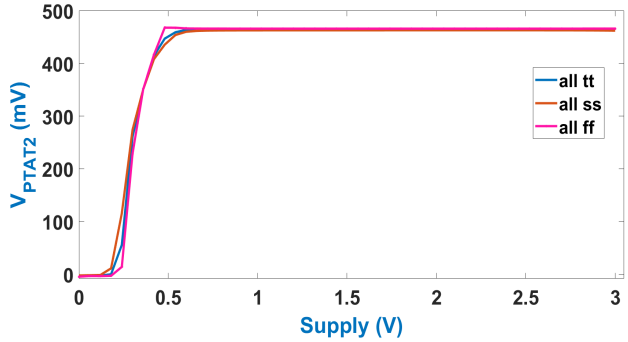

Fig. 7: Line sensitivity of V_{PTAT2} in diff. corners

TABLE I: COMPARISON WITH STATE-OF-THE-ART ARCHITECTURES

Specifications	**This Work**	[1]	[2]	[7]	[8]	[10]	[11]
Technology	**65nm**	160nm	160nm	180nm	180nm	180nm	65nm
PTAT Generation	**BJT**	BJT	BJT	CMOS	CMOS	CMOS	CMOS
Fully Integrated	**No**	Yes	Yes	No	No	Yes	Yes
Temperature Range (^oC)	**-55 to 80**	-55 to 125	-30 to 125	-55 to 125	-55 to 125	0 to 100	-20 to 40
Sensing Accuracy[1] (3σ)	$\mathbf{+0.1^oC/-0.02^oC}$	NA	NA	$\pm 0.4^oC$	$\pm 0.4^oC$	NA	NA
Process Spread (3σ)	$\mathbf{+0.36^oC/-1.61^oC}$	$\pm 0.6^oC/\pm 0.15^oC$	$\pm 0.2^oC$	$\pm 0.6^oC$	NA	$+1.5^oC/-1.4^oC$	$\pm 1.93^oC$
Calibration	**No**	Untrimmed/1-point	1-point	No	1-point	2-point	NA
Supply Range	**0.7V-3V**	1.5V-2V	1.6V-2V	1.1V-3.5V	0.7V-3.6V	1V-1.4V	NA
Line sensitivity	$\mathbf{0.56^oC/V}$	$0.5^oC/V$	$0.1^oC/V$	0.11%/V	$0.23^oC/V$	$11.25^oC/V$	NA
Power Consumption[2]	**419pW**	5.1uW	7.36uW	108uW	47nW	71nW	113pW
Area (mm^2)	**0.005**	0.08	0.12	0.002	0.82	0.09	0.15

[1]**Sensing Accuracy - error due to non-linearity in sensing**

[2] **Power Consumption calculated at least supply voltage**

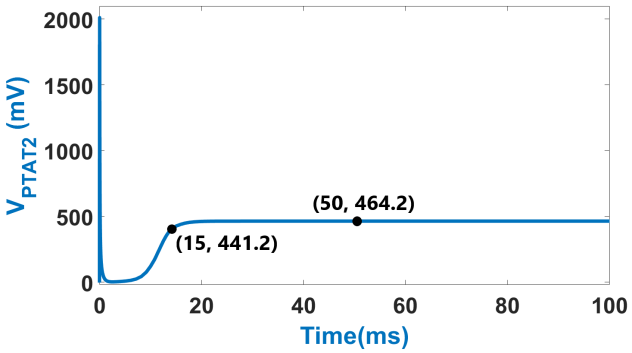

Fig. 8: Start-up time

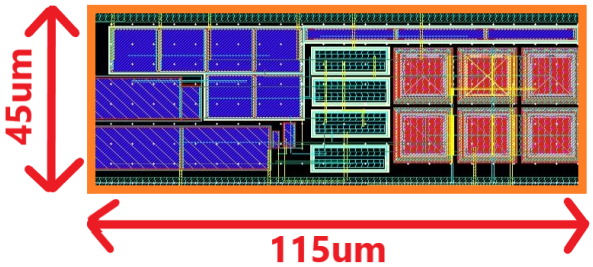

Fig. 9: Layout of the proposed temperature sensor

IV. CONCLUSION

A sub-nW BJT based temperature sensor has been proposed which inherits the advantages of BJT based PTAT voltage generation for process invariant nature and gate-leakage transistors for pico-watt power consumption. The claims of process-independent nature of the temperature sensor are proven by various monte-carlo simulations. Apart from being process invariant, the sensor works for a wide supply range of 0.7V-3V, achieving a low supply sensitivity of $0.56^oC/V$.

REFERENCES

[1] K. Souri, Y. Chae, and K. A. Makinwa, "A CMOS Temperature Sensor with a Voltage-Calibrated Inaccuracy of $\pm 0.15^oC(3\sigma)$ from -55^oC to 125^oC," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 292–301, 2012.

[2] K. Souri and K. A. Makinwa, "A $0.12mm^2$ $7.4\mu W$ Micropower Temperature Sensor with an Inaccuracy of $\pm 0.2^oC(3\sigma)$ from 30^oC to 125^oC," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1693–1700, 2011.

[3] B. Yousefzadeh, S. H. Shalmany, and K. A. Makinwa, "A BJT-Based Temperature-to-Digital Converter With ± 60 mK (3σ) Inaccuracy From -55^oC to 125^oC in 0.16μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1044–1052, 2017.

[4] M. Pertijs, A. Niederkorn, X. Ma, B. McKillop, A. Bakker, and J. Huijsing, "A CMOS Temperature Sensor with a 3σ Inaccuracy of $\pm 0.5^oC$ From -50^oC to 120^oC," *ISSCC Dig. Tech. Papers*, pp. 200–201, 2003.

[5] K. Souri, Y. Chae, F. Thus, and K. Makinwa, "12.7 A 0.85V 600nW All-CMOS Temperature Sensor with an Inaccuracy of$\pm 0.4^oC(3\sigma)$ from -40 to 125^oC," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 222–223, IEEE, 2014.

[6] M. K. Law, A. Bermak, and H. C. Luong, "A Sub-μW Embedded CMOS Temperature Sensor for RFID Food Monitoring Application," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1246–1255, 2010.

[7] S. K. Maddikatla and S. Jandhyala, "An Accurate All CMOS Temperature Sensor for IoT Applications," in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 349–354, IEEE, 2016.

[8] A. Ali, S. Kiran, A. Jain, and Z. Abbas, "A 47nW, 0.7-3.6 V Wide Supply Range, Resistor Based Temperature Sensor for IoT Applications," in *2019 IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC)*, pp. 293–298, IEEE, 2019.

[9] D. Blaauw, D. Sylvester, P. Dutta, Y. Lee, I. Lee, S. Bang, Y. Kim, G. Kim, P. Pannuto, Y. . Kuo, D. Yoon, W. Jung, Z. Foo, Y. . Chen, S. Oh, S. Jeong, and M. Choi, "IoT design space challenges: Circuits and systems," in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*, pp. 1–2, 2014.

[10] S. Jeong, Z. Foo, Y. Lee, J.-Y. Sim, D. Blaauw, and D. Sylvester, "A Fully-Integrated 71 nW CMOS Temperature Sensor for Low Power Wireless Sensor Nodes," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1682–1693, 2014.

[11] H. Wang and P. P. Mercier, "A 113 pW Fully Integrated CMOS Temperature Sensor Operating at 0.5 V," in *2017 IEEE SENSORS*, pp. 1–3, IEEE.

[12] H. Wang and P. P. Mercier, "A 763 pW 230 pJ/Conversion Fully Integrated CMOS Temperature-to-Digital Converter With $+0.81^oC/-0.75^oC$ Inaccuracy," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2281–2290, 2019.

[13] H. Wang and P. P. Mercier, "A Reference-Free Capacitive-Discharging Oscillator Architecture Consuming 44.4 pW/75.6 nW at 2.8 Hz/6.4 kHz," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 6, pp. 1423–1435, 2016.

[14] H. Wang and P. P. Mercier, "A 3.4-pW 0.4-V $469.3ppm/^oC$ Five-Transistor Current Reference Generator," *IEEE Solid-State Circuits Letters*, vol. 1, no. 5, pp. 122–125, 2018.

[15] H. Wang and P. P. Mercier, "A 14.5 pW, $31ppm/^oC$ Resistor-Less 5 pA Current Reference Employing a Self-Regulated Push-Pull Voltage Reference Generator," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1290–1293, IEEE, 2016.

[16] A. Ali, A. Pullela, A. Jain, and Z. Abbas, "A Sub-nW, 8T Current Reference Consuming Constant Power w.r.t Process & Temperature," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 730–733, 2020.

[17] H. Zhuang, X. Liu, and H. Wang, "Voltage Reference With Linear-Temperature-Dependent Power Consumption-," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 4, pp. 1043–1049, 2020.

[18] B. Razavi, "The Bandgap Reference [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 8, no. 3, pp. 9–12, 2016.

[19] Y.-S. Lin, D. Sylvester, and D. Blaauw, "A sub-pW timer using gate leakage for ultra low-power sub-Hz monitoring systems," in *2007 IEEE Custom Integrated Circuits Conference*, pp. 397–400, IEEE, 2007.