Virtual VLSI Laboratory for Computer Science students: Erudite and illusive

Shubhajit Roy Chowdhury
Centre for VLSI and Embedded Systems Technology,
IIIT Hyderabad,
Hyderabad, India
e-mail: src.vlsi@iiit.ac.in

Sandhya Kode
Centre for Education Technology and Learning Science
IIIT Hyderabad,
Hyderabad, India
e-mail: skodev@iiit.ac.in

***Abstract*—The paper reports a novel approach of self teaching Very Large Scale Integration (VLSI) to Computer Science students through the use of a Virtual laboratory. It formalizes the notion of hierarchical design of Integrated Circuits and abstracts the notion of design of integrated circuits based on physical approaches. Using the developed Virtual VLSI Laboratory, a set of about 100 Computer Science students have been trained and the feedback from them indicates that more than 80% of these students could understand the experiments being taught through the Virtual Laboratory and 70% of the students were interested in the field of VLSI Design after doing experiments in the lab.**

Keywords- Virtual Laboratory, VLSI, VHDL

I. INTRODUCTION

Programming is an integral and important part of learning Computer Science (CS) but anything other than programming seems to be a woe for CS students. Consequently, CS students consider courses like VLSI Design absolutely unnecessary [1]. As a matter of fact, young CS undergraduates lack exposure to circuits and systems. So, the current challenge is to show these students the possibility of extending their knowledge to the frontiers of VLSI Design. VLSI is an area where CS graduates can contribute significantly. Hence it is pertinent for CS students to learn electronics based courses such as digital logic, basic electronic devices and Hardware Description Language (HDL) programming. Numerous studies have revealed that engineering students learn best by practical work rather than when lectured [1]. However, the tools for VLSI design that are currently available are geared more for students of electronics engineering [2-6] as opposed to students of CS.

One way of inculcating interest for VLSI among CS students is to show them the operation and modeling of devices and circuits via programming. The idea behind this approach is that CS students, in general, are not very comfortable with hardware and devices. Software and simulations, on the other hand, attract CS students more than a circuit on a breadboard [1]. Moreover, an electronics lab needs equipment which is usually very expensive. This gap can be bridged to some extent if we provide virtual labs where students can draw circuits using a graphical user interface, and program the behavior of circuits, simulate and see the outputs and waveforms on their computer screens. This process is very hands-on and practical oriented ensuring learning by doing [7].

II. ALGORITHMIC APPROACH TO LEARN VLSI

CS students will be interested in the class if they can generate the actual hardware by writing code in a High Level Language which describes the behavior or algorithm of circuit operation. The properties of the actual hardware can be known when they simulate the circuit by various inputs.

This algorithmic approach provides an easy way to impart the basics of VLSI Design to the CS students who are somewhat reluctant to learn about the electronics of design. The approach is to provide a functional description of the system using a HDL. Then the virtual lab tool will synthesize and convert the same into a structural model with interconnections. This structural model can then be used in simulations to display properties modeled in the HDL functional description. Let us take the example of a half adder which forms the fundamental building block of most digital VLSI circuits. The flow chart of the half adder is shown in figure 1. The flowchart in figure 1 is depicted in the Very High Speed Integrated Circuit Hardware Description Language (VHDL) [8] architecture as shown below in figure 2. It is this architecture that has to be coded by the learner.

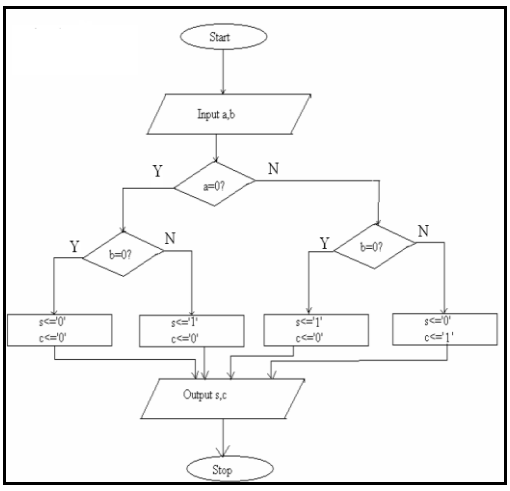

Figure 1. Flowchart depicting the behavior of half adder

```
architecture behave of ha is
   begin
   process(a,b)
   if (a='0')then
      c<='0';
   if(b='0')then
     s<='0';
     elsif(b='1')then
     s<='1';
     end if;
elsif(a='1')then
    if(b='0')then
       s<='1';
       c<='0';
    else
       s<='1';
       c<='1';
end behave;
```

Figure 2. VHDL architecture of the half adder

It is evident from this VHDL description that a student need not worry about the circuitry of the half adder and only needs to be concerned about its behavior. Our virtual lab synthesizes the circuitry of the half adder from the behavioral description. The design of the half adder is shown in figure 3.

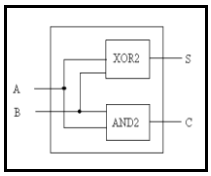

Figure 3. Design of the half adder

Once the design of the half adder is done, the virtual lab allows the circuit to be simulated using the regular techniques for simulation.

III. Results and Discussion

This Virtual VLSI lab was used by a group of 100 CS students for 3 months, after which a survey was conducted. A summary of the survey results is shown in Table 1.

TABLE I. Feedback summary from 100 CS students who used the Virtual VLSI Lab

Question	No. of students giving positive feedback
1. Was the interface understandable? (Yes/No)	83 (Yes)
2. Was the theory self explanatory? (Yes/No)	81 (Yes)
3. Was the manual self explanatory? (Yes/No)	89 (Yes)
4. Do you feel the experiments are too time consuming? (Yes/No)	84 (No)
5. Do you need to learn a lot about devices and circuits? (Yes/No)	82 (No)
6. Do you feel interested to work in VLSI? (Yes/No)	70 (Yes)

70% of the students were actually interested in working further in VLSI. As the initial results are very encouraging, more experiments can be designed to help in learning VLSI design. It is also evident that by using the right methodology and tools for teaching, a greater number of computer science students can be persuaded to learn about and experience VLSI design, VLSI tool development and applications.

IV. Challenges

Although the proposed approach is very efficient in terms of realizing circuit architectures from algorithms, it nonetheless suffers from a few drawbacks. The circuit architectures that are synthesized from the behavioural model may not be the most efficient ones. Optimizations at the logic level, transistor level and layout level require a considerable amount of human intervention and extensive design tools in the form of advanced virtual lab experiments.

V. Conclusion

The paper presents an approach to teaching and self teaching which allows for the CS student to model circuits in an algorithmic way and synthesize circuit architectures. Since the Virtual lab requires an individual to know the behavioural and functional description, the students are only required to model circuits algorithmically. Thus this approach and lab is very useful in teaching VLSI design to CS students.

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